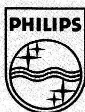
Small- signal Field-effect Transistors

BOOK SC07 1994

DATA HANDBOOK

Philips Semiconductors



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Small-signal Field-effect transistors

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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SELECTION GUIDE

N-channel junction field-effect transistors, general purpose

N-channel junction field-effect transistors for differential amplifiers

N-channel junction field-effect transistors for switching

P-channel junction field-effect transistors for switching

N-channel single-gate MOS-FETs for switching

N-channel dual-gate MOS-FETs

N-channel vertical D-MOS-FETs for switching

P-channel vertical D-MOS-FETs for switching

INTRODUCTION

The following tables represent our complete range of small-signal field-effect transistors, grouped according to main application area. Types added to the range since the last issue of Handbook SC07 (1991 issue) are shown in bold print.

N-channel junction field-effect transistors, general purpose

TYPE NUMBER	ENVELOPE	$\pm V_{DS}$ (V)	CHARACTERISTICS					REMARKS	PAGE
			I_G (mA)	I_{DSS} min.-max. (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. f = 1 kHz (mS)	C_{rs} (pF)		
BC264A	TO-92 var.	30	10	2 - 4.5	> 0.5	2.5	1.2	hi-fi amplifiers and AF equipment	51
BC264B				3.5 - 6.5		3			
BC264C				5 - 8		3.5			
BC264D				7 - 12		4			
BF245A	TO-92 var.	30	10	2 - 6.5	> 8	3 - 6.5	1.1	DC, LF and HF amplifiers	57
BF245B				6 - 15					
BF245C				12 - 25					
BF246A	TO-92 var.	25	10	30 - 80	0.6 - 14.5	8	3.5	VHF and UHF amplifiers; general purpose switching	69
BF246B				60 - 140					
BF246C				110 - 250					
BF247A	TO-92 var.	25	10	30 - 80	0.6 - 14.5	8	3.5	VHF and UHF amplifiers; general purpose switching	69
BF247B				60 - 140					
BF247C				110 - 250					
BF256A	TO-92 var.	30	10	3 - 70	7.5	4.5	0.7	VHF and UHF applications	71
BF256B				6 - 13					
BF256C				11 - 18					
BF410A	TO-92 var.	20 (note 1)	10	0.7 - 3	typ. 0.8	2.5	0.3	RF stages FM portables	83
BF410B				2.5 - 7	typ. 1.5	4		RF stages car radios	
BF410C				6 - 12	typ. 2.2	6		RF stages mains radios	
BF410D				10 - 18	typ. 3	7		mixer stages	
BF510	SOT23	20 (note 1)	10	0.7 - 3	typ. 0.8	2.5	0.3	RF stages FM portables	87
BF511				2.5 - 7	typ. 1.5	4		RF stages car radios	
BF512				6 - 12	typ. 2.2	6		RF stages mains radios	
BF513				10 - 18	typ. 3	7		mixer stages	

TYPE NUMBER	ENVELOPE	$\pm V_{DS}$ (V)	CHARACTERISTICS					REMARKS	PAGE
			I_G (mA)	I_{DSS} min.-max. (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. f = 1 kHz (mS)	C_{rs} (pF)		
BF545A **BF545B** **BF545C**	SOT23	30	10	2 - 6.5 6 - 15 12 - 25	0.4 - 7.8	3 - 6.5	0.8	DC, LF and HF amplifiers	93
BF556A **BF556B** **BF556C**	SOT23	30	10	3 - 7 6 - 13 11 - 18	0.5 - 7.5	4.5	0.8	DC, LF and HF amplifiers	105
BFR30 BFR31	SOT23	25	5	4 - 10 1 - 5	5 2.5	1 - 4 1.5 - 4.5	0.85	low-level, general purpose amplifiers	241
BFR200	SOT143	30	10	0.2 - 3.5	2	1.3	–	source follower	257
BFT46	SOT23	25	5	0.2 - 1.5	1.2	1	0.85	general purpose amplifier	261
BFU308 **BFU309** **BFU310**	TO-18	25	50	12 - 60 12 - 30 24 - 60	1 - 6.5 1 - 4 2 - 6.5	10	1.3	AM input stages UHF/VHF amplifiers	269
BFW10 BFW11	TO-72	30	10	8 - 20 4 - 10	8 6	3.5 - 6.5 3 - 6.5	0.6	broad band up to 300 MHz and differential ampl.	281
BFW12 BFW13	TO-72	30	5	1 - 5 0.2 - 1.5	2.5 1.2	2 1	0.6	low current, low voltage applications	293
BFW61	TO-72	25	10	2 - 20	8	2 - 6.5	< 2	general purpose amplifier	303
J308 **J309** **J310**	TO-92	25	50	12 - 60 12 - 30 24 - 60	1 - 6.5 1 - 4 2 - 6.5	10	1.3	AM input stages UHF/VHF amplifiers	629
PMBF4416 **PMBF4416A**	SOT23	30 35	10	5 - 15	6 2.5 - 6	4.5 - 7.5	0.8	AM input stages UHF/VHF amplifiers	653
PMBF5484 **PMBF5485** **PMBF5486**	SOT23	25	10	1 - 5 4 - 10 8 - 20	0.3 - 3 0.5 - 4 2 - 6	3 3.5 4	1	AM input stages UHF/VHF amplifiers	659
PMBFJ308 **PMBFJ309** **PMBFJ310**	TO-18	25	50	12 - 60 12 - 30 24 - 60	1 - 6.5 1 - 4 2 - 6.5	10	1.3	AM input stages UHF/VHF amplifiers	679
PN4416 **PN4416A**	SOT54	30 35	10	5 - 15	6 2.5 - 6	4.5 - 7.5	0.8	AM input stages UHF/VHF amplifiers	693

TYPE NUMBER	ENVELOPE	±V_{DS} (V)	CHARACTERISTICS					REMARKS	PAGE
			I_G (mA)	I_{DSS} min.-max. (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. f = 1 kHz (mS)	C_{rs} (pF)		
2N4416 **2N4416A**	TO-72	30 35	10	5 - 15	6 2.5 - 6	4.5 - 7.5	0.8	AM input stages UHF/VHF amplifiers	731
2N5484 **2N5485** **2N5486**	SOT54	25	10	1 - 5 4 - 10 8 - 20	0.3 - 3 0.5 - 4 2 - 6	3 3.5 4	1	AM input stages UHF/VHF amplifiers	749

Note

1. Asymmetrical.

N-channel junction field-effect transistors for switching

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		$R_{DS(on)}$ max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
BSJ108	TO-18	25	50	80	–	3	10	8	15	typ. 4	typ. 6	349
BSJ109				40	–	2	6	12				
BSJ110				10	–	0.5	4	18				
BSR56	SOT23	40	50	50	–	4	10	25	–	9	25	493
BSR57				20	100	2	6	40	5	10	50	
BSR58				8	80	0.8	4	60	–	20	100	
BSV78	TO-18	40	50	50	–	3.75	11	25	–	10	10	603
BSV79				20	–	2	7	40	5	18	16	
BSV80				10	–	1	5	60	–	30	32	
J108	TO-92	25	50	80	–	3	10	8	15	typ. 4	typ. 6	617
J109				40	–	2	6	12				
J110				10	–	0.5	4	18				
J111	TO-92	40	50	20	–	3	10	30	–	typ. 13	typ. 35	621
J112				5	–	1	5	50	–			
J113				2	–	0.5	3	100	–			
PMBF4391	SOT23	40	50	50	150	4	10	30	–	15	20	649
PMBF4392				25	75	2	5	60	3.5		35	
PMBF4393				5	30	0.5	3	100	–		50	
PMBFJ108	SOT23	25	50	80	–	3	10	8	15	typ. 4	typ. 6	667
PMBFJ109				40	–	2	6	12				
PMBFJ110				10	–	0.5	4	18				

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		$R_{DS(on)}$ max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
PMBFJ111	SOT23	40	50	20	–	3	10	30	–	typ. 13	typ. 35	671
PMBFJ112				5	–	1	5	50	–			
PMBFJ113				2	–	0.5	3	100	–			
PN4391	TO-92 var.	40	50	50	150	4	10	30	5	15	20	689
PN4392				25	100	2	5	60			35	
PN4393				5	60	0.5	3	100			50	
PZFJ108	SOT223	25	50	80	–	3	10	8	15	typ. 4	typ. 6	699
PZFJ109				40	–	2	6	12				
PZFJ110				10	–	0.5	4	18				
2N4091	TO-18	40	10	30	–	5	10	30	5	25	40	715
2N4092				15	–	2	7	50		35	60	
2N4093				8	–	1	5	80		60	80	
2N4391	TO-18	50	50	50	150	4	10	30	3.5	15	20	727
2N4392				25	75	2	5	60			35	
2N4393				5	30	0.5	3	100			50	
2N4856	TO-18	40	50	50	–	4	10	25	8	9	25	737
2N4857		40		20	100	2	6	40		10	50	
2N4858		40		8	80	0.8	4	60		20	100	
2N4859		30		50	–	4	10	25		9	25	
2N4860		30		20	100	2	6	40		10	50	
2N4861		30		8	80	0.8	4	60		20	100	

P-channel junction field-effect transistors for switching

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		$R_{DS(on)}$ max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
J174	TO-92	30	50	20	135	5	10	85	4	7	15	625
J175				7	70	3	6	125		15	30	
J176				2	35	1	4	250		35	35	
J177				1.5	20	0.8	2.25	300		45	40	
PMBFJ174	SOT23	30	50	20	135	5	10	85	4	7	15	675
PMBFJ175				7	70	3	6	125		15	30	
PMBFJ176				2	35	1	4	250		35	35	
PMBFJ177				1.5	20	0.8	2.25	300		45	40	

N-channel, single gate MOS-FETs for switching

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS									PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V) (note 1)		mode	$R_{DS(on)}$ max. (Ω)	C_{rs} typ. (pF)	t_{on}/t_{off} typ. (ns)		
				min.	max.	min.	max.						
BFR29	TO-72	30 (note 2)	20	10	40	0.5	3.5	depl.	–	0.4	–		233
BSD12	TO-72	20	50	–	–	–	2	depl.	30	0.6	1/5		331
BSD22	SOT143	20	50	–	–	–	2	depl.	30	0.6	1/5		335
BSD212 BSD213 BSD214 BSD215	TO-72	10 10 20 20	50	–	–	0.1	2	enh.	70	0.6	1/5		339
BSS83	SOT143	10	50	–	–	0.1	2	enh.	45	0.6	1/5		497
BSV81	TO-72	30 (note 2)	25	–	–	–	–	depl.	100	0.5	–		611

Notes

1. Enhancement types $V_{GS(th)}$.
2. V_{DB}/V_{SB}.

N-channel, dual gate MOS-FETs

All types protected against excessive input voltage surges.

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS						REMARKS	PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} min.- max. (mA)	$-V_{(P)G1-S}$ (note 1) max. (V)	$\|y_{fs}\|$ min. (mS)	C_{is} typ. (pF)	C_{os} typ. (pF)	F typ. (dB)		
BF901	SOT143	12	30	–	0.7	25	2.35	1.2	1.7	VHF & UHF	113
BF901R	SOT143R	12	30	–	0.7	25	2.35	1.2	1.7	VHF & UHF	113
BF904	SOT143	7	30	–	1.8	22	2.2	1.3	2	VHF & UHF	117
BF904R	SOT143R	7	30	–	1.8	22	2.2	1.3	2	VHF & UHF	117
BF908	SOT143	12	40	–	2	36	3.1	1.7	1.5	VHF & UHF	123
BF908R	SOT143R	12	40	–	2	36	3.1	1.7	1.5	VHF & UHF	123
BF960	SOT103	20	20	2 - 20	2.7	9.5	1.8	0.9	2.8	UHF	129
BF964S	SOT103	20	30	4 - 20	2.5	15	2.5	1	1	VHF	133
BF965	SOT103	20	30	2 - 20	2.5	15	2.5	1	1	VHF	139
BF966S	SOT103	20	30	4 - 20	2.5	15	2.3	0.8	1.8	UHF	143
BF980A	SOT103	18	30	–	1.3	18	2.6	1.1	2	UHF	149
BF981	SOT103	20	20	4 - 25	2.5	10	2.1	1.1	1	VHF	155
BF982	SOT103	20	40	–	1.3	20	4	2	1.2	VHF	163

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS						REMARKS	PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} min.- max. (mA)	$-V_{(P)G1-S}$ (note 1) max. (V)	$\|y_{fs}\|$ min. (mS)	C_{is} typ. (pF)	C_{os} typ. (pF)	F typ. (dB)		
BF988	SOT103	12	30	2 - 18	2.5	21	2.1	1.05	1	VHF & UHF	167
BF989	SOT143	20	20	2 - 20	2.7	9.5	1.8	0.9	2.8	UHF	179
BF990A	SOT143	18	30	–	1.3	18	2.6	1.2	2.8	UHF	183
BF990AR	SOT143R	18	30	–	1.3	18	–	1.2	2	UHF	187
BF991	SOT143	20	20	4 - 25	2.5	10	2.1	1.1	0.7	VHF	189
BF992	SOT143	20	40	–	1.3	20	4	2	1.2	VHF	193
BF992R	SOT143R	20	40	–	1.3	20	–	2	1.2	VHF	199
BF994S	SOT143	20	30	4 - 20	2.5	15	2.5	1	1	VHF	201
BF996S	SOT143	20	30	4 - 20	2.5	15	2.3	0.8	1.8	UHF	205
BF997	SOT143	20	30	2 - 20	2.5	15	2.5	1	1	VHF	209
BF998	SOT143	12	30	2 - 18	2.5	21	2.1	1.05	1	VHF & UHF	213
BF998R	SOT143R	12	30	2 - 18	2.5	21	2.1	1.05	1	VHF & UHF	223
BFR84	TO-72	20	50	20 - 55	3.8	12	5.5	3.5	2.3	general purpose	251

Note

1. Enhancement types $V_{GS(th)}$.

N-channel vertical D-MOS-FETs for switching

Total power dissipation (P_{tot}) measured at T_{amb} = 25 °C, unless otherwise specified.

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	$R_{DS(on)}$ (Ω)		at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
						typ.	max.				
BS107	TO-92 var.	200	120	500	typ. 1.8	15	28	20	2.6	10/10	305
BS107A	TO-92 var.	200	250	600	1 - 3	4.5	6.4	250	10	5/15	311
BS108	TO-92 var.	200	250	1000	0.4 - 1.8	5	8	100	2.8	10/30	315
BS170	TO-92 var.	60	500	830	0.8 - 3	2.5	5	200	10	10/10	317
BSD254	TO-92 var.	250	200	850	0.6 - 1.4	–	12	250	5	10/30	343
BSD254A	TO-92 var.	250	200	850	0.6 - 1.4	–	12	250	5	10/30	343
BSD254AR	TO-92 var.	250	200	850	0.6 - 1.4	–	12	250	5	10/30	343
BSN10	TO-92 var.	50	175	830	0.4 - 1.8	14	20	100	5	5/10	353
BSN10A	TO-92 var.	50	175	830	0.4 - 1.8	14	20	100	5	5/10	353
BSN12	TO-92 var.	50	150	830	0.4 - 1.8	20	30	100	5	4/8	357
BSN12A	TO-92 var.	50	150	830	0.4 - 1.8	20	30	100	5	4/8	357
BSN20	SOT23	50	100	250	0.4 - 1.8	14	20	100	5	5/10	359
BSN22	SOT23	50	100	250	0.4 - 1.8	20	30	100	5	4/8	363

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BSN204	TO-92	200	250	1000	0.4 - 1.8	5	8	100	2.8	10/30	365
BSN204A	TO-92	200	250	1000	0.4 - 1.8	5	8	100	2.8	10/30	365
BSN205	TO-92 var.	200	300	1000	0.8 - 2.8	4.5	6	400	10	10/20	369
BSN205A	TO-92 var.	200	300	1000	0.8 - 2.8	4.5	6	400	10	10/20	369
BSN254	TO-92 var.	250	300	1000	0.8 - 2.2	4.5	10	20	2.4	–	373
BSN254A	TO-92 var.	250	300	1000	0.8 - 2.2	4.5	10	20	2.4	–	373
BSN274	TO-92 var.	270	250	1000	0.8 - 2	6.5	14	20	2.4	10/30	377
BSN274A	TO-92 var.	270	250	1000	0.8 - 2	6.5	14	20	2.4	10/30	377
BSN304	TO-92 var.	300	250	1000	0.8 - 2	7.9	14	20	2.4	10/30	383
BSN304A	TO-92 var.	300	250	1000	0.8 - 2	7.9	14	20	2.4	10/30	383
BSP89	SOT223	240	350	1500	0.8 - 2	4	6	340	10	10/30	389
BSP106	SOT223	60	425	1500	0.8 - 3	2.5	4	200	10	5/15	397
BSP107	SOT223	200	200	1500	0.8 - 2.4	20	28	20	2.6	10/20	405
BSP108	SOT223	80	500	1500	1.5 - 3.5	2	3	500	10	8/15	413
BSP110	SOT223	80	325	1500	0.8 - 2.8	7	10	150	5	5/10	417
BSP120	SOT223	200	250	1500	0.8 - 2.8	7	12	250	10	6/20	421
BSP121	SOT223	200	350	1500	0.8 - 2.8	4.5	6	400	10	10/20	425
BSP122	SOT223	200	550	1500	0.4 - 2	1.6	2.5	750	10	35/50	431
BSP124	SOT223	250	250	1500	0.6 - 1.4	–	12	250	5	10/30	433
BSP126	SOT223	250	350	1500	0.8 - 2	5	10	20	2.4	10/30	439
BSP127	SOT223	270	350	1500	0.8 - 2	6.5	8	250	10	10/30	445
BSP128	SOT223	200	350	1500	0.4 - 1.8	5	8	100	2.8	10/30	447
BSP130	SOT223	300	300	1500	0.8 - 2	6.7	8	250	10	10/30	449
BSP152	SOT223	200	550	1500	1.5 - 3.5	–	2.5	750	10	15/30	455
BSS87	SOT89	200	280	1000	0.8 - 2.8	4.5	6	400	10	10/25	505
BSS88	TO-92 var.	230	250	1000	0.4 - 1.2	5	8	150	5	10/30	509
BSS89	TO-92 var.	200	300	1000	0.8 - 2.8	4.5	6	400	10	–	511
BSS91	TO-18	200	350	1500 (note 1)	0.8 - 2.8	4.5	6	400	10	15/25	515
BSS100	TO-92 var.	100	250	830	0.8 - 2.8	3	6	120	10	10/20	523
BSS123	SOT23	100	150	250	0.8 - 2.8	3	6	120	10	10/20	527
BST70A	TO-92 var.	80	500	1000	1.5 - 3.5	2	4	500	10	10/15	545
BST72A	TO-92 var.	80	300	830	1.5 - 3.5	7	10	150	5	10/10	549
BST74A	TO-92 var.	200	300	1000	0.8 - 2.8	6	12	250	10	10/25	553
BST76A	TO-92 var.	180	300	1000	0.7 - 2.7	7	10	15	3	10/15	557
BST78	TO-126	450	750	15000 (note 2)	2 - 4	10	14	100	10	10/100	561

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BST80	SOT89	80	500	1000	1.5 - 3.5	2	4	500	10	10/15	565
BST82	SOT23	80	175	300	1.5 - 3.5	7	10	150	5	10/10	569
BST84	SOT89	200	250	1000	0.8 - 2.8	6	12	250	10	10/25	573
BST86	SOT89	180	300	1000	0.7 - 2.7	7	10	15	3	10/15	577
BST124	TO-126	250	450	6000	1.4 - 0.6	–	12	250	5	10/30	597
PMBF107	SOT23	200	100	250	0.8 - 2.4	20	28	20	2.6	10/20	639
PMBF170	SOT23	60	250	300	0.8 - 3	2.5	5	200	10	10/15	645
VN2406L	TO-92 var.	240	210	1000	0.8 - 2	–	6	500	10	10/30	703
VN2410L	TO-92 var.	240	150	1000	0.8 - 2	–	10	100	2.5	10/30	709
2N7000	TO-92 var.	60	280	830	0.8 - 3	2.5	5.3	75	4.5	10/10	757
2N7002	SOT23	60	180	300	0.8 - 3	2.5	5.3	75	4.5	10/15	763

Notes

1. P_{tot} measured at T_{case} = 25 °C..
2. P_{tot} measured at T_{mb} = 75 °C.

P-channel vertical D-MOS-FETs for switching

P_{tot} measured at T_{amb} = 25 °C.

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS208	TO-92 var.	200	200	830	0.8 - 2.8	10	14	200	10	10/30	321
BS250	TO-92 var.	45	250	830	1.3 - 5	9	14	200	10	4/10	327
BSP92	SOT223	240	180	1500	0.8 - 1.8	12	20	180	10	10/30	393
BSP204	TO-92 var.	200	250	1000	0.8 - 2.8	10	15	200	10	–	461
BSP204A	TO-92 var.	200	250	1000	0.8 - 2.8	10	15	200	10	–	461
BSP205	SOT223	60	275	1500	1.5 - 3.5	7.5	10	200	10	6/15	467
BSP206	SOT223	60	350	1500	1.5 - 3.5	4.5	6	200	10	8/25	471
BSP220	SOT223	200	225	1500	0.8 - 2.8	10	12	200	10	20/30	475
BSP225	SOT223	250	225	1500	0.8 - 2.8	10	15	200	10	10/30	481
BSP254	TO-92 var.	250	200	1000	0.8 - 2.8	10	15	200	10	10/30	487
BSP254A	TO-92 var.	250	200	1000	0.8 - 2.8	10	15	200	10	10/30	487
BSS84	SOT23	50	130	360	0.8 - 2	6	10	100	5	20/43	501
BSS92	TO-92 var.	200	250	1000	0.8 - 2.8	10	20	100	10	–	519
BSS192	SOT89	200	150	1000	0.8 - 2.8	10	20	100	10	10/30	539
BST100	TO-92 var.	60	300	1000	1.5 - 3.5	4.5	6	200	10	4/20	581
BST110	TO-92 var.	50	300	830	1.5 - 3.5	7.5	10	200	10	4/20	585
BST120	SOT89	60	300	1000	1.5 - 3.5	4.5	6	200	10	4/20	589
BST122	SOT89	50	250	1000	1.5 - 3.5	7.5	10	200	10	4/20	593

MARKING CODES

Small-signal Field-effect Transistors

Marking codes

Types in SOT23, SOT89 and SOT143 envelopes are marked with a code as listed in the following tables.

TYPE NUMBER	MARKING CODE
BF510	S6p
BF511	S7p
BF512	S8p
BF513	S9p
BF545A	M65
BF545B	M66
BF545C	M67
BF556A	M84
BF556B	M85
BF556C	M86
BF901	M01
BF901R	M02
BF904	M04
BF904R	M06
BF989	MAp
BF990A	M87
BF990AR	M85
BF991	M91
BF992	M92
BF992R	M52
BF994S	MGp
BF996S	MHp
BF997	MKp
BF998	MOp
BF998R	MO$\overline{p}$
BFR30	M1p
BFR31	M2p
BFR200	M20
BSD20	M31
BSD22	M18
BSN20	M8p
BSN22	M18
BSR56	M4p
BSR57	M5p
BSR58	M6p
BSS83	M74

TYPE NUMBER	MARKING CODE
BSS84	Sp
BSS87	KA
BSS123	SA
BSS131	SR
BSS138	SS
BSS192	KB
BST80	KM
BST82	02p
BST84	KN
BST86	KO
BST120	LM
BST122	LN
PMBF107	pK2
PMBF170	pKX
PMBF4391	p6j
PMBF4392	p6K
PMBF4393	p6G
PMBF4416	P6A
PMBF4416A	M16
PMBF5484	p6B
PMBF5485	p6M
PMBF5486	p6H
PMBFJ108	p08
PMBFJ109	p09
PMBFJ110	p10
PMBFJ111	p11
PMBFJ112	p12
PMBFJ113	p13
PMBFJ174	p6X
PMBFJ175	p6W
PMBFJ176	p6S
PMBFJ177	p6Y
PMBFJ308	M08
PMBFJ309	M09
PMBFJ310	M10
2N7002	702

GENERAL

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QUALITY

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

quality assurance

based on ISO 9000 standards, customer standards such as Ford Q1 and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates

partnerships with customers

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes

partnerships with suppliers

ship-to-stock, statistical process control and ISO 9000 audits

quality improvement programme

continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- incoming material management through partnerships with suppliers
- in-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A germanium or other material with a band gap of 0.6 to 1 eV

B silicon or other material with a band gap of 1 to 1.3 eV

C gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.
In the following list low power types are defined by $R_{th\ j\text{-}mb}$ > 15 K/W and power types by $R_{th\ j\text{-}mb} \leq$ 15 K/W.

A diode; signal, low power

B diode; variable capacitance

C transistor; low power, audio frequency

D transistor; power, audio frequency

E diode; tunnel

F transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under '*Serial number*'

H diode; magnetic sensitive

L transistor; power, high frequency

N photocoupler

P radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q radiation generator; e.g. LED, laser; with special third letter

R control or switching device; e.g. thyristor, low power; with special third letter

S transistor; low power, switching

T control and switching device; e.g. thyristor, power; with special third letter

U transistor; power, switching

W surface acoustic wave device

X diode; multiplier, e.g. varactor, step recovery

Y diode; rectifying, booster

Z diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A for triacs, after second letter 'R' or 'T'

F for emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L for lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O for opto-triacs, after second letter 'R'

T for 3-state bicolour LEDs, after second letter 'Q'

W for transient voltage suppressor diodes, after second letter 'Z'.

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

EXAMPLES OF BASIC TYPE NUMBERS

AA112	germanium, low power signal diode (consumer type)
ACY32	germanium, low power AF transistor (industrial type)
BD232	silicon, power AF transistor (consumer type)
CQY17	GaAs, light-emitting diode (industrial type)
RPY84	CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%
B 2%
C 5%
D 10%
E 20%

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (µm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

S-PARAMETER DEFINITIONS

The S-parameter symbols in this section are based on IEC publication 747-7.

S-parameters (return losses or reflection coefficients) of a module can be defined as the S_{11} and the S_{22} of a two-port network (see Fig.1).

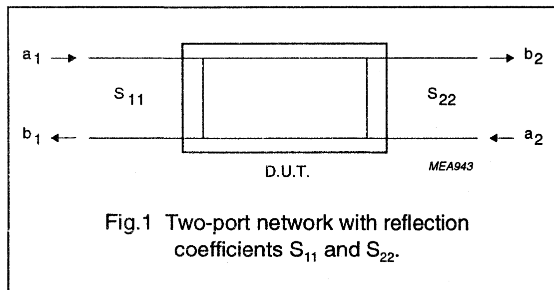


Fig.1 Two-port network with reflection coefficients S_{11} and S_{22}.

$$b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2 \quad (1)$$

$$b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2 \quad (2)$$

where

$$a_1 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_1) = \text{signal into port 1} \quad (3)$$

$$a_2 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_2 + Z_o \cdot i_2) = \text{signal into port 2} \quad (4)$$

$$b_1 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_1) = \text{signal out of port 1}$$

$$b_2 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_2 + Z_o \cdot i_2) = \text{signal out of port 2}$$

From (1) and (2) formulae for the return losses can be derived:

$$S_{11} = \frac{b_1}{a_1} \mid a_2 = 0 \quad (5)$$

$$S_{22} = \frac{b_2}{a_2} \mid a_1 = 0 \quad (6)$$

In (5), $a_2 = 0$ means output port terminated with Z_o (derived from formula (4)).

In (6), $a_1 = 0$ means input port terminated with Z_o (derived from formula (3)).

Measurement

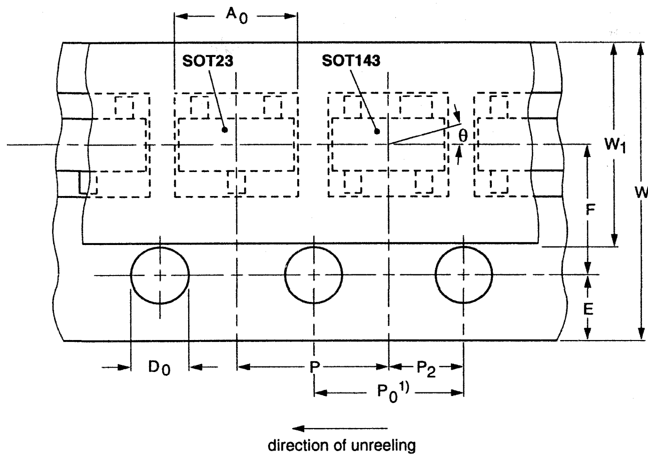
The return losses are measured with a network analyzer after calibration, where the influence of the test jig is eliminated. The necessary termination of the other port with Z_o is done automatically by the network analyzer.

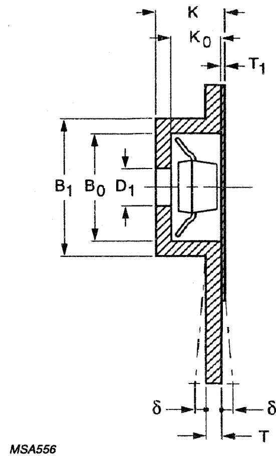
The network analyzer must have a directivity of at least 40 dB to obtain an accuracy of 0.5 dB when measuring return loss figures of 20 dB. A full two-port correction method can be used to improve the accuracy.

TAPE and REEL PACKING

Tape and reel packing meets the feed requirements of automatic pick and place equipment (packing conforms to IEC publication 286). The tape is an ideal shipping container, making handling easy and providing secure blister cavities in which the transistors are sealed with peel-off cover tape.

SOT23	8 mm tape, 7- or 13-inch reels
SOT143	8 mm tape, 7- or 13-inch reels
SOT89	12 mm tape, 7-inch reels
SOT223	12 mm tape, 7-inch reels

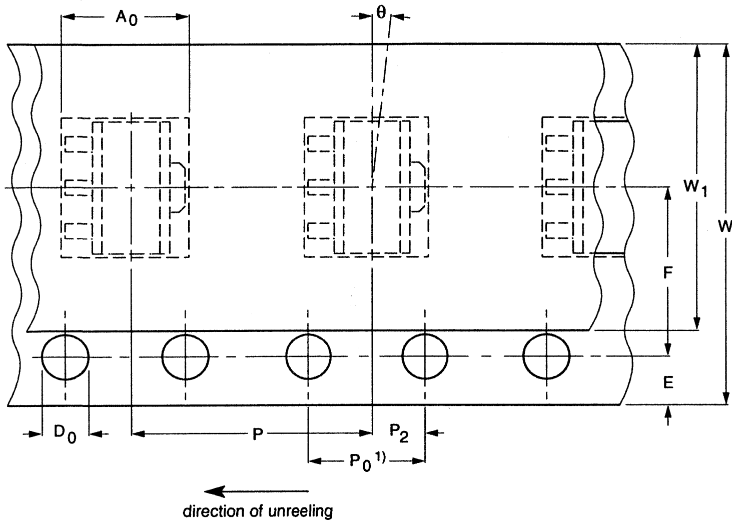


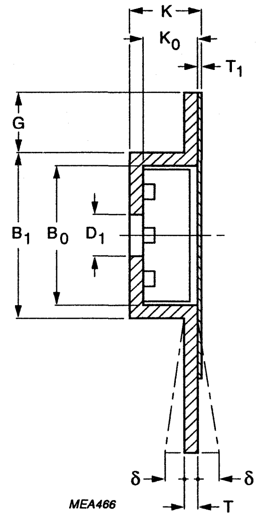


For dimensions see Table 5.

1) Tolerance over any 10 pitches: ±0.2 mm.

Fig.2 Specification for 8 mm tape (SOT23 and SOT143).

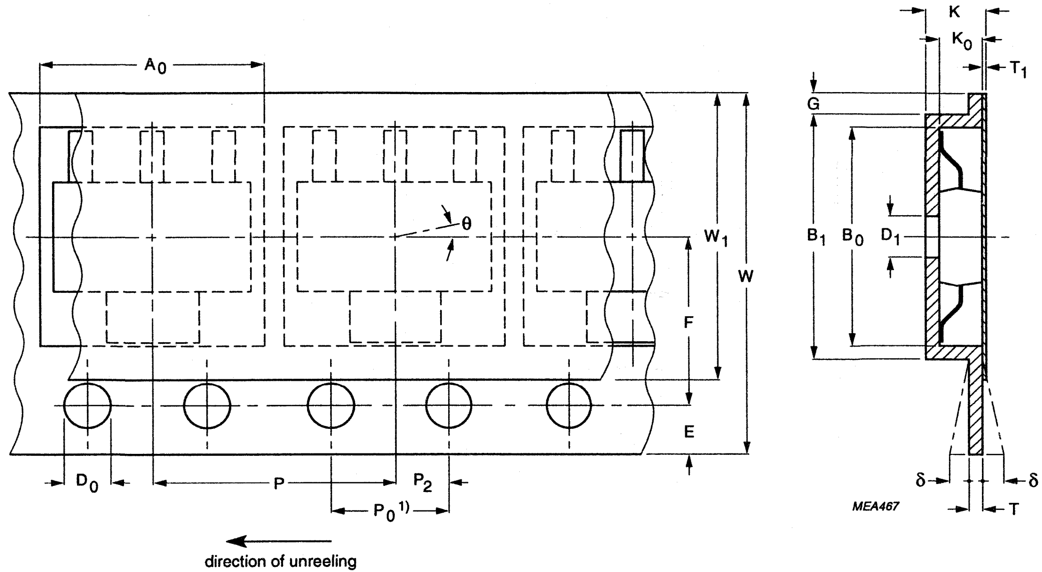




For dimensions see Table 5.

1) Tolerance over any 10 pitches: ±0.2 mm.

Fig.3 Specification for 12 mm tape (SOT89).



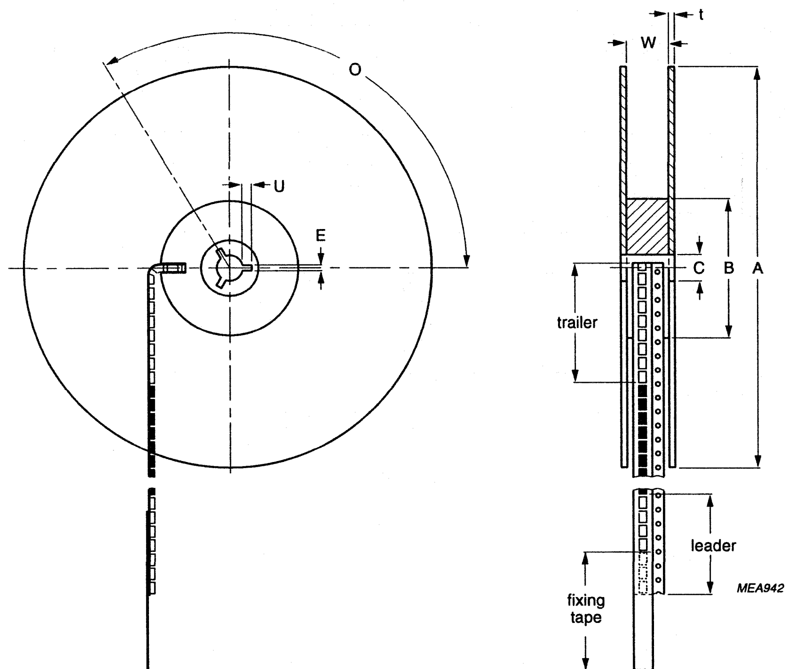
For dimensions see Table 5.

1) Tolerance over any 10 pitches: ±0.2 mm.

Fig.4 Specification for 12 mm tape (SOT223).

Table 5 Tape dimensions (in mm)

DIMENSION (Figs 2 to 4)	CARRIER TAPE FOR:			TOLERANCE
	SOT23 SOT143	SOT89	SOT223	
Overall dimensions				
W	8.0	12.0	12	±0.2
K	1.5	2.4	2.0	max.
G	–	1.8	0.75	min.
Sprocket holes				
D_0	1.5	1.5	1.5	+0.1/–0
E	1.75	1.75	1.75	±0.1
P_0	4.0	4.0	4.0	±0.1
Relative placement compartment				
P_2	2.0	2.0	2.0	±0.1
F	3.5	5.5	5.5	±0.05
Compartment				
A_0	component + 0.2	component + 0.2	component + 0.2	–
B_0	component + 0.2	component + 0.2	component + 0.2	–
B_1	3.3	5.7	8.0	max.
K_0	0.95 + 0.2	component	component	–
D_1	1.0	1.5	1.5	min.
P	4.0	8.0	8.0	±0.1
θ	15°	5°	5°	max.
Cover tape				
W_1	5.5 ±0.25	9.5 max.	9.5 max.	–
T_1	0.1	0.1	0.1	max.
Carrier tape				
W	8.0	12.0	12.0	±0.2
T	0.4	0.4	0.4	max.
δ	0.3	0.3	0.3	max.



For dimensions see Table 6.

Fig.5 Reel specification.

Table 6 Reel dimensions (in mm)

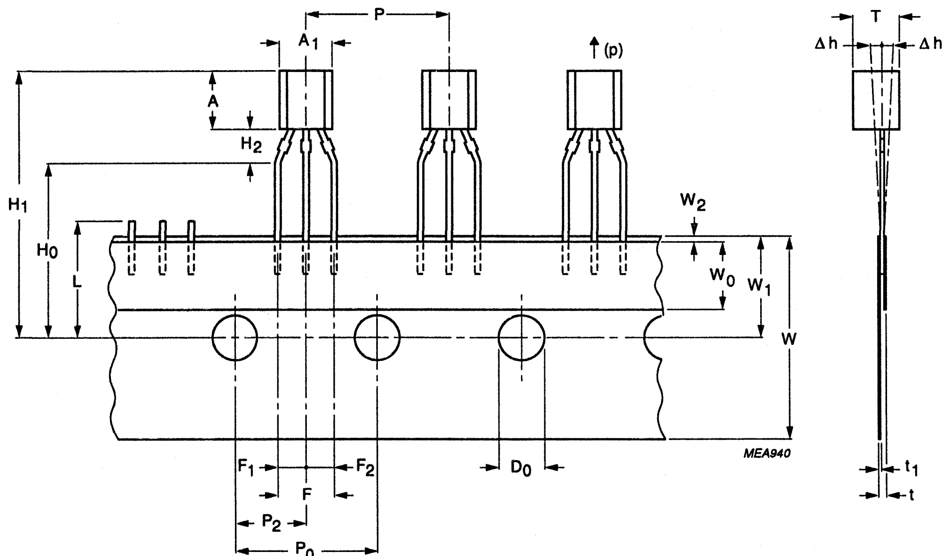
DIMENSION (Fig.5)	8 mm tape	12 mm tape	16 mm tape
Flange			
A	180	180	180
t	1.5	1.5	1.5
W	9.5	14.0	18.0
Hub			
B	62	62	62
C	12.75	12.75	12.75
Key slot			
E	2	2	2
U	4	4	4
O	120°	120°	120°

TO-92 transistors on tape

TO-92 transistors are supplied on tape in boxes (ammopacks) or on reels. The number per ammopack or per reel is 2000. Each ammopack has 80 layers of 25 transistors. Following the 25th transistor in each layer is an empty position that allows the layer to fold correctly. The maximum number of empty positions per tape is not more than 0.5% of the total number of transistors per tape, and a maximum of three consecutive transistors may be missing provided that this gap is followed by six consecutive transistors.

The ammopack is accessible from both sides to enable the user to choose 'normal' or 'reverse' tape. 'Normal' is indicated by a plus sign (+) on the ammopack and 'reverse' by a minus sign (–). Orientation of the TO-92 package is such that its flat side is the upper side of the tape.

Tape splicing is permitted: splice the tape on the back and/or front so the feed hole pitch is maintained (see Fig. 8).



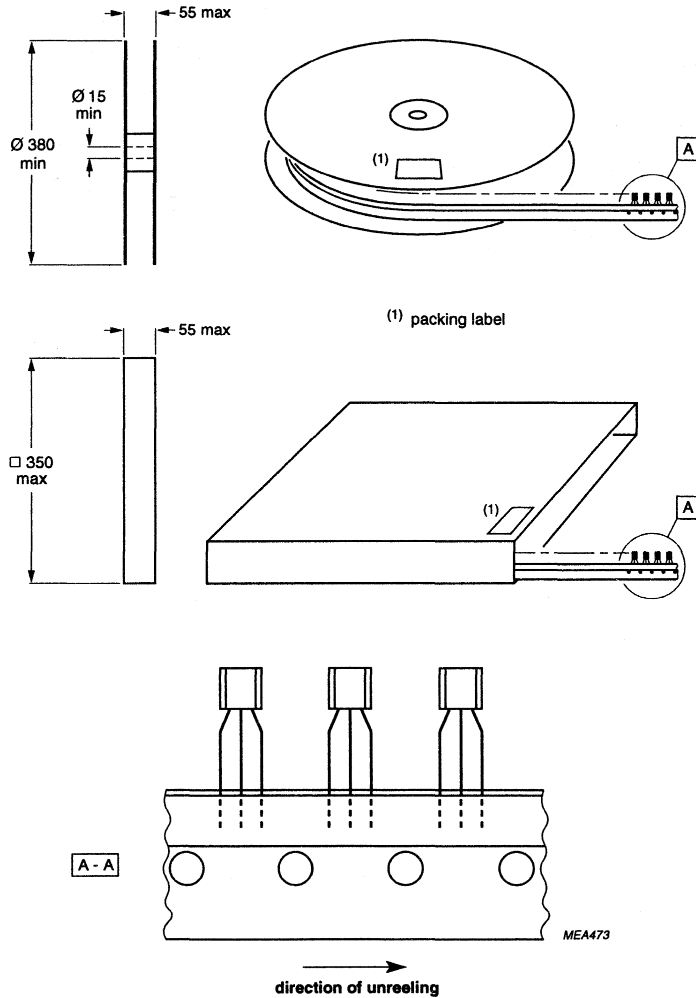
For dimensions see Table 7.

1) Tolerance over any 20 pitches: ±1.0 mm.

Fig.6 Specification for TO-92 tape.

Table 7 TO-92 tape dimensions

DIMENSION (Fig.6)	DESCRIPTION	MIN.	TYP.	MAX.	TOL.	UNIT
A_1	body width	4.0	–	4.8	–	mm
A	body height	4.8	–	5.2	–	mm
T	body thickness	3.9	–	4.2	–	mm
P	pitch of component	–	12.7	–	±1	mm
P_0	feed hole pitch	–	12.7	–	±0.3	mm
P_2	feed hole centre to component centre (measured at bottom of clinch)	–	6.35	–	±0.4	mm
F	distance between outer leads	–	5.08	–	+0.6/–0.2	mm
Δh	component alignment at top of body	–	0	1.0	–	mm
W	tape width	–	18.0	–	±0.5	mm
W_0	hold-down tape width	–	6.0	–	±0.2	mm
W_1	hole position	–	9.0	–	+0.7/–0.5	mm
W_2	hold-down tape position	–	0.5	–	±0.2	mm
H_0	lead wire clinch height	–	16.5	–	±0.5	mm
H_1	component height	–	–	23.25	–	mm
L	length of snipped leads	–	–	11.0	–	mm
D_0	feed hole diameter	–	4.0	–	±0.2	mm
t	total tape thickness (t_1 = 0.3 to 0.6)	–	–	1.2	–	mm
F_1 F_2	lead-to-lead distance	–	2.54	–	+0.4/–0.2	mm
H_2	clinch height	–	–	3.0	–	mm
(p)	pull-out force	6.0	–	–	–	N



Dimensions in mm.

Fig.7 Dimensions of reel and ammopack.

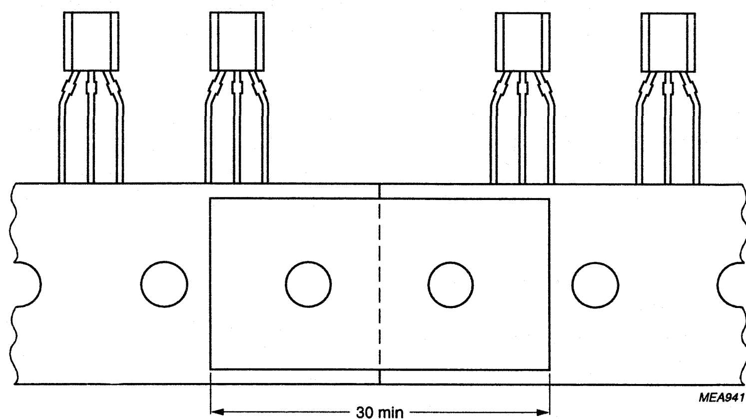


Fig.8 Splicing tape with jointing patch.

MOUNTING AND SOLDERING

Mounting methods

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting (SMD). Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly. Surface mounting techniques are complex and this chapter gives only a simplified overview of the subject.

Although many electronic components are available as surface mounting types, some are not and this often leads to the use of through-hole as well as surface mounting components on one substrate (a mixed print). The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

Reflow soldering

This is the preferred soldering technique for SOT23, SOT89, SOT143 and SOT223 components.

SOLDER PASTE

Most reflow soldering techniques utilize a paste that is a mixture of flux and solder. The solder paste is applied to the substrate before the components are placed. It is of sufficient viscosity to hold the components in place and, therefore, an application of adhesive is not required. Drying of the solder paste by preheating increases the viscosity and prevents any tendency for the components to become displaced during the soldering process. Preheating also minimizes thermal shock and drives off flux solvents.

Screen printing

This is the best high-volume production method of solder paste application. An emulsion-coated, fine mesh screen with apertures etched in the emulsion to coincide with the surfaces to be soldered is placed over the substrate. A squeegee is passed across the screen to force solder paste through the apertures and on to the substrate. The layer thickness of screened solder paste is usually between 150 and 200 μm.

Stencilling

In this method a stencil with etched holes to pass the paste is used. The thickness of the stencil determines the amount of amount of solder paste that is deposited on the substrate. This method is also suited to high-volume work.

Dispensing

A computer-controlled pressure syringe dispenses small doses of paste to where it is required. This method is mainly suitable for small production runs and laboratory use.

Pin transfer

A pin picks up a droplet of solder paste from a reservoir and transfers it to the surface of the substrate or component. A multi-pin arrangement with pins positioned to match the substrate is possible and this speeds up the process time.

REFLOW TECHNIQUES

Thermal conduction

The prepared substrates are carried on a conveyor belt, first through a preheating stage and then through a soldering stage. Heat is transferred to the substrate by conduction through the belt. Figure 9 shows a theoretical time/temperature relationship for thermal conduction reflow soldering. This method is particularly suited to thick film substrates and is often combined with infrared heating.

Infrared

An infrared oven has several heating elements giving a broad spectrum of infrared radiation, normally above and below a closed loop belt system. There are separate zones for preheating, soldering and cooling. Dwell time in the soldering zone is kept as short as possible to prevent damage to components and substrate. A typical heating profile is shown in Fig.10. This reflow method is often applied in double-sided prints.

Vapour phase

A substrate is immersed in the vapours of a suitable boiling liquid. The vapours transfer latent heat of condensation to the substrate and solder reflow takes place. Temperature is controlled precisely by the boiling point of the liquid at a given pressure. Some systems employ two vapour zones, one above the other. An elevator tray, suspended from a hoist mechanism passes the substrate vertically through the first vapour zone into the secondary soldering zone and then hoists it out of the vapour to be cooled. A theoretical time/temperature relationship for this method is shown in Fig.11.

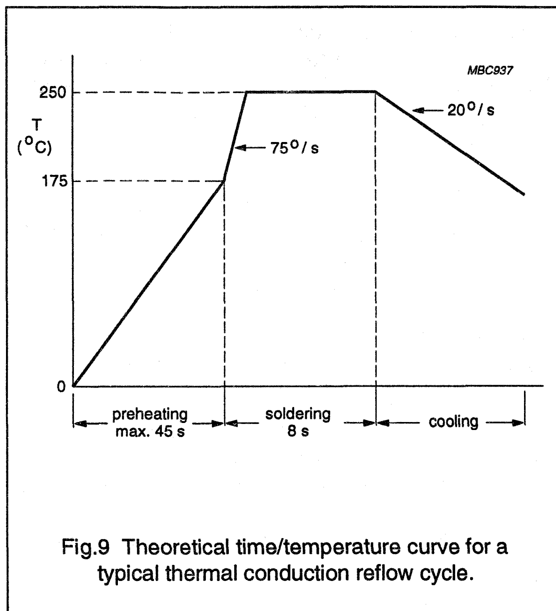


Fig.9 Theoretical time/temperature curve for a typical thermal conduction reflow cycle.

Wave soldering

This soldering technique can be applied to SOT23, SOT143 and SOT223 components but is not recommended for SOT89.

ADHESIVE APPLICATION

Since there are no connecting wires to retain them, leadless and short-leaded components are held in place with adhesive for wave soldering. A spot of adhesive is carefully placed between each SMD and the substrate. The adhesive is then heat-cured to withstand the forces of the soldering process, during which the components are fully immersed in solder. There are several methods of adhesive application.

Pin transfer method

A pin is used to transfer a droplet of adhesive from a reservoir to a precise position on the surface where it is required. The size of the droplet depends on pin diameter, depth to which the pin is dipped in the reservoir, rheology of the adhesive, and the temperature of adhesive and surrounds. The pin can be part of a pin

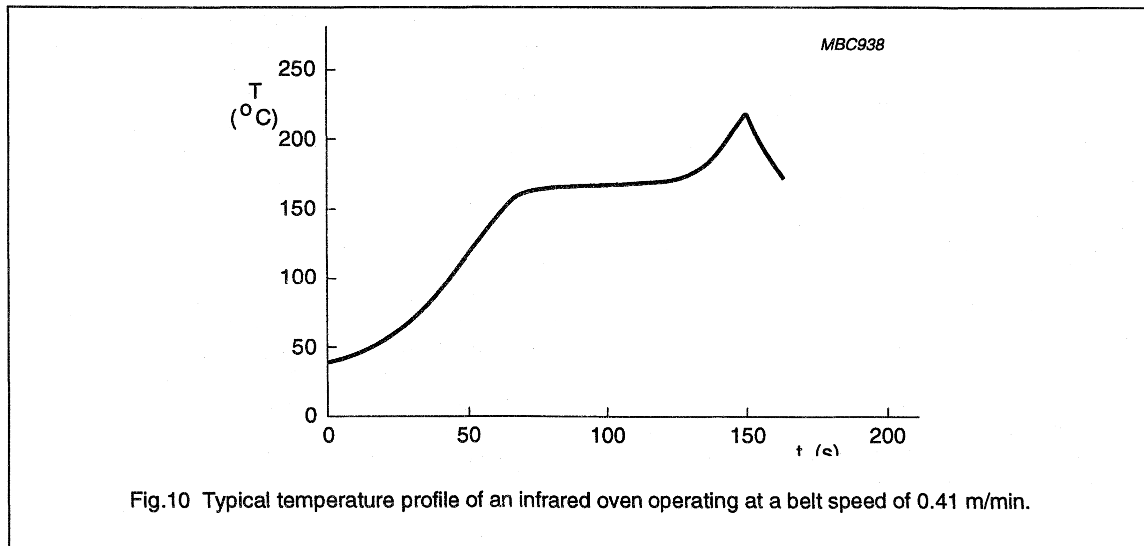


Fig.10 Typical temperature profile of an infrared oven operating at a belt speed of 0.41 m/min.

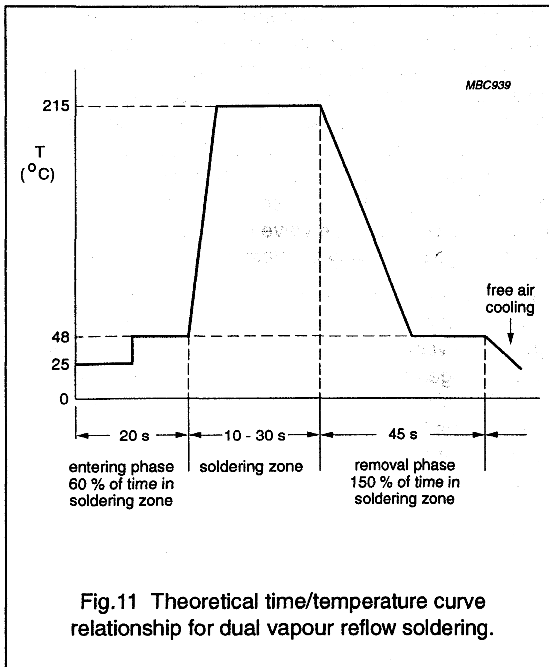


Fig.11 Theoretical time/temperature curve relationship for dual vapour reflow soldering.

array (bed of nails) that corresponds exactly with the required adhesive positions on the substrate. With this method, adhesive can be applied to the whole of one side of a substrate in one operation and is therefore suitable for high-volume production and can be used with pre-loaded mixed prints.

Alternatively, pins can be used to transfer adhesive to the components before they are placed on the substrate. This adds flexibility to production runs where variations in layout must be accommodated.

Screen printing method

A fine mesh screen is coated with emulsion except in the positions where the adhesive is required to pass. The screen is placed on the substrate and a squeegee passing across it forces adhesive through the uncoated parts of the screen. The amount of adhesive printed-through depends on the size of the uncoated screen areas, the thickness of the screen coating, the rheology of the adhesive and various machine parameters. With this method, the substrate must be flat and pre-loaded mixed prints cannot be accommodated.

Pressure syringe method

A computer-controlled syringe dispenses adhesive from an enclosed reservoir by means of pulses of compressed air. The adhesive dot size depends on the size of the syringe nozzle, the duration and pressure of the pulsed air and the viscosity of the adhesive. This method is most suited to low volume production. An advantage is the flexibility provided by computer programmability.

FLUXING

The quality of the soldered connections between components and substrate is critical for circuit performance and reliability. Flux promotes solderability of the connecting surfaces and is chosen for the following attributes:

- removal of surface oxides
- prevention of reoxidation
- transference of heat from source to joint area
- residue that is non-corrosive or, if residue is corrosive, should be easy to clean away after soldering
- ability to improve wettability (readiness of a metal surface to form an alloy at its interface with the solder) to ensure strong joints with low electrical resistance
- suitability for the desired method of flux application.

In wave soldering, liquified flux is usually applied as a foam, a spray or in a wave.

Foam

Flux foam is made by forcing low-pressure, water-free clean air through an aerator immersed in liquid flux. Fine bubbles of flux are directed onto the substrate/component surfaces where they burst and form a thin, even layer. The flux also penetrates any plated-through holes. The flux has to be chosen for its foaming capabilities.

Spray

Several methods of spray fluxing exist, the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate. The amount of flux deposited is controllable by the speed of the substrate passing through the spray, the speed of rotation of the drum and the density of the flux.

Wave

A wave fluxer creates a double flowing wave of liquid flux which adheres to the surface as the substrate passes through. Wave height control is essential and a soft wipe-off brush is usually incorporated to remove excess flux from the substrate.

PRE-HEATING

Pre-heating of the substrate and components is performed immediately before soldering. This reduces thermal shock as the substrate enters the soldering process, causes the flux to become more viscous and accelerates the chemical action of the flux and so speeds up the soldering action.

SOLDERING

Wave soldering is usually the best method to use when high throughput rates are required. The single-wave soldering principle (Fig.12) is the most straight forward method and can be used on simple substrates with two-terminal SMD components. More complex substrates with increased circuit density and closer spacing of conductors can pose the problems of nonwetting (dry joints) and solder bridging. Bridging can occur across the closely spaced leads of multi-leaded devices as well as across adjacent leads on neighbouring components. Nonwetting is usually caused by components with plastic bodies. The plastic is not wetted by solder and creates a depression in the solder wave, which is augmented by surface tension. This can cause a shadow behind the component and prevent solder from reaching the joint surfaces. A smooth laminar solder wave is required to avoid bridging and a high pressure wave is needed to completely cover the areas that are difficult to wet. These conflicting demands are difficult to attain in a single wave but dual wave techniques go a long way in overcoming the problem.

In a dual wave machine (Fig.13), the substrate first comes into contact with a turbulent wave which has a high vertical velocity. This ensures good solder contact with both edges of the components and prevents joints from being missed. The second smooth laminar wave completes the formation of the solder fillet, removes excess solder and prevents bridging. Figure 14 indicates the time/temperature relationship measured at the soldering site in dual wave soldering.

New methods of wave soldering are developing continually. For example, the Omega System is a single wave agitated by pulses, which combines the functions of smoothness and turbulence. In another, a lambda wave injects air bubbles in the final part of the wave. A further innovation is the hollow jet wave in which the solder wave flows in the opposite direction to the substrate.

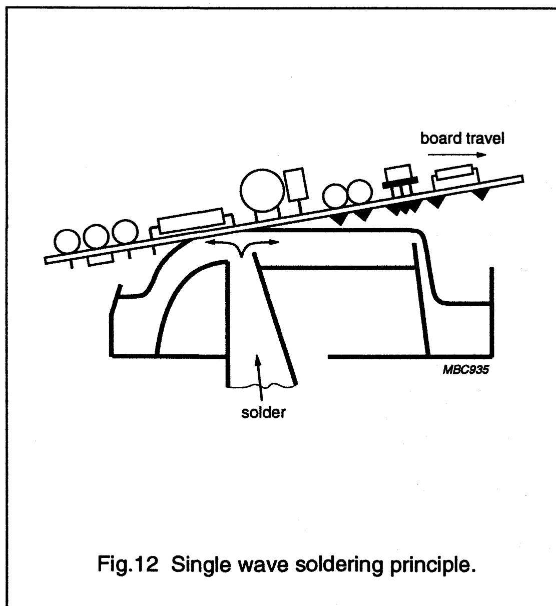


Fig.12 Single wave soldering principle.

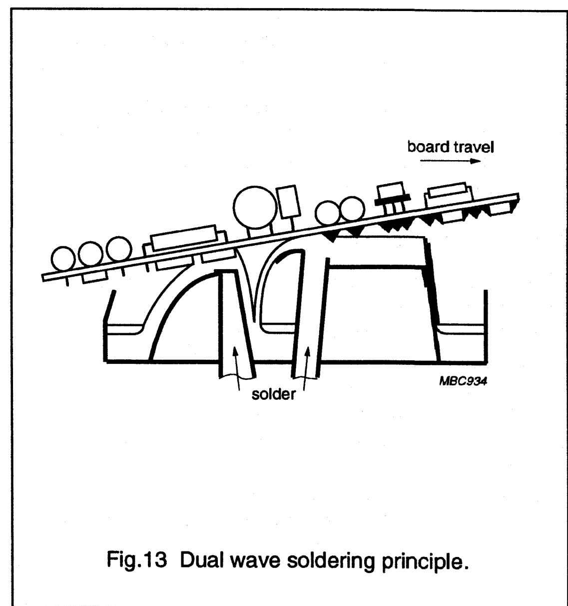


Fig.13 Dual wave soldering principle.

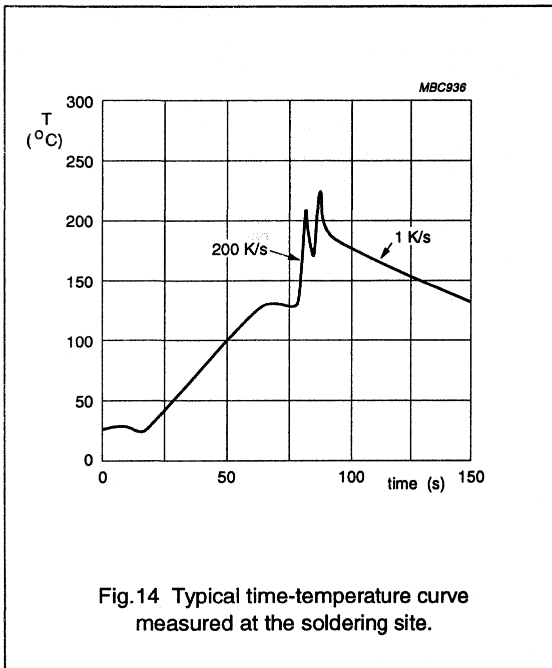


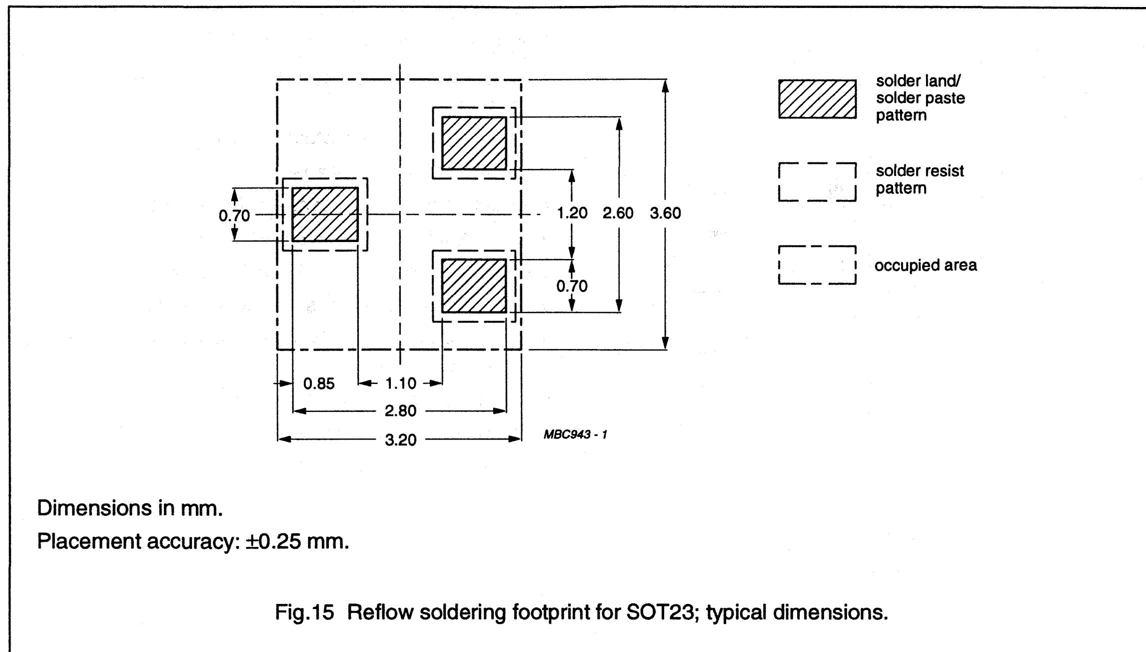
Fig.14 Typical time-temperature curve measured at the soldering site.

Footprint design

The footprint design of a component for surface mounting is influenced by many factors:

- features of the component, its dimensions and tolerances
- circuit board manufacturing processes
- desired component density
- minimum spacing between components
- circuit tracks under the component
- component orientation (if wave soldering)
- positional accuracy of solder resist to solder lands
- positional accuracy of solder paste to solder lands (if reflow soldering)
- component placement accuracy
- soldering process parameters
- solder joint reliability parameters.

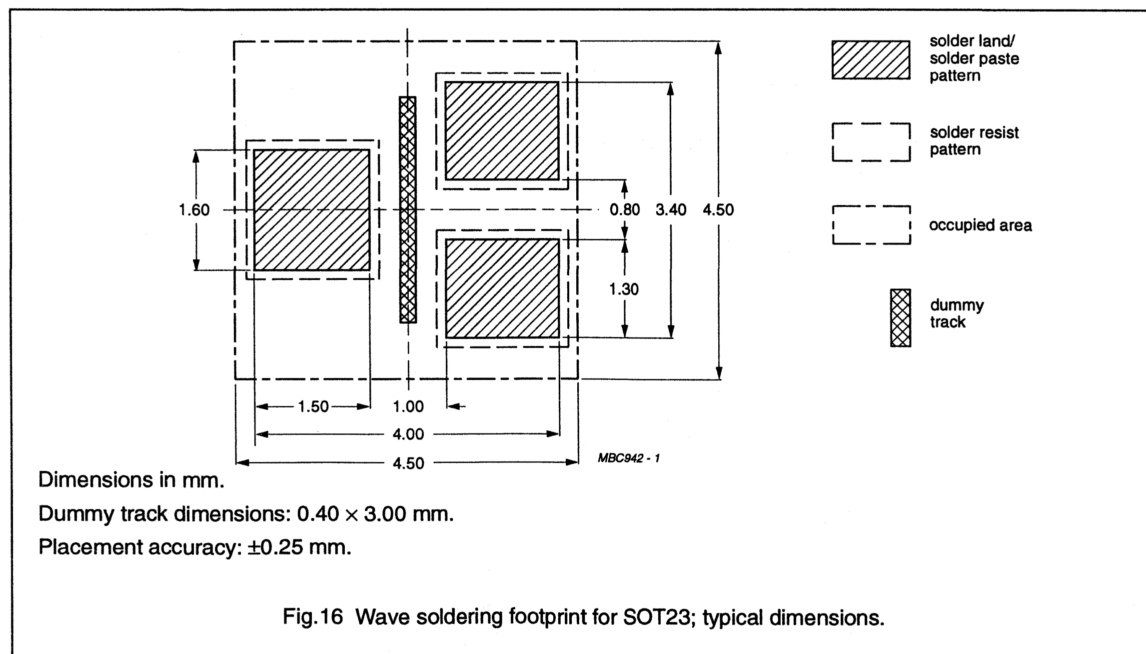
SOT23 FOOTPRINTS



Dimensions in mm.

Placement accuracy: ±0.25 mm.

Fig.15 Reflow soldering footprint for SOT23; typical dimensions.



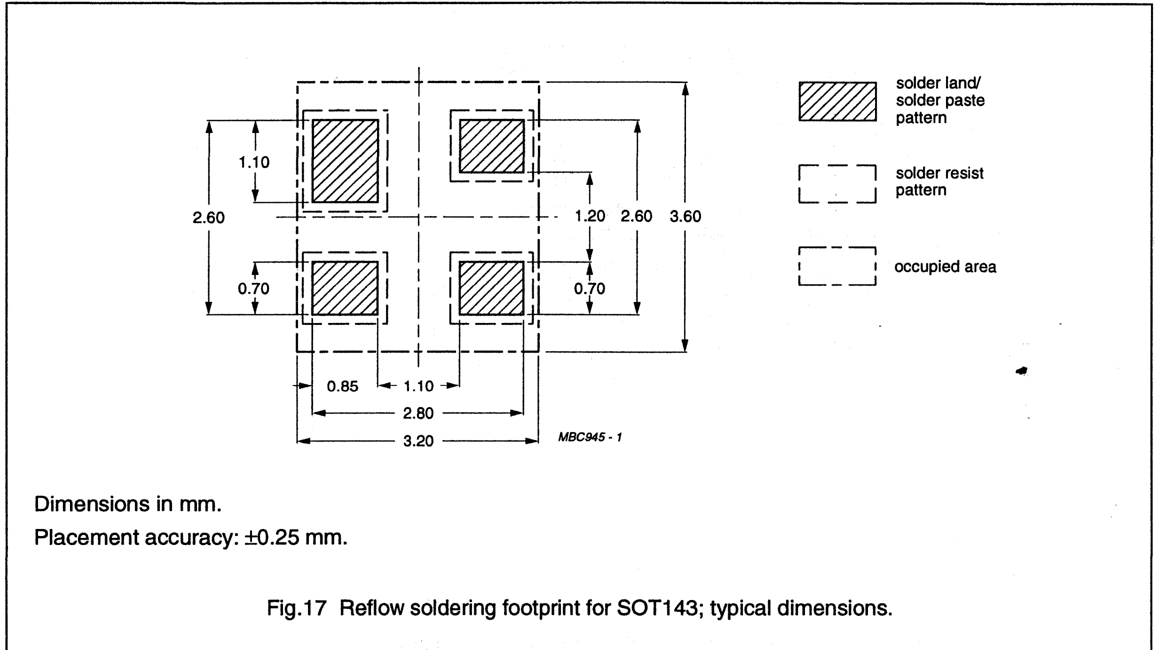
Dimensions in mm.

Dummy track dimensions: 0.40 × 3.00 mm.

Placement accuracy: ±0.25 mm.

Fig.16 Wave soldering footprint for SOT23; typical dimensions.

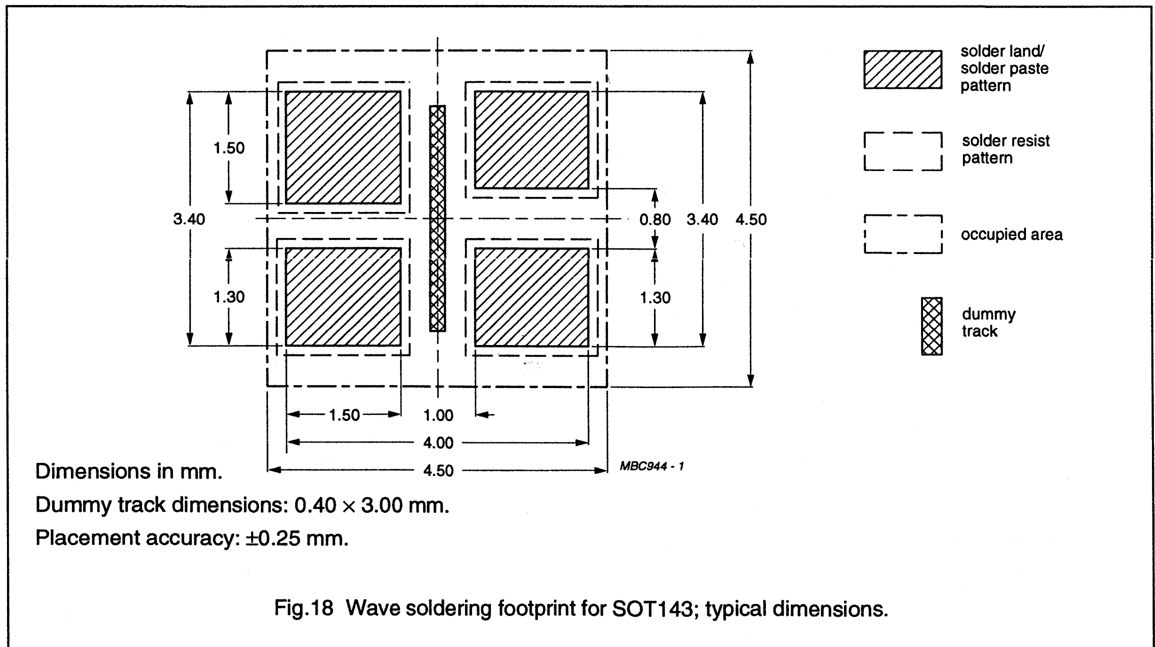
SOT143 FOOTPRINTS



Dimensions in mm.

Placement accuracy: ±0.25 mm.

Fig.17 Reflow soldering footprint for SOT143; typical dimensions.



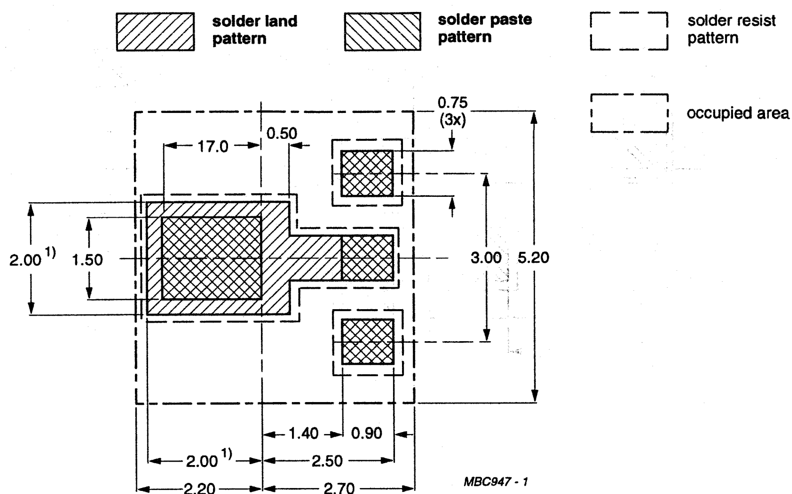
Dimensions in mm.

Dummy track dimensions: 0.40 × 3.00 mm.

Placement accuracy: ±0.25 mm.

Fig.18 Wave soldering footprint for SOT143; typical dimensions.

SOT89 FOOTPRINTS

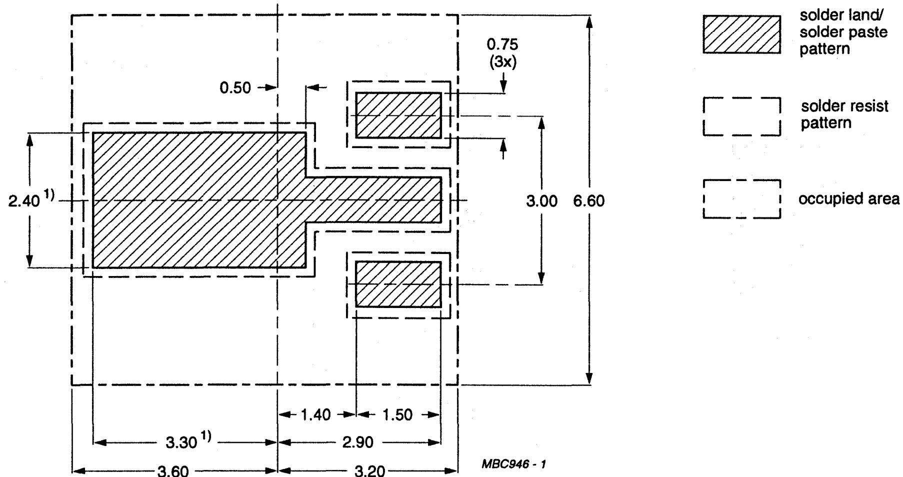


Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve the power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.19 Reflow soldering footprint for SOT89; typical dimensions.



We do not recommend SOT89 for wave soldering, SOT223 is preferred.

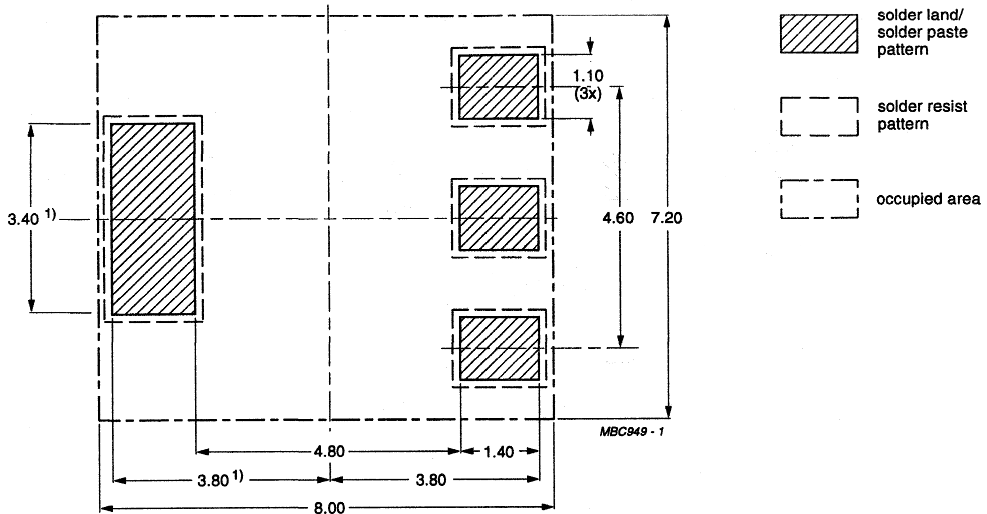
Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.20 Wave soldering footprint for SOT89; typical dimensions.

SOT223 footprints

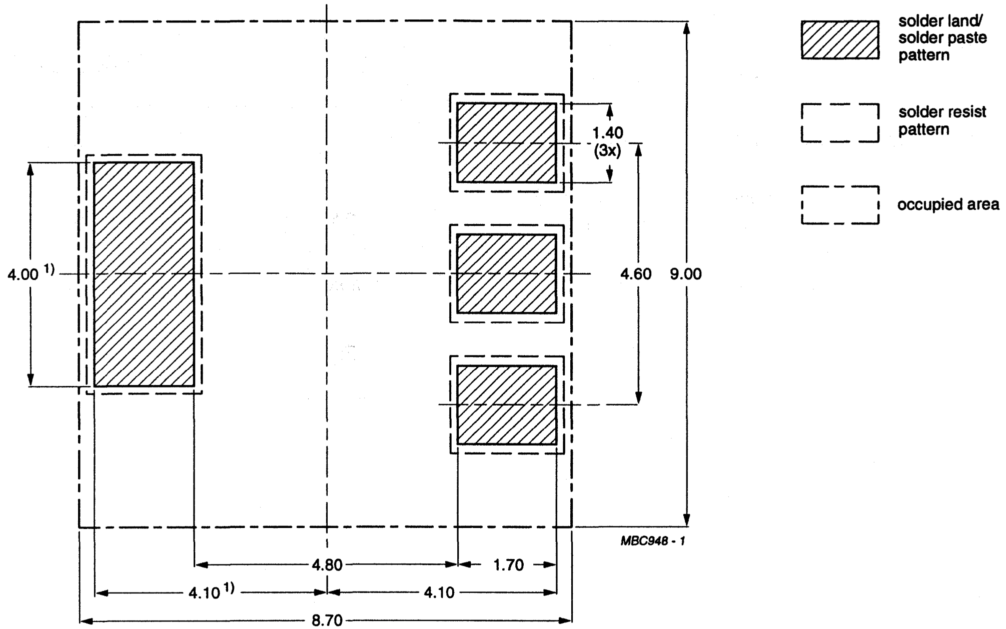


Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve the power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.21 Reflow soldering footprint for SOT223; typical dimensions.



Dimensions in mm.

Placement accuracy: ±0.25 mm.

1) To improve power dissipation the marked dimensions may be enlarged without changing the solder resist cut out of the footprint.

Fig.22 Wave soldering footprint for SOT223; typical dimensions.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

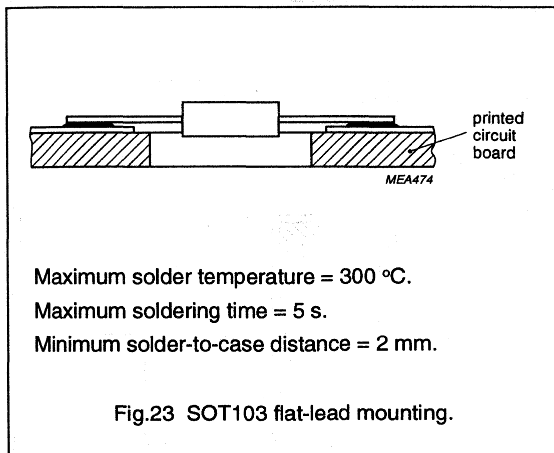
- hand-soldering is time-consuming and therefore expensive
- the component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- there is a risk of breaking the substrate and internal connections in the component could be damaged
- the component envelope could be damaged by the iron.

SOT103

Transistors in SOT103 envelopes may be mounted with leads flat, bent for surface mounting or bent for through-hole mounting.

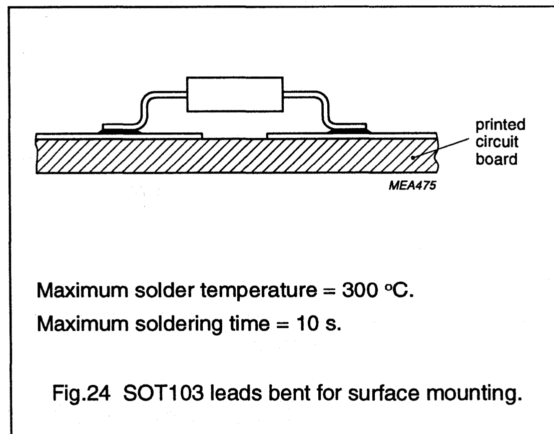
When soldering by hand and with the leads flat (Fig.23), avoid putting any force on the leads during or just after soldering. Solder the leads one at a time and not simultaneously. Proceed from one lead to the adjacent lead, not to the lead opposite. With the leads bent (Figs 24 and 25) all leads may be soldered simultaneously if desired.

SOT103 envelopes are suitable for dip or wave soldering. The maximum allowable temperature of the solder is 260 °C. Solder at this temperature must not be in contact with the joint for more than 5 s and the total contact time of successive solder waves must not exceed 5 s. The component may be mounted up to the lead projections but the temperature of the body must not exceed the specified storage temperature.



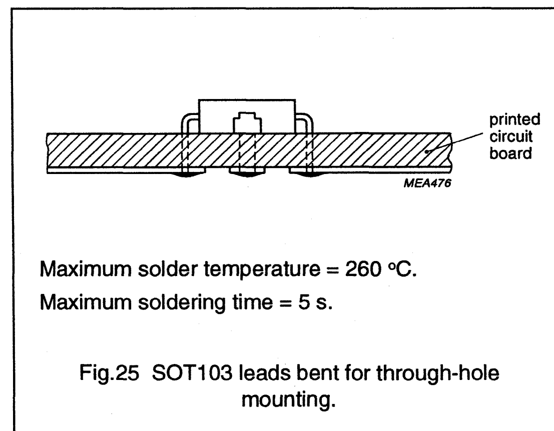
Maximum solder temperature = 300 °C.
Maximum soldering time = 5 s.
Minimum solder-to-case distance = 2 mm.

Fig.23 SOT103 flat-lead mounting.



Maximum solder temperature = 300 °C.
Maximum soldering time = 10 s.

Fig.24 SOT103 leads bent for surface mounting.



Maximum solder temperature = 260 °C.
Maximum soldering time = 5 s.

Fig.25 SOT103 leads bent for through-hole mounting.

THERMAL CONSIDERATIONS

Thermal resistance

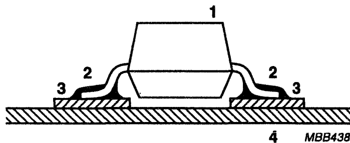
Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a substrate. Referring to Fig.26, heat conducts from its source (the junction) via the envelope leads and soldered connections to the substrate. Some heat radiates from the envelope into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The elements of thermal resistance shown in Fig.27 are defined as follows:

- $R_{th\ j\text{-}mb}$ thermal resistance from junction to mounting base
- $R_{th\ j\text{-}c}$ thermal resistance from junction to case
- $R_{th\ j\text{-}s}$ thermal resistance from junction to soldering point
- $R_{th\ s\text{-}a}$ thermal resistance from soldering point to ambient
- $R_{th\ c\text{-}a}$ thermal resistance from case to ambient ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$ are the same for most envelopes)
- $R_{th\ j\text{-}a}$ thermal resistance from junction to ambient.



Heat radiates from the envelope (1) to ambient.
Heat conducts via leads (2), solder joints (3) to the substrate (4).

Fig.26 Heat losses.

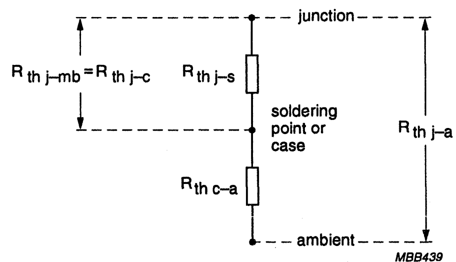


Fig.27 Representation of thermal resistance paths of a device mounted on a substrate or printed board.

The temperature at the junction depends on the ability of the envelope and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$$T_{j\,max} = T_{amb} + P_{tot\,max}(R_{th\,j\text{-}s} + R_{th\,s\text{-}a})$$
$$= T_{amb} + P_{tot\,max}(R_{th\,j\text{-}a})$$

where

$T_{j\,max}$ is the maximum junction temperature

T_{amb} is the ambient temperature

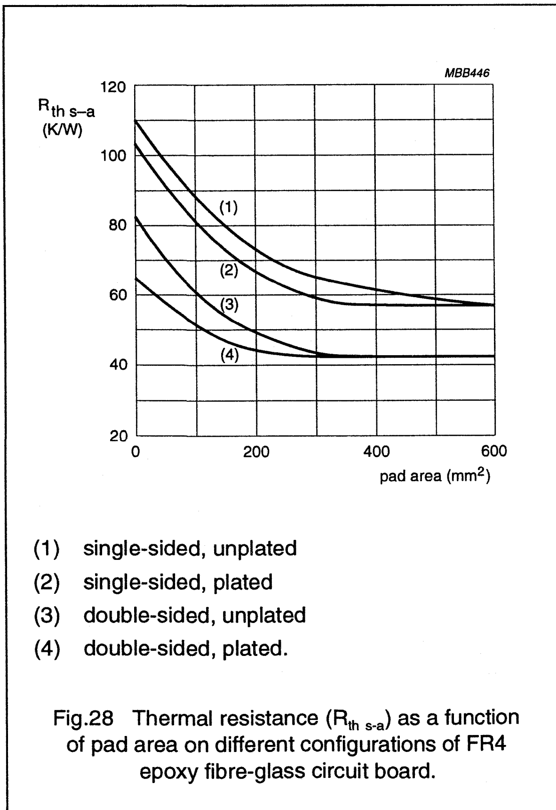
$P_{tot\,max}$ is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\,max}$, only T_{amb} and $R_{th\,s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\,s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\,j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the envelope construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\,max}$ and $R_{th\,j\text{-}s}$ or $R_{th\,j\text{-}c}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from $T_j = T_{case} + P_{tot} \times R_{th\,j\text{-}c}$ or, using the soldering point definition, from $T_j = T_{solder} + P_{tot} \times R_{th\,j\text{-}s}$.

Thermal resistance ($R_{th\,s\text{-}a}$ and $R_{th\,c\text{-}a}$)

The thermal resistance from soldering point to ambient and that from case to ambient depends on the shape and material of the tracks and substrate as illustrated in Figs 28 and 29. Standard mounting conditions to set the maximum power ratings of the various envelopes are shown in Figs 30 to 33. Each figure shows single-sided 35 µm copper-clad epoxy fibre-glass print, 1.5 mm thick, the tracks are fully solder-tinned and the shaded areas shown are copper.



(1) single-sided, unplated
(2) single-sided, plated
(3) double-sided, unplated
(4) double-sided, plated.

Fig.28 Thermal resistance ($R_{th\,s\text{-}a}$) as a function of pad area on different configurations of FR4 epoxy fibre-glass circuit board.

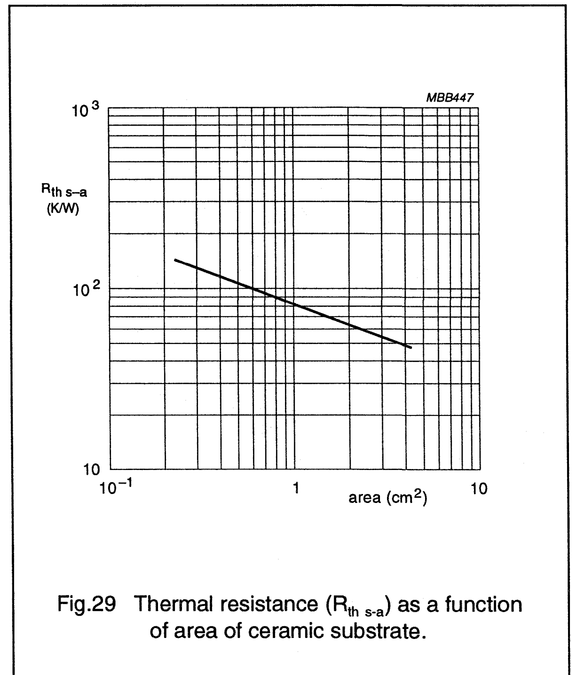
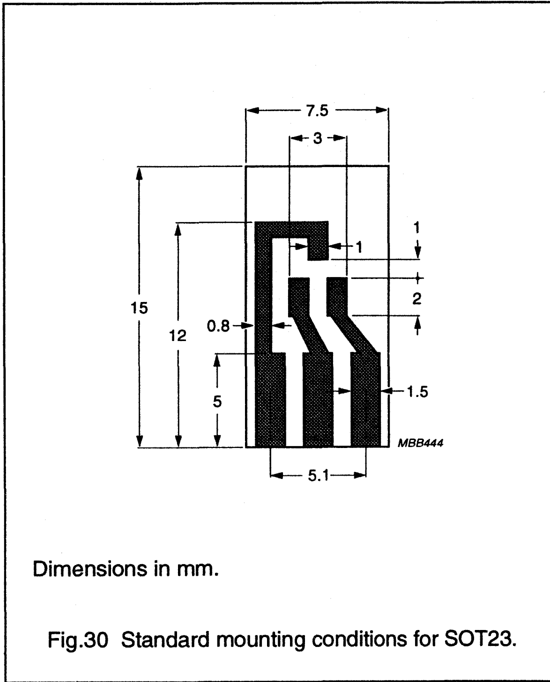
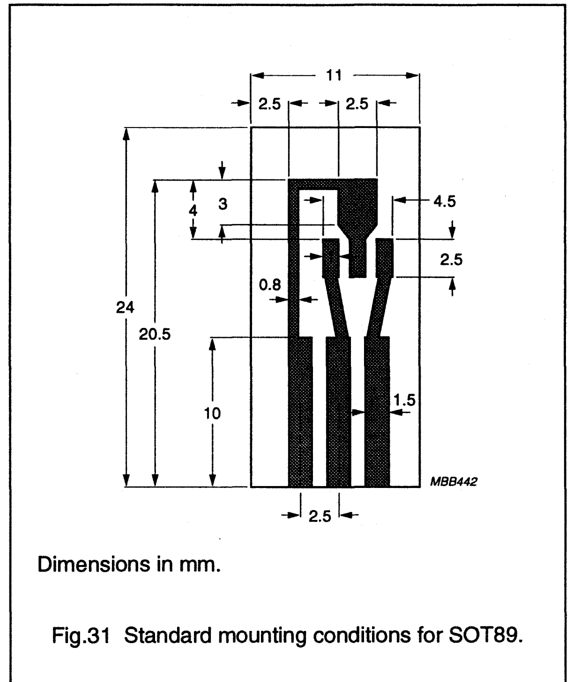


Fig.29 Thermal resistance ($R_{th\,s\text{-}a}$) as a function of area of ceramic substrate.



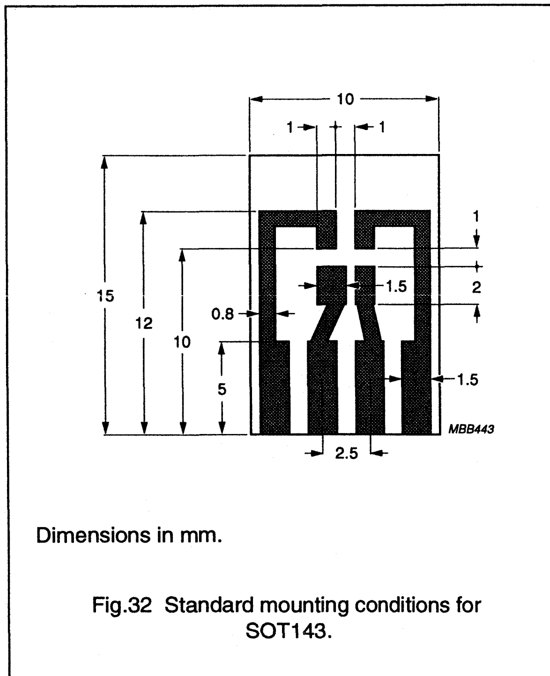
Dimensions in mm.

Fig.30 Standard mounting conditions for SOT23.



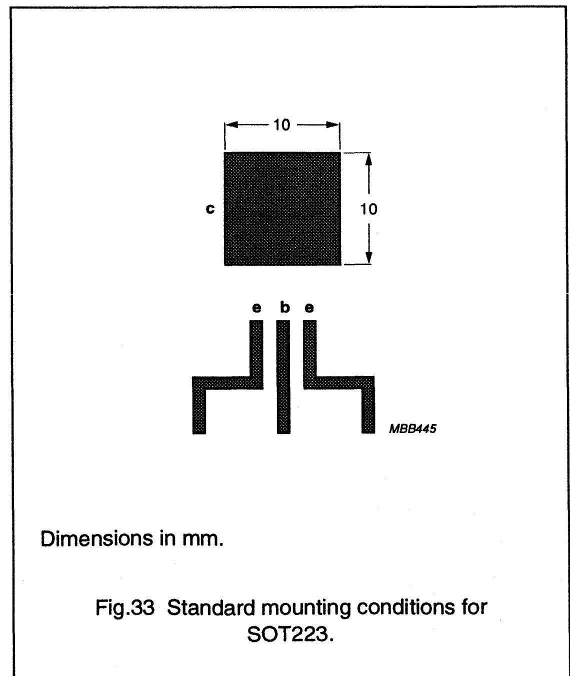
Dimensions in mm.

Fig.31 Standard mounting conditions for SOT89.



Dimensions in mm.

Fig.32 Standard mounting conditions for SOT143.



Dimensions in mm.

Fig.33 Standard mounting conditions for SOT223.

DEVICE DATA
in alphanumeric sequence

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

QUICK REFERENCE DATA

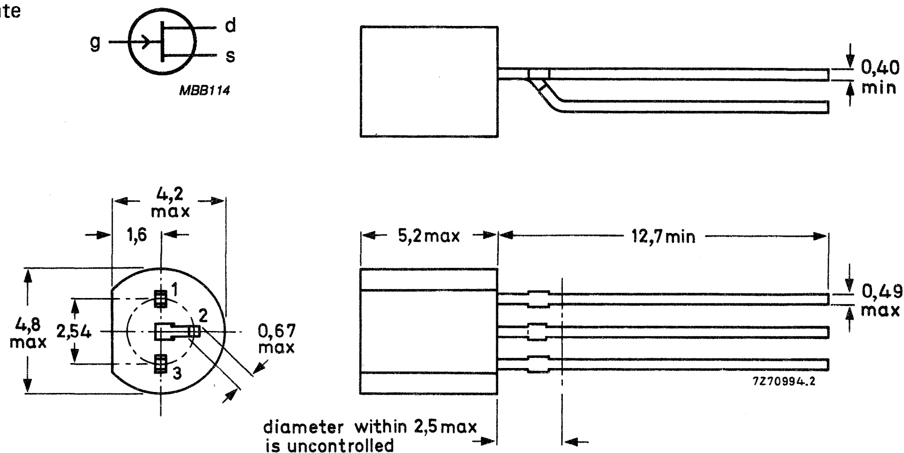
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	°C
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 12	mA
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$	typ.	3,5	mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0 f = 1 kHz; R_G = 1 MΩ	F	<	2	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Parameter	Conditions	Symbol		BC264A	B	C	D	Unit
Gate cut-off current	$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	<	5	5	5	5	nA
Drain current	$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	2,0	3,5	5,0	7,0	mA
			<	4,5	6,5	8,0	12,0	mA
Gate-source breakdown voltage	$-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source voltage	$I_D = 200\ \mu A$; $V_{DS} = 15$ V	$-V_{GS}$	>	0,4	0,4	0,4	0,4	V
	$I_D = 1,0$ mA; $V_{DS} = 15$ V	$-V_{GS}$	>	0,2	–	–	–	V
			<	1,2	–	–	–	V
	$I_D = 1,5$ mA; $V_{DS} = 15$ V	$-V_{GS}$	>	–	0,4	–	–	V
			<	–	1,4	–	–	V
	$I_D = 2,5$ mA; $V_{DS} = 15$ V	$-V_{GS}$	>	–	–	0,5	–	V
			<	–	–	1,5	–	V
	$I_D = 3,5$ mA; $V_{DS} = 15$ V	$-V_{GS}$	>	–	–	–	0,6	V
			<	–	–	–	1,6	V
Gate-source cut-off voltage	$I_D = 10$ nA ; $V_{DS} = 15$ V	$-V_{(P)GS}$	>	0,5	0,5	0,5	0,5	V
y-parameters at $T_{amb} = 25\ ^oC$; $V_{DS} = 15$ V; $V_{GS} = 0$; f = 1 kHz	Transfer admittance	$\lvert y_{fs} \rvert$	>	2,5	3,0	3,5	4,0	mS

$V_{DS} = 15$ V; $-V_{GS} = 1$ V; f = 1 MHz

Parameter	Symbol		Value	Unit
Input capacitance	C_{is}	typ.	4,0	pF
Feedback capacitance	C_{rs}	typ.	1,2	pF
Output capacitance	C_{os}	typ.	1,6	pF
Noise figure at f = 1 kHz; $R_G = 1\ M\Omega$; $V_{DS} = 15$ V; $V_{GS} = 0$; $T_{amb} = 25\ ^oC$	F	typ.	0,5	dB
		<	2	dB
Equivalent noise voltage at $T_{amb} = 25\ ^oC$; $V_{DS} = 15$ V; $V_{GS} = 0$; f = 10 Hz	$V_n / \sqrt{B}$	typ.	40	$nV/\sqrt{Hz}$

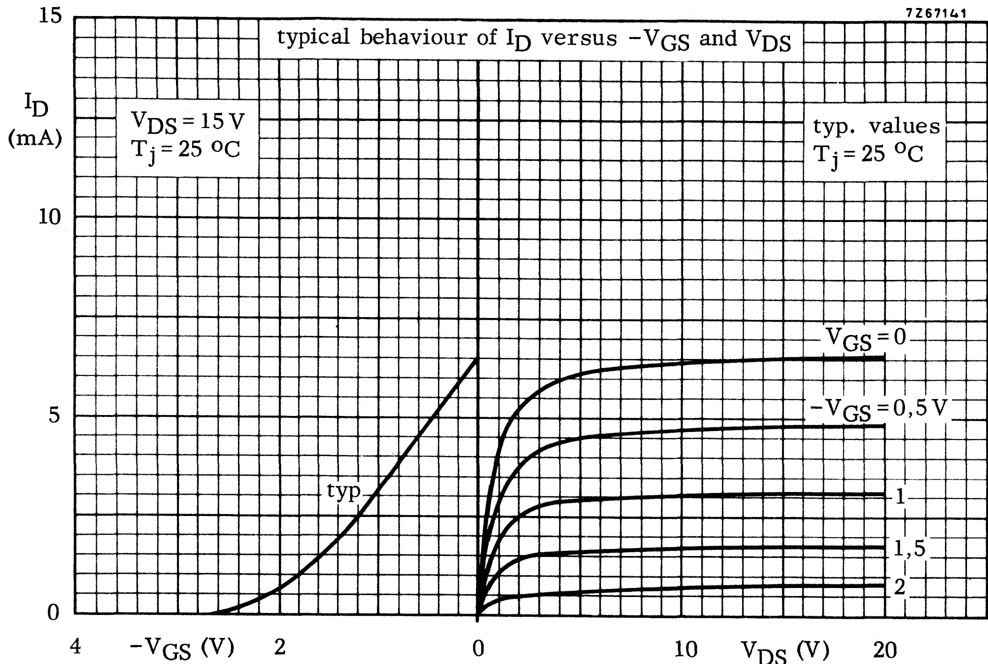


Fig. 2

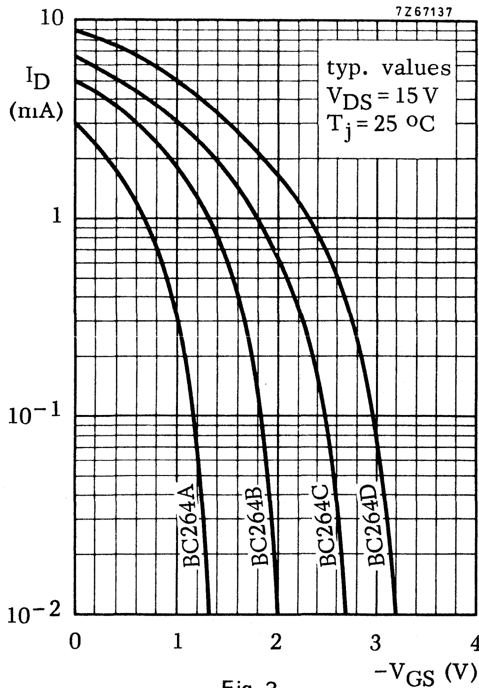


Fig. 3

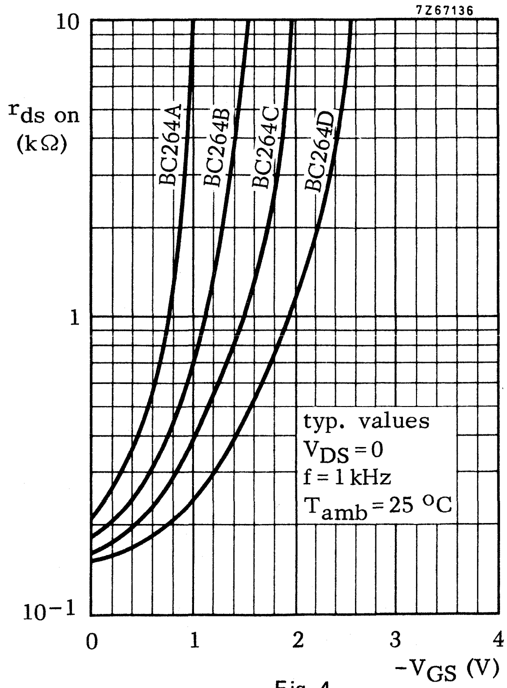


Fig. 4

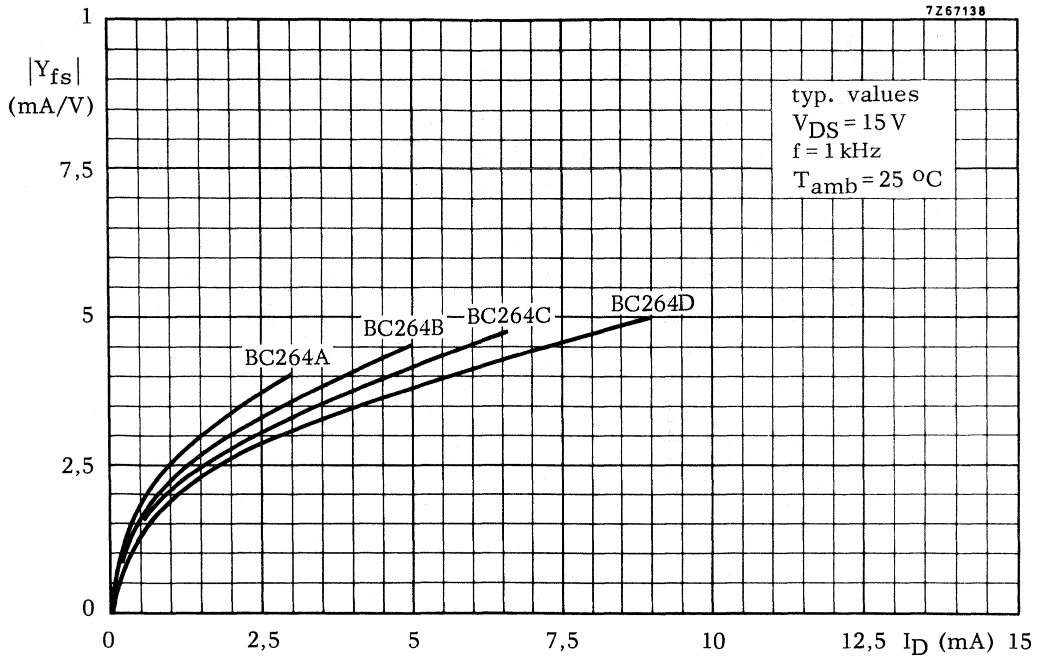


Fig. 5

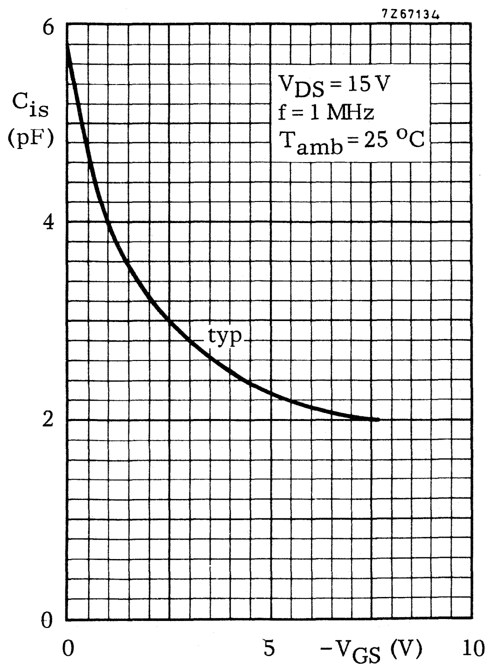


Fig. 6

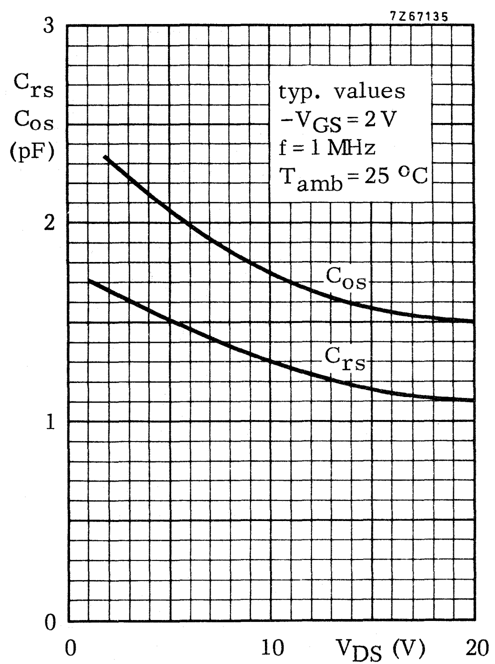


Fig. 7

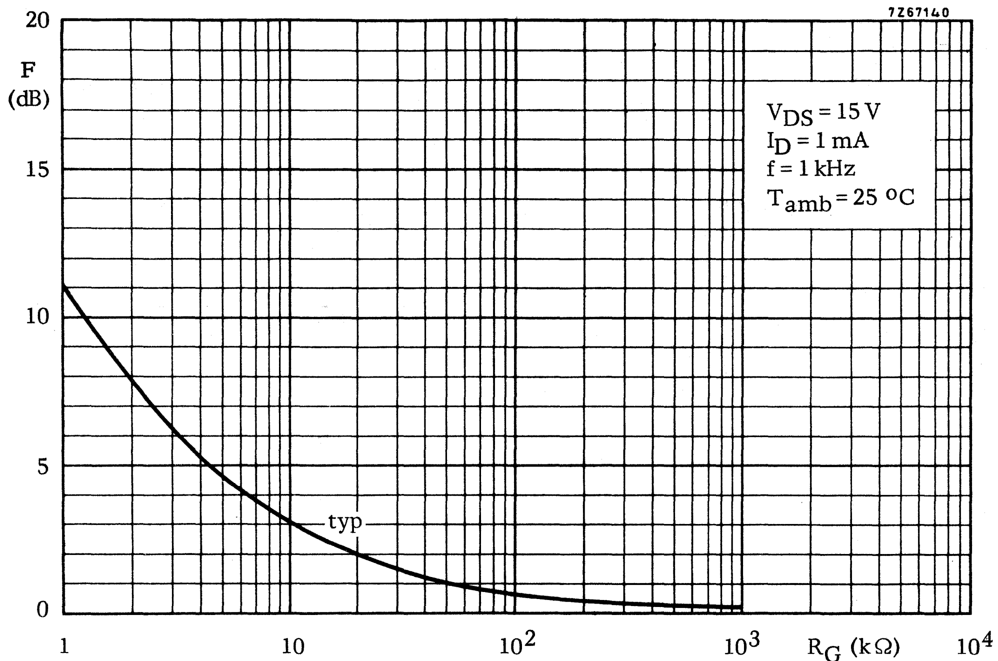


Fig. 8

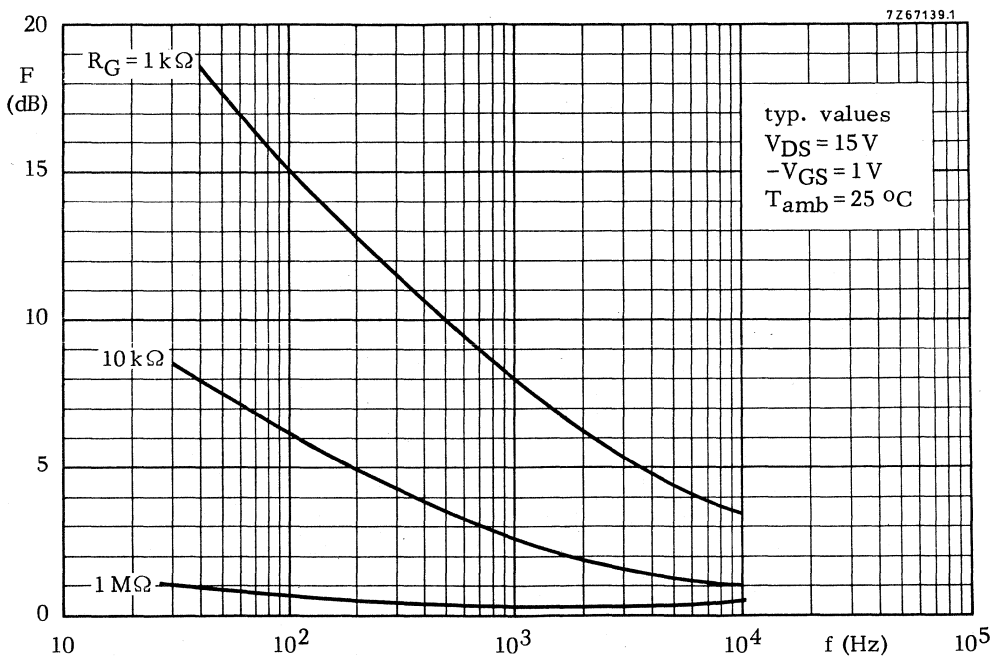


Fig. 9

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

QUICK REFERENCE DATA

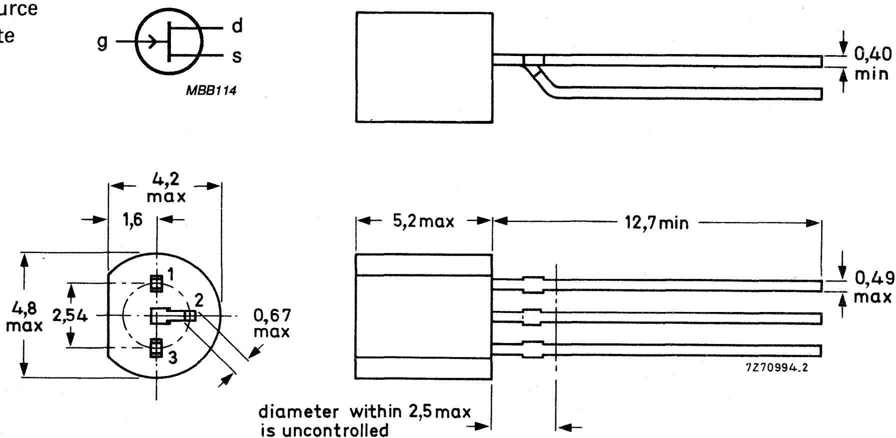
Drain-source voltage	$\pm V_{DS}$		max.			30	V
Gate-source voltage (open drain)	$-V_{GSO}$		max.			30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}		max.			300	mW
			BF245A/0	A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	0,5	2,0	6	12	mA
		<	2,1	6,5	15	25	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$		0,25 to 8,0				V
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}		typ.			1,1	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\lvert y_{fs} \rvert$		3,0 to 6,5				mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	25 mA
Gate current	I_G	max.	10 mA
Power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BF245A	B	C	
Gate cut-off current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	5	5	5	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	<	0,5	0,5	0,5	μA
Drain current 2)						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	>	2	6,0	12	mA
		<	6,5	15,0	25	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	30	30	V
Gate-source voltage						
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)	>	0,4	1,6	3,2	V
		<	2,2	3,8	7,5	V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leq$ 0,02.

3) BF245A/0: I_{DSS} = 0,5 to 2,1 mA; $-V_{GS}$ = 0,2 to 1,0 V
BF245A/1: I_{DSS} = 1,9 to 3,0 mA; $-V_{GS}$ = 0,4 to 1,0 V
BF245A/2: I_{DSS} = 3,0 to 4,5 mA; $-V_{GS}$ = 0,7 to 1,4 V
BF245A/3: I_{DSS} = 4,5 to 6,5 mA; $-V_{GS}$ = 1,1 to 2,2 V.

Gate-source cut-off voltage			
I_D = 10 nA; V_{DS} = 15 V		$-V_{(P)GS}$	0,25 to 8,0 V
y-parameters at T_{amb} = 25 °C (common source)			
V_{DS} = 15 V; V_{GS} = 0			
f = 1 kHz	Transfer admittance	$\|y_{fs}\|$	3,0 to 6,5 mS
	Output admittance	$\|y_{os}\|$	typ. 25 μS
f = 200 MHz	Input conductance	g_{is}	typ. 250 μS
	Reverse transfer admittance	$\|y_{rs}\|$	typ. 1,4 mS
	Transfer admittance	$\|y_{fs}\|$	typ. 6 mS
	Output conductance	g_{os}	typ. 40 μS
V_{DS} = 20 V; $-V_{GS}$ = 1 V			
f = 1 MHz	Input capacitance	C_{is}	typ. 4,0 pF
	Feedback capacitance	C_{rs}	typ. 1,1 pF
	Output capacitance	C_{os}	typ. 1,6 pF
Cut-off frequency *			
V_{DS} = 15 V; V_{GS} = 0		f_{gfs}	typ. 700 MHz
Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)			
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise		F	typ. 1,5 dB

* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

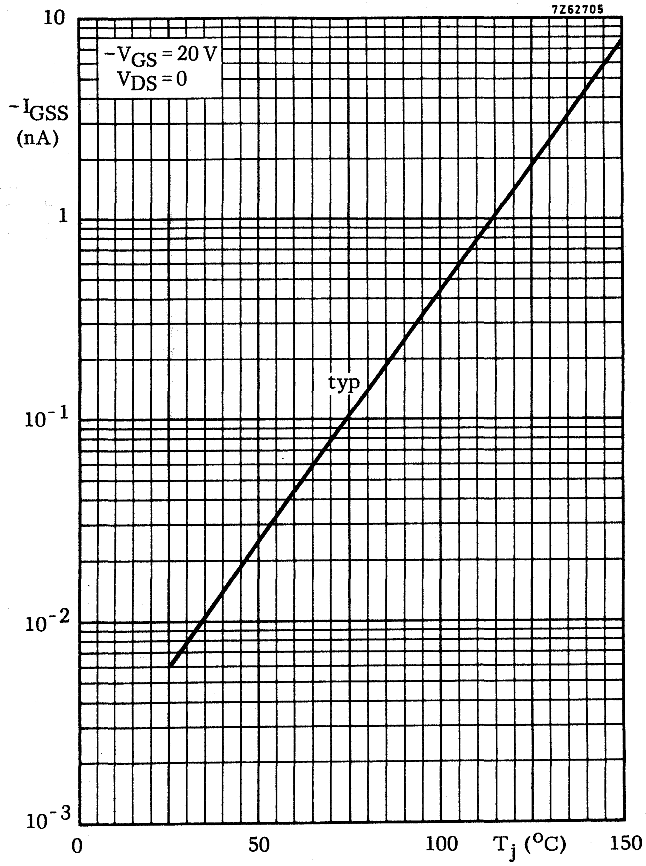


Fig. 2

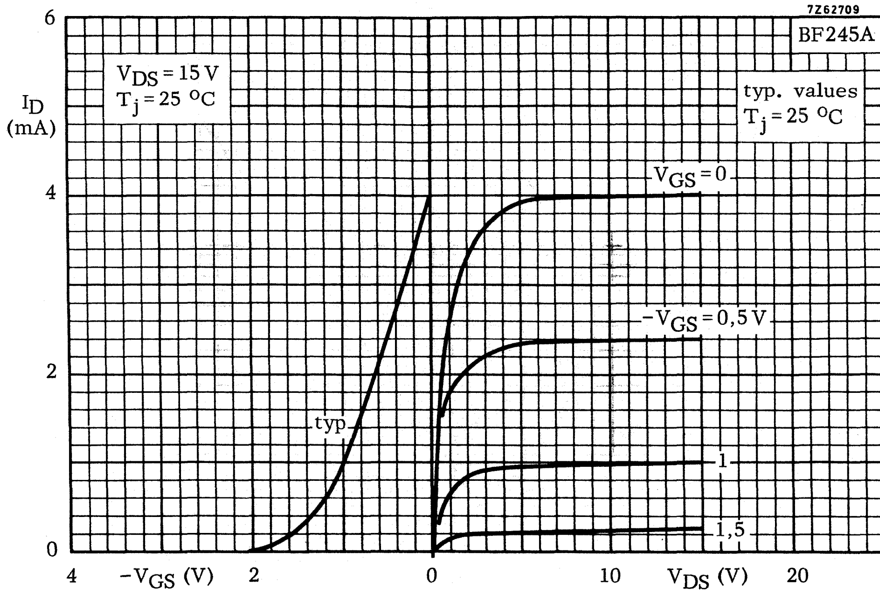


Fig. 3

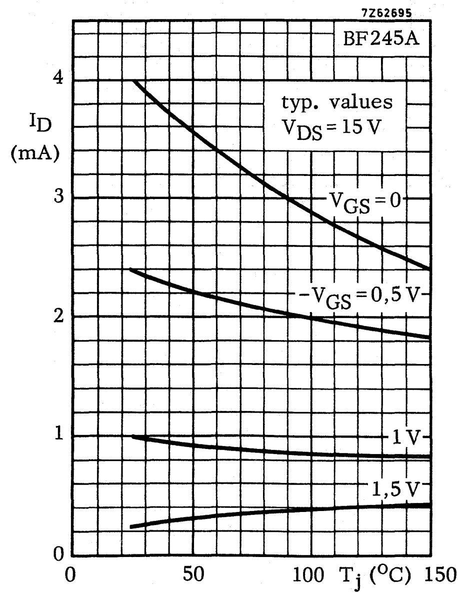


Fig. 4

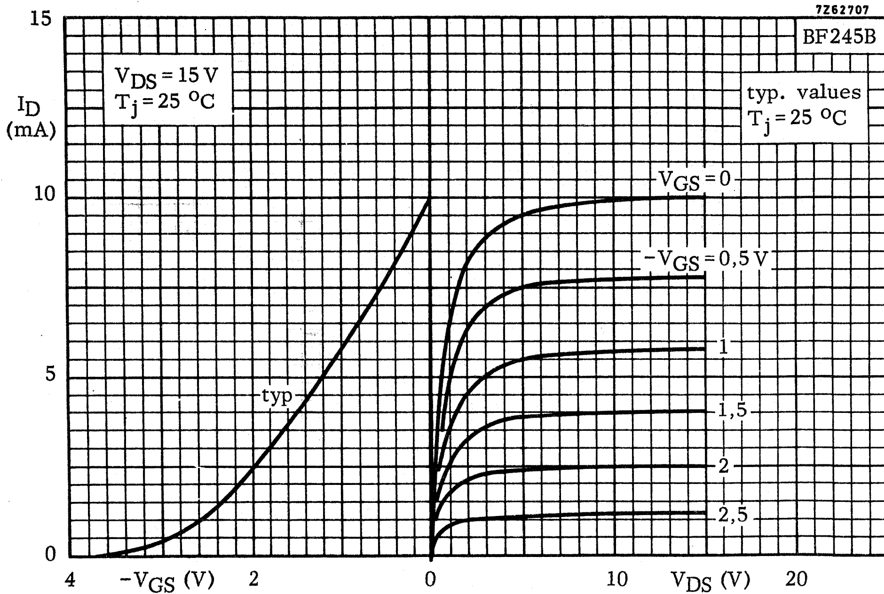


Fig. 5

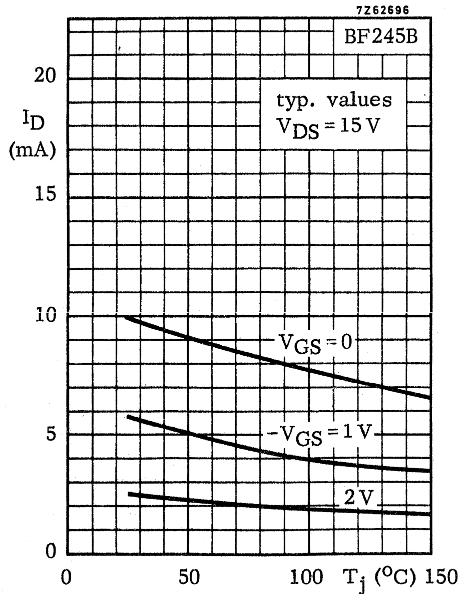


Fig. 6

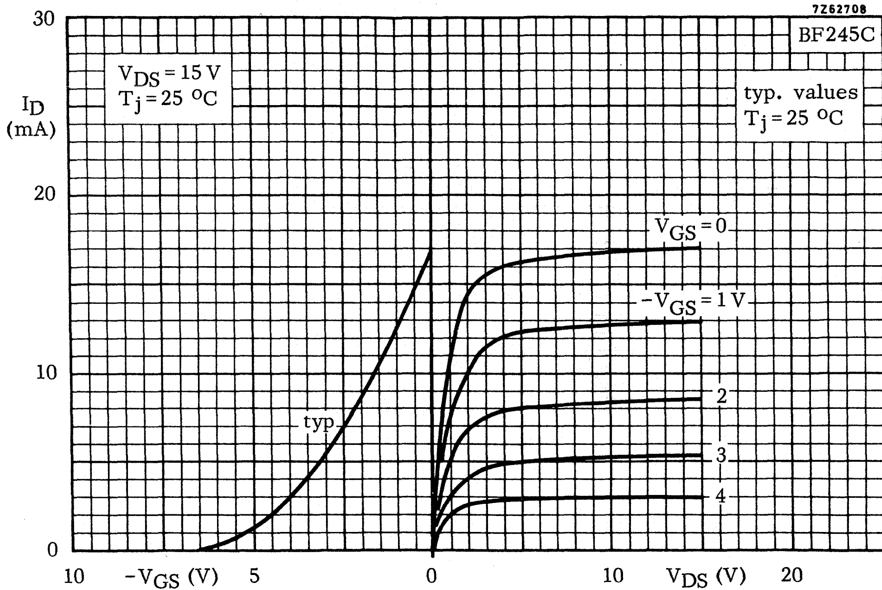


Fig. 7

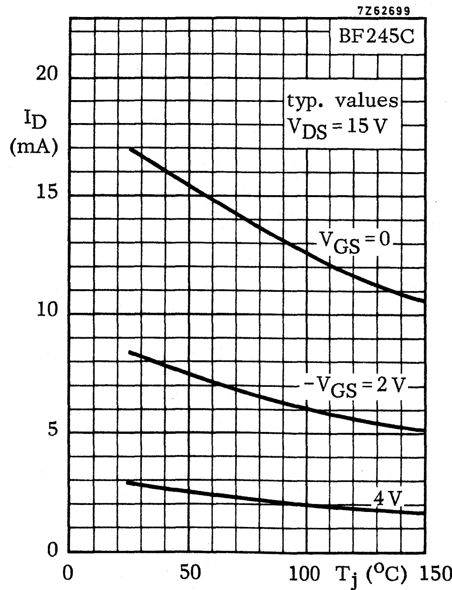


Fig. 8

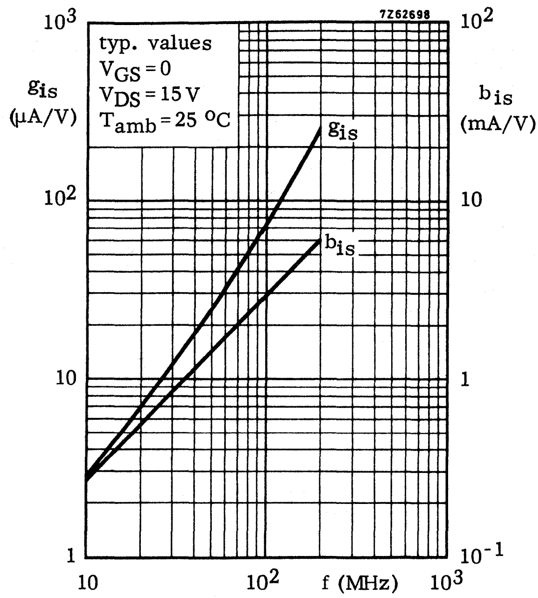


Fig. 9

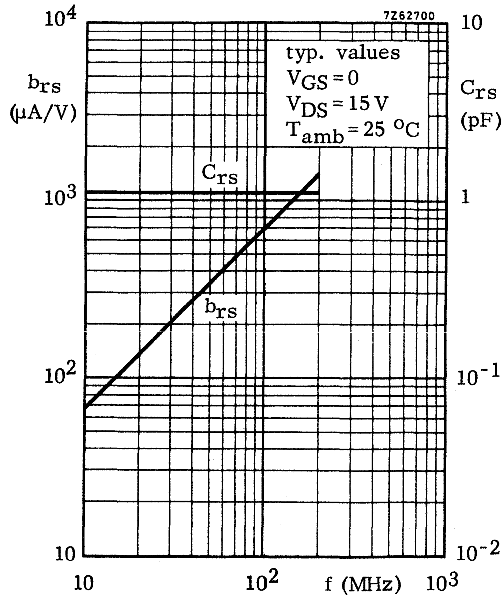


Fig. 10

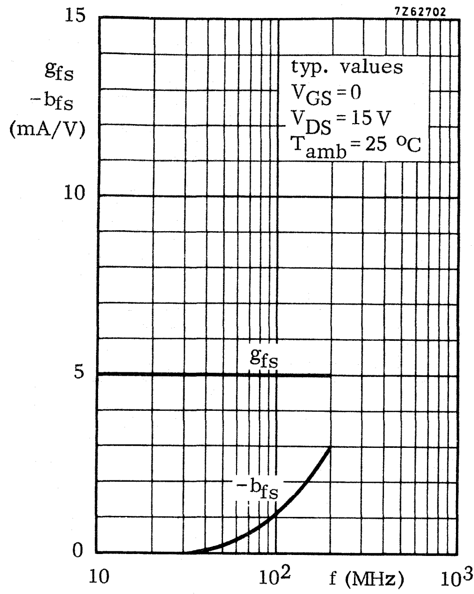


Fig. 11

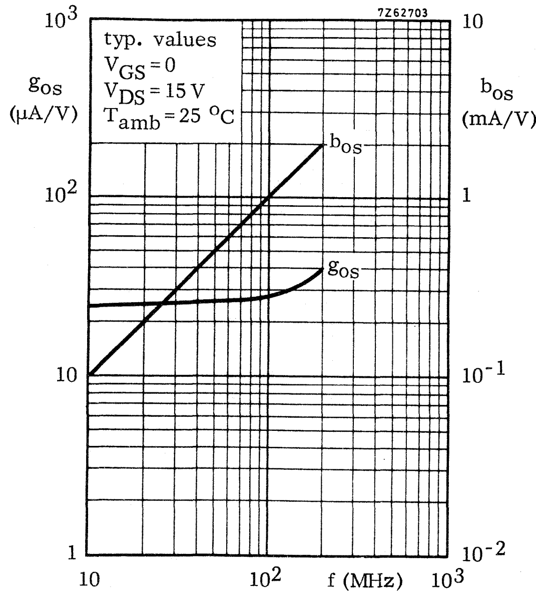


Fig. 12

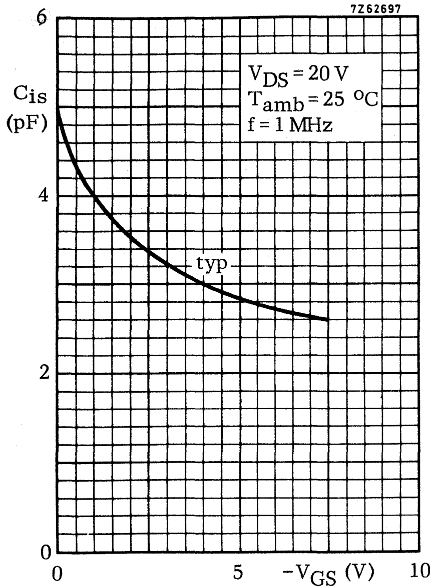


Fig. 13

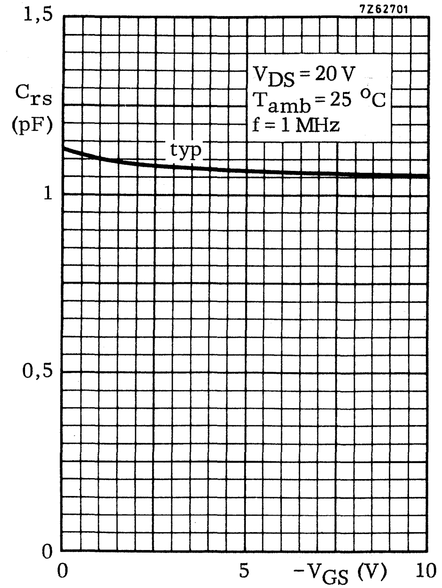


Fig. 14

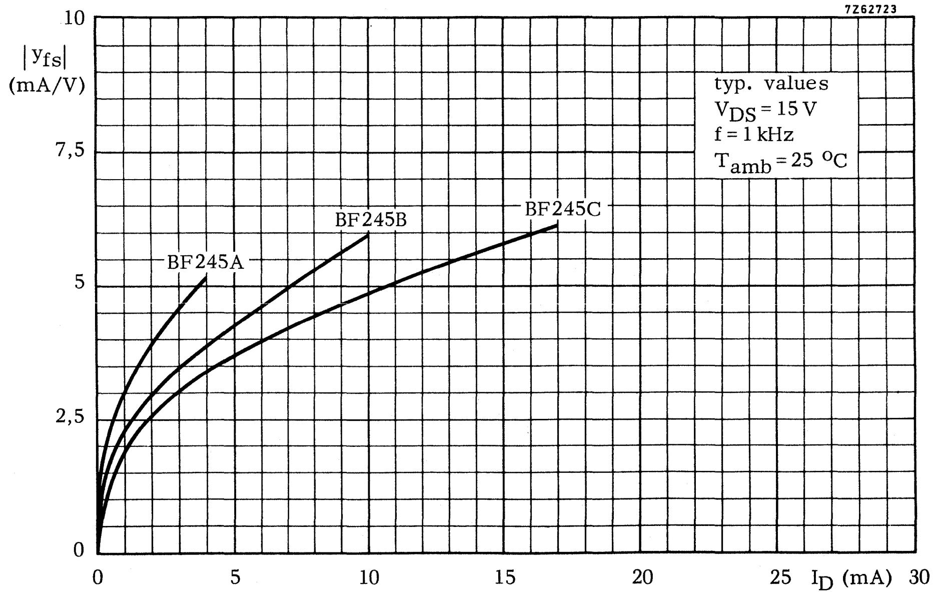


Fig. 15

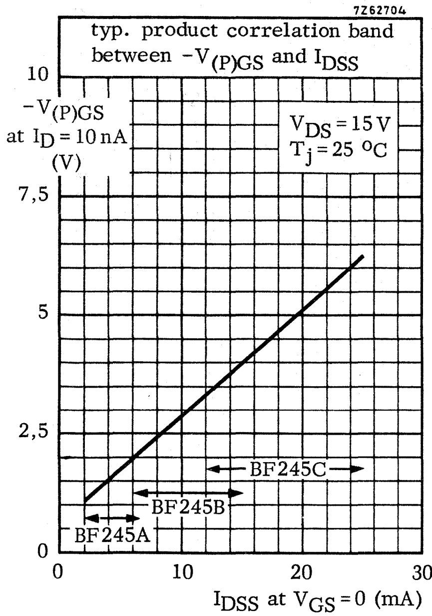


Fig. 16

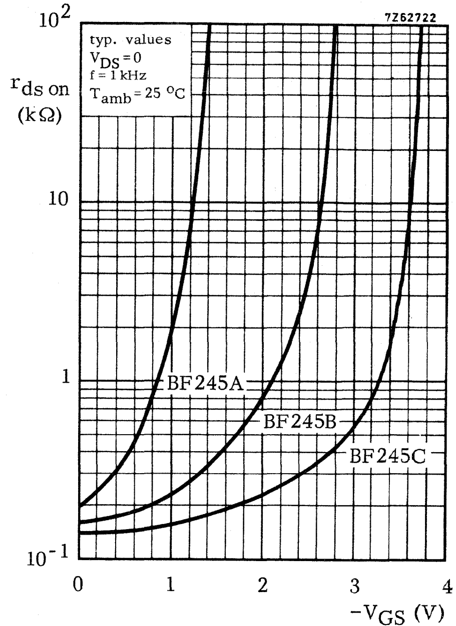


Fig. 17

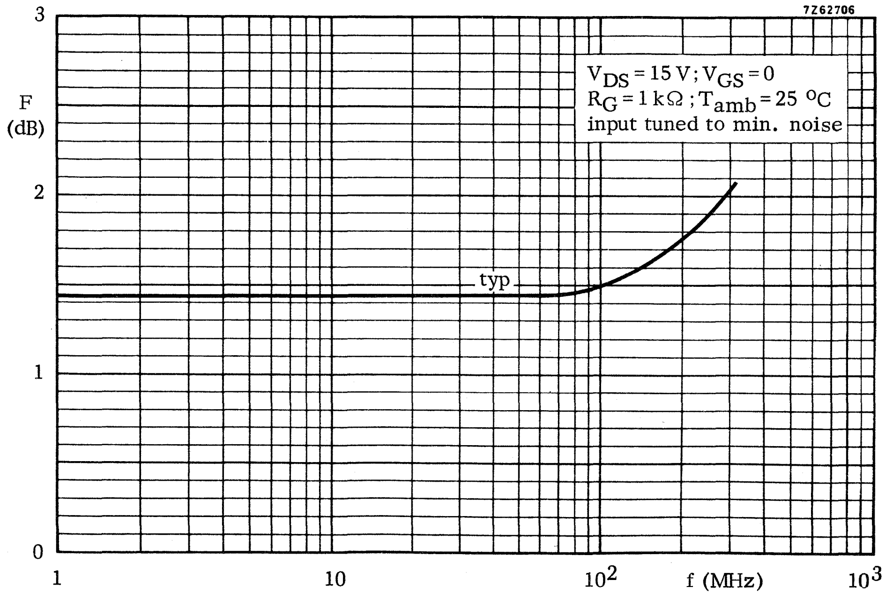


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for VHF and UHF amplifiers, mixers and general purpose switching.

QUICK REFERENCE DATA

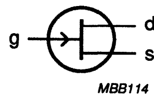
Parameter	Symbol		A	B	C	Unit
Drain-source voltage	$\pm V_{DS}$	max.			25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.			250	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$				0.6 to 14.5	V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V	C_{rs}	typ.			3.5	pF
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	min.			8	mS

MECHANICAL DATA

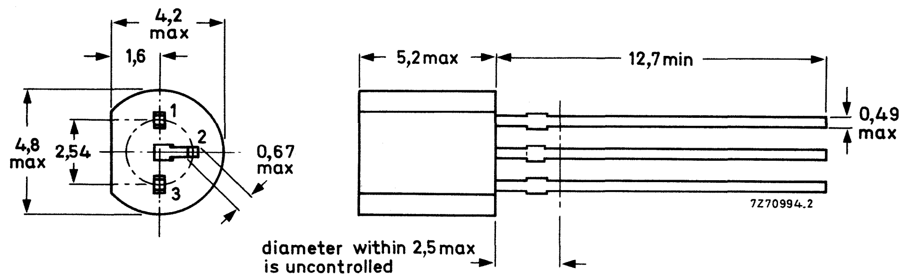
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning (BF246):
1 = drain
2 = gate
3 = source



Pinning (BF247):
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate current	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W

CHARACTERISTICS

T_{amb} = 25 °C

			A	B	C	
Gate cut-off current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	5	5	5	nA
Drain current* V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	25	25	25	V
Gate-source voltage I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	min.	1.5	3.0	5.5	V
		max.	4.0	7.0	12.0	V

Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$		0.6 to 14.5 V
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	min.	8 mS
		typ.	17 mS
Capacitances at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V			
feed-back capacitance	C_{rs}	typ.	3.5 pF
input capacitance	C_{is}	typ.	11 pF
output capacitance	C_{os}	typ.	5 pF
Cut-off frequency** V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	450 MHz

* Measured under pulse conditions; t_p = 300 μs; $\delta \leqslant 0.02$.

** The frequency at which g_{fs} is 0.7 of its value at 1 kHz.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA

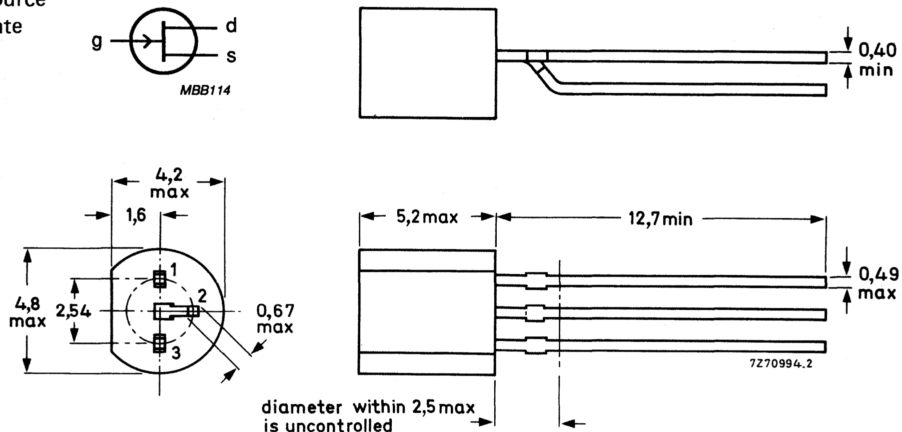
Drain-source voltage	$\pm V_{DS}$		max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$		max.	30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}		max.	300	mW
		BF256A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 3 < 7	6 13	11 18	mA mA
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}		typ.	0,7	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\|y_{fs}\|$		>	4,5	mS
Power gain at f = 800 MHz V_{DS} = 15 V; R_S = 47 Ω	G_p		typ.	11	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning;
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Gate current	I_G	max.	10 mA
Total power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W 1)

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current
$-V_{GS}$ = 20 V; V_{DS} = 0 — $-I_{GSS}$ < 5 nA

Drain current 2)
V_{DS} = 15 V; V_{GS} = 0 — I_{DSS} 3)

		BF256A	B	C	
I_{DSS} 3)	>	3	6	11	mA
	<	7	13	18	mA

Gate-source breakdown voltage
$-I_G$ = 1 μA; V_{DS} = 0 — $-V_{(BR)GSS}$ > 30 V

Gate-source voltage
I_D = 200 μA; V_{DS} = 15 V — $-V_{GS}$ 3) 0,5 to 7,5 V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0,02$.

3) BF256B/1: I_{DSS} = 6 to 8 mA; $-V_{GS}$ = 1,4 to 2,6 V.

y-parameters (common source)			
Transistor admittance at f = 1 kHz			
V_{DS} = 15 V; V_{GS} = 0	$\lvert y_{fs} \rvert$	>	4,5 mS 1)
		typ.	5 mS 1)
Output capacitance at f = 1 MHz			
V_{DS} = 20 V; V_{GS} = 0	C_{os}	typ.	1,2 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 20 V; $-V_{GS}$ = 1 V	C_{rs}	typ.	0,7 pF
Cut-off frequency			
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	1 GHz 2)
Noise figure at f = 800 MHz			
V_{DS} = 10 V; R_S = 47 Ω	F	typ.	7,5 dB
Power gain at f = 800 MHz			
V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11 dB

1) Measured under pulse conditions: $t_p = 300\ \mu s$; $\delta \leqslant 0{,}02$.

2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

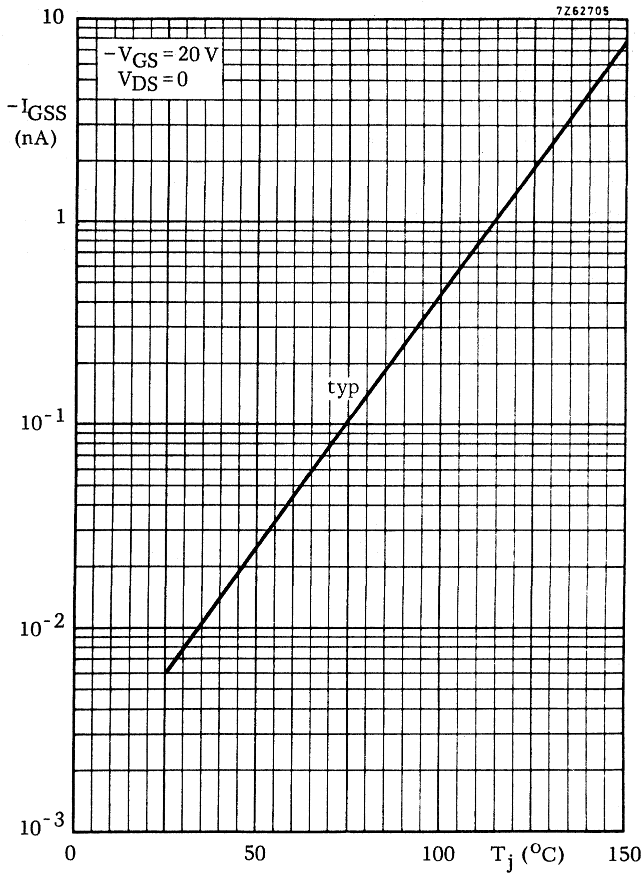


Fig. 2

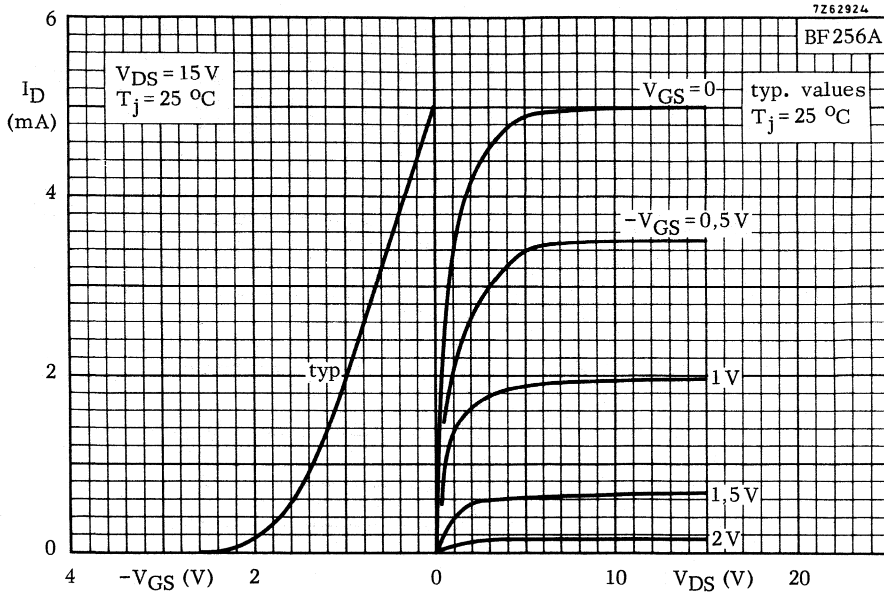


Fig. 3

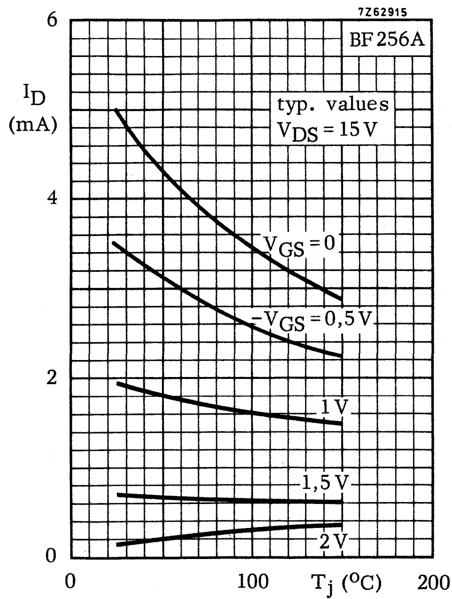


Fig. 4

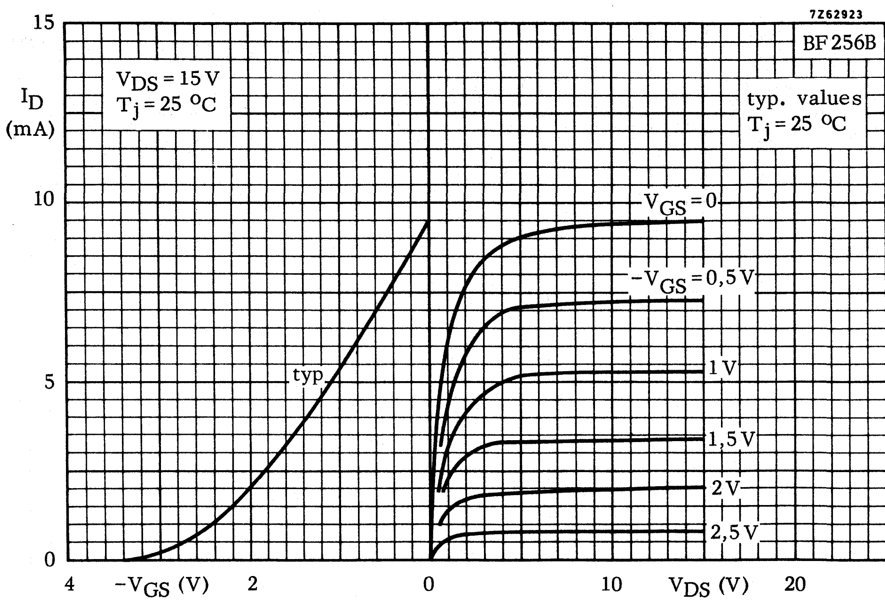


Fig. 5

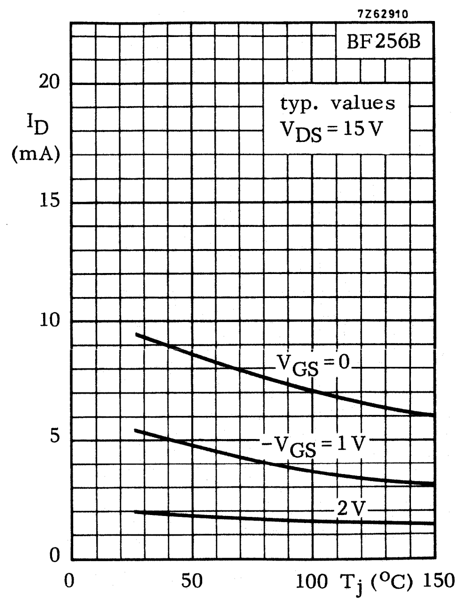


Fig. 6

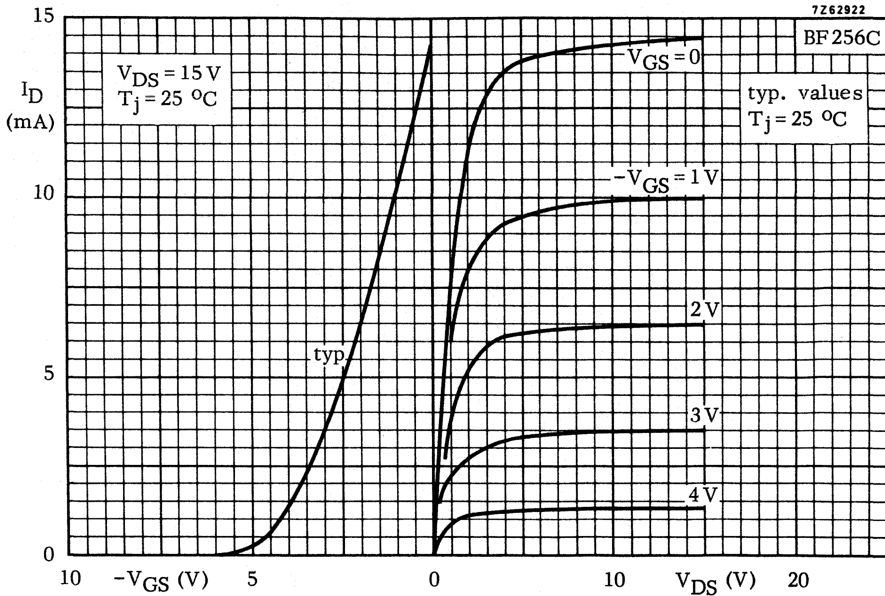


Fig. 7

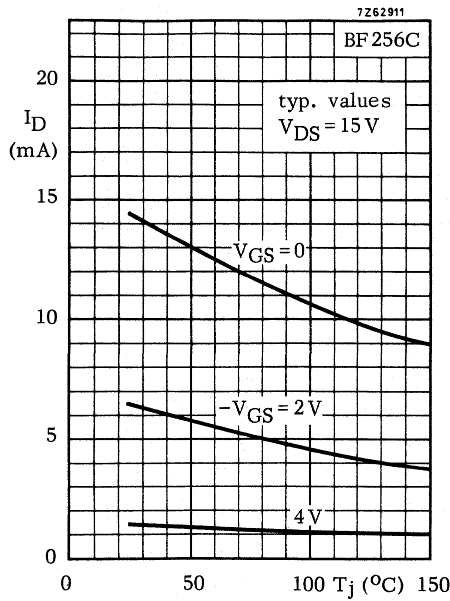


Fig. 8

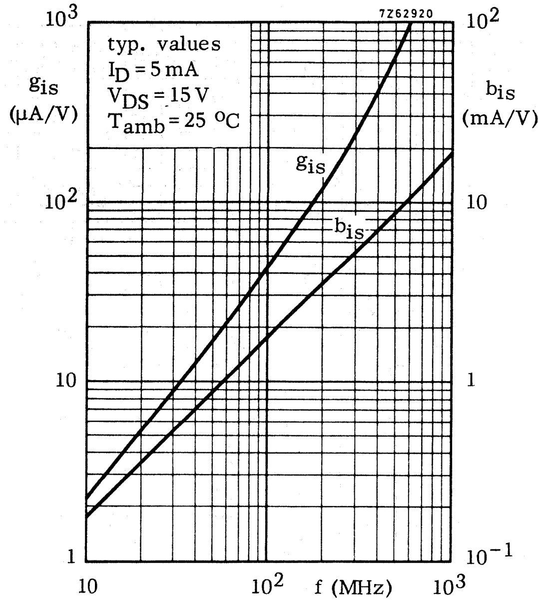


Fig. 9

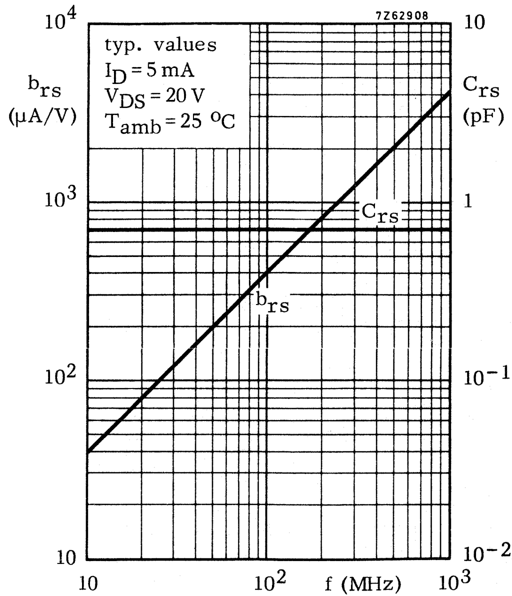


Fig. 10

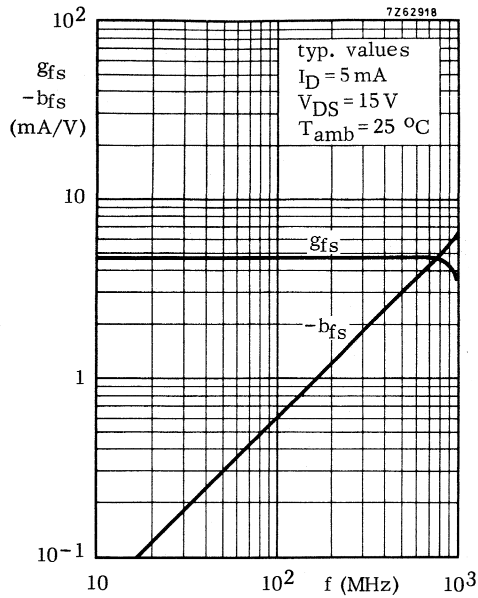


Fig. 11

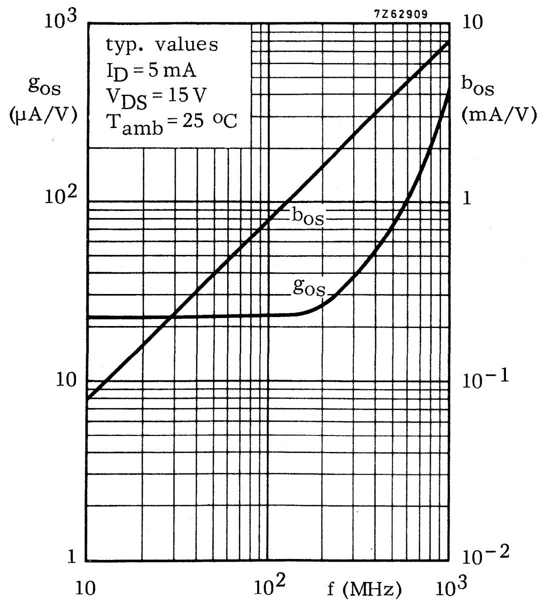


Fig. 12

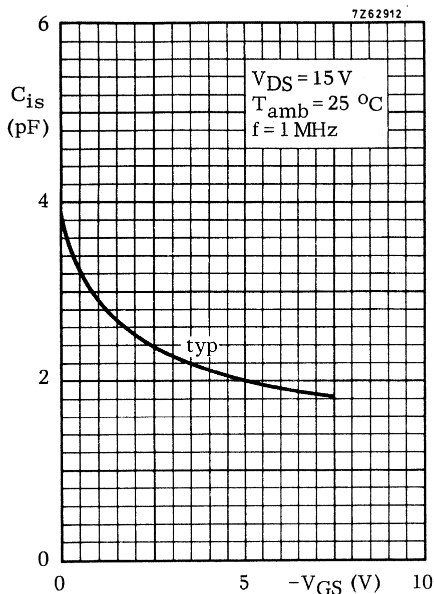


Fig. 13

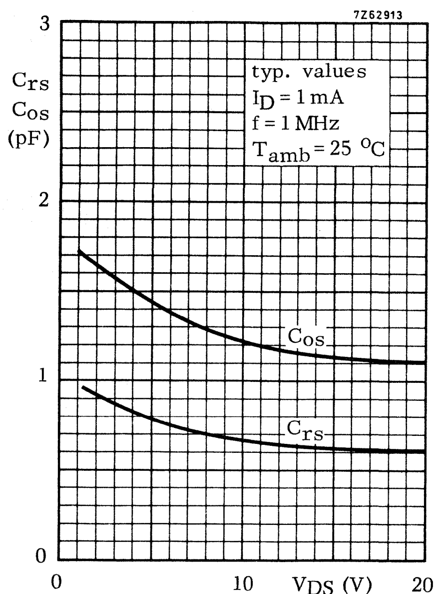


Fig. 14

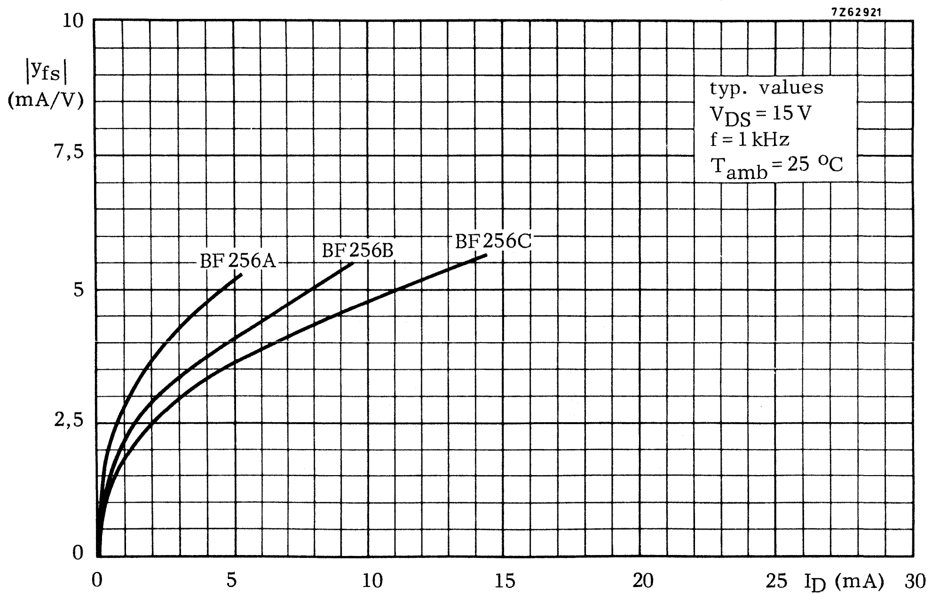


Fig. 15

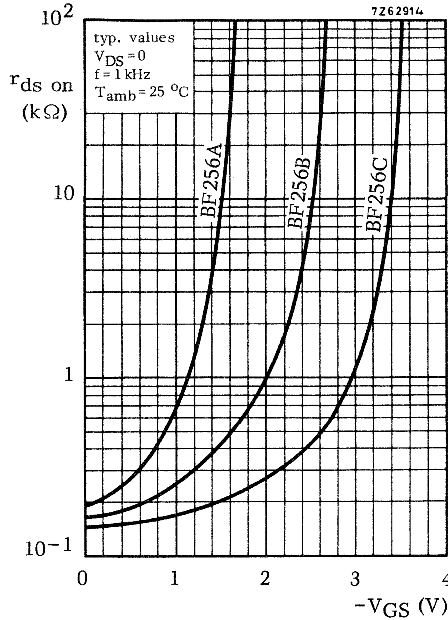


Fig. 16

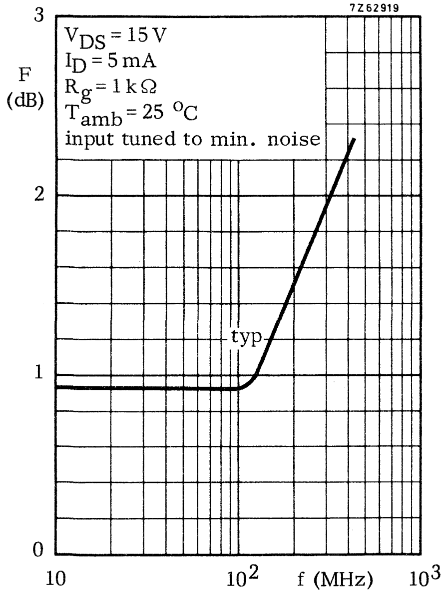


Fig. 17

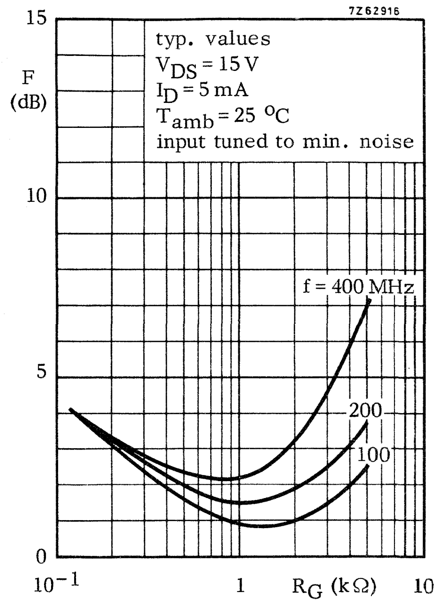


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the VHF range.
These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the RF stages in FM portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW

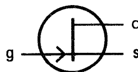
			BF410A	B	C	D	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Transfer admittance V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	min.	2.5	4	6	7	mS
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0.5	0.5	—	—	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	—	—	0.5	0.5	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz V_{DS} = 10 V; V_{GS} = 0	F	typ.	1.5	1.5	—	—	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	—	—	1.5	1.5	dB

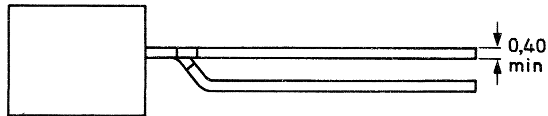
MECHANICAL DATA

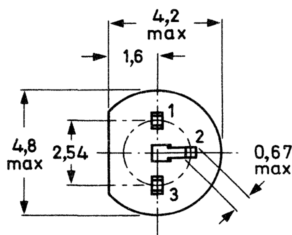
Dimensions in mm

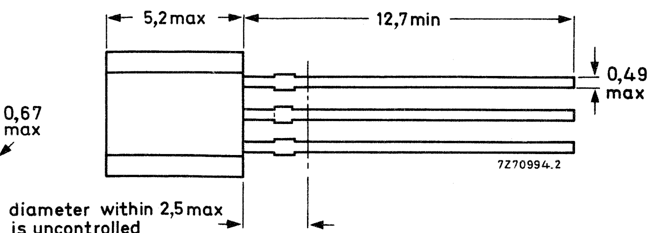
Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate









RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF410A	B	C	D	
Gate cut-off current $-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	max.	10	10	10	10	nA
Gate-drain breakdown voltage I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	min.	20	20	20	20	V
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Gate-source cut-off voltage I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for **BF410A** and **B**
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for **BF410C** and **D**

y-parameters (common source)			BF410A	B	C	D	
Input capacitance at f = 1 MHz	C_{is}	max.	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.5	0.5	0.5	0.5	pF
		max.	0.7	0.7	0.7	0.7	pF
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	min.	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\|y_{fs}\|$	min.	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\|y_{fs}\|$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	max.	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	max.	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

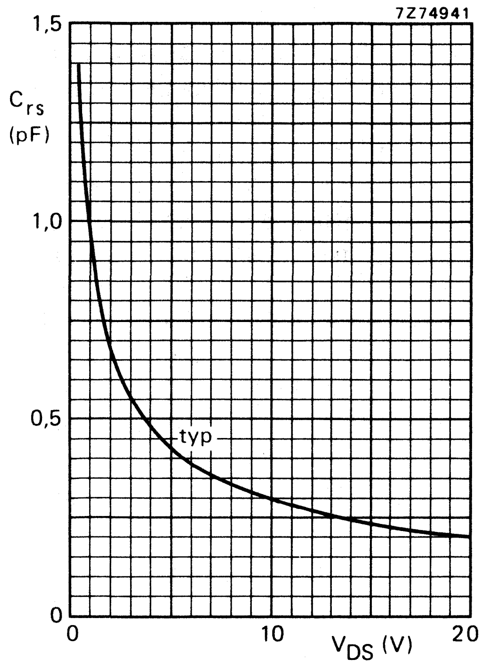


Fig. 2 $V_{GS} = 0$ for **BF410A** and **BF410B**; $I_D = 5$ mA for **BF410C** and **BF410D**; f = 1 MHz; $T_{amb} = 25\ ^oC$.

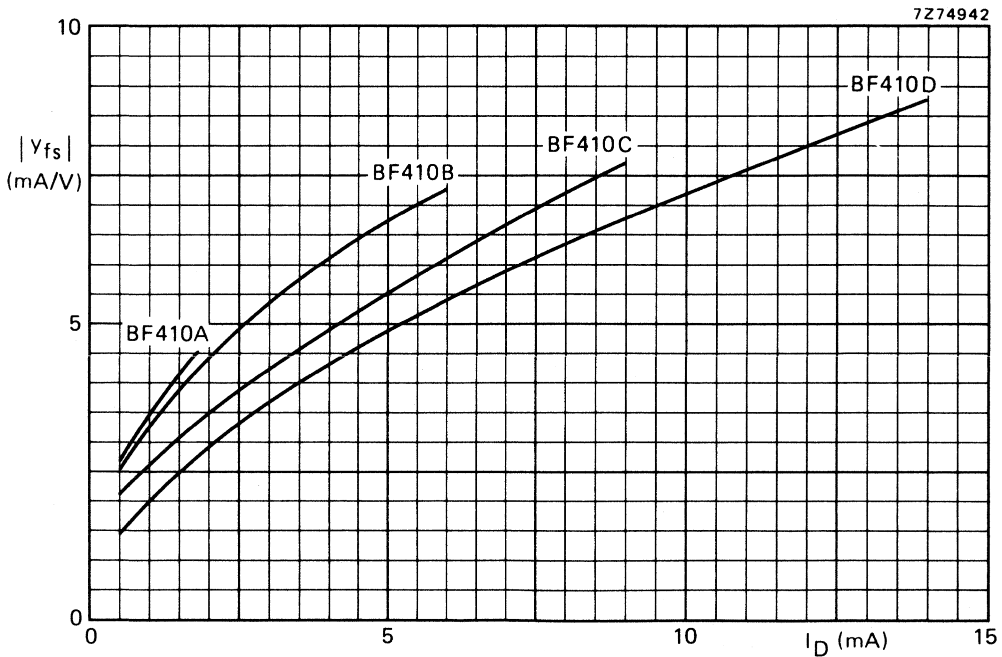


Fig. 3 $V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25\ ^oC$; typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.		20			V
Drain current (DC or average)	I_D	max.		30			mA
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.		250			mW
			BF510	511	512	513	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Transfer admittance (common source) V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	>	2.5	4	6	7	mS
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0.3	0.3	—	—	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	—	—	0.3	0.3	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz							
V_{DS} = 10 V; V_{GS} = 0	F	typ.	1.5	1.5	—	—	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	—	—	1.5	1.5	dB

MECHANICAL DATA

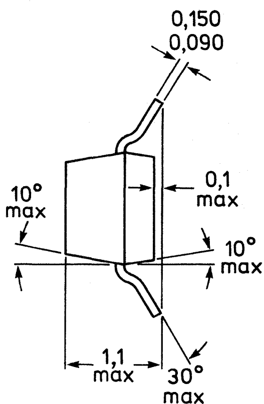
SOT23.

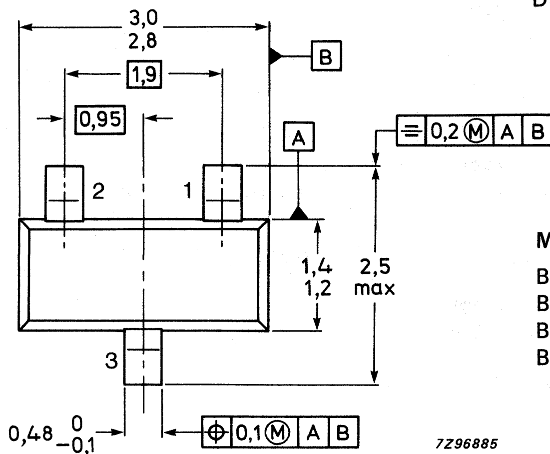
See also *Soldering recommendations.*

MECHANICAL DATA

Fig. 1 SOT23.

Dimensions in mm

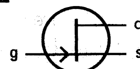




TOP VIEW

Pinning

1 = gate
2 = drain
3 = source



Marking code

BF510 = S6p
BF511 = S7p
BF512 = S8p
BF513 = S9p

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-gate voltage (open source)	V_{DGO}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate current	$\pm I_G$	max.	10 mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

Note

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF510	511	512	513	
Gate cut-off current $-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Gate-source cut-off voltage I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF510 and BF511
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF512 and BF513

y-parameters (common source)			BF510	511	512	513	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.3	0.3	0.3	0.3	pF
		<	0.4	0.4	0.4	0.4	pF
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\|y_{fs}\|$	>	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\|y_{fs}\|$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

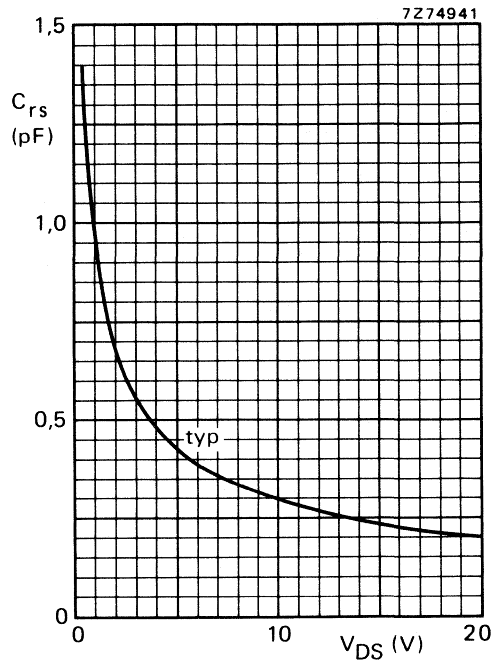


Fig. 2 $V_{GS} = 0$ for BF510 and BF511;
$I_D = 5$ mA for BF512 and BF513;
f = 1 MHz; $T_{amb} = 25\ ^{o}C$.

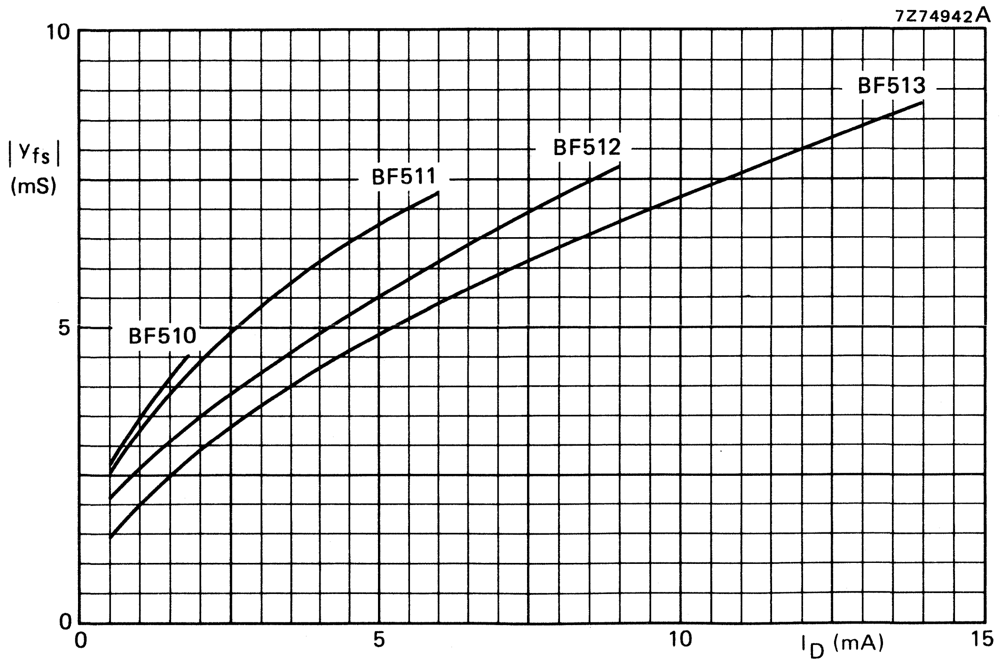


Fig. 3 $V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25\ ^{o}C$; typical values.

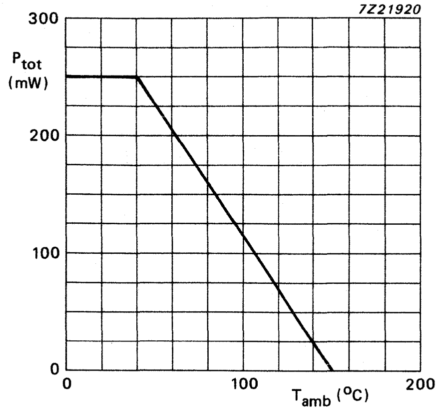


Fig.4 Power derating curve.

N-channel silicon junction field-effect transistor

BF545A; BF545B; BF545C

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage (max. 2.2 V for BF545A).

DESCRIPTION

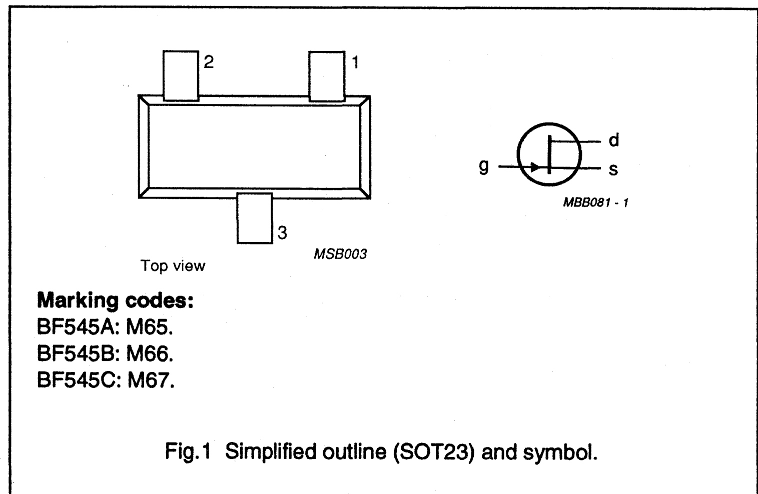
N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are specially designed for use as impedance converters in (for example) electret microphones and infra-red detectors, and as VHF amplifiers in oscillators and mixers.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BF545A		2	6.5	mA
	BF545B		6	15	mA
	BF545C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 μA	0.4	7.8	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	6.5	mS



Marking codes:
BF545A: M65.
BF545B: M66.
BF545C: M67.

Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
$-V_{GSO}$	gate-source voltage		–	30	V
$-V_{GDO}$	gate-drain voltage		–	30	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

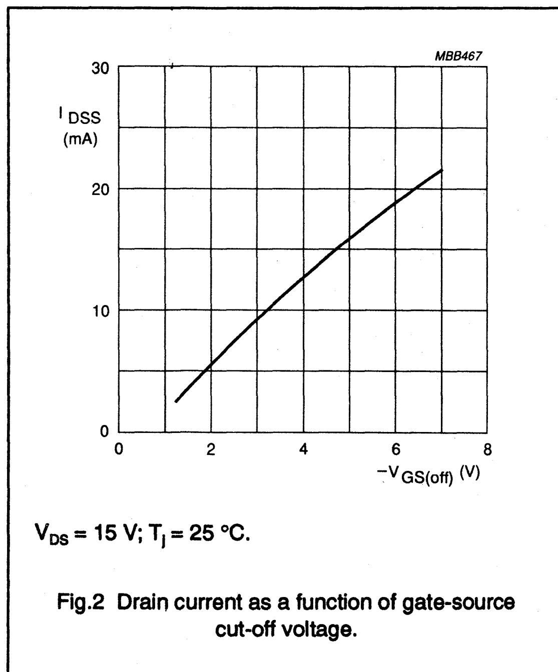
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{DS}$ = 0; $-V_{GS}$ = 20 V	–	0.5	1000	pA
		$-V_{DS}$ = 0; $-V_{GS}$ = 20 V; T_j = 125 °C	–	–	100	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF545A		2	–	6.5	mA
	BF545B		6	–	15	mA
	BF545C		12	–	25	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; $-I_G$ = 1 μA	30	–	–	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 μA				
	BF545A		0.4	–	2.2	V
	BF545B		1.6	–	3.8	V
	BF545C		3.2	–	7.8	V
		V_{DS} = 15 V; I_D = 1 μA	0.4	–	7.8	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	–	6.5	mS
Y_{os}	common source output admittance	V_{DS} = 15 V; V_{GS} = 0	–	40	–	μS

DYNAMIC CHARACTERISTICS

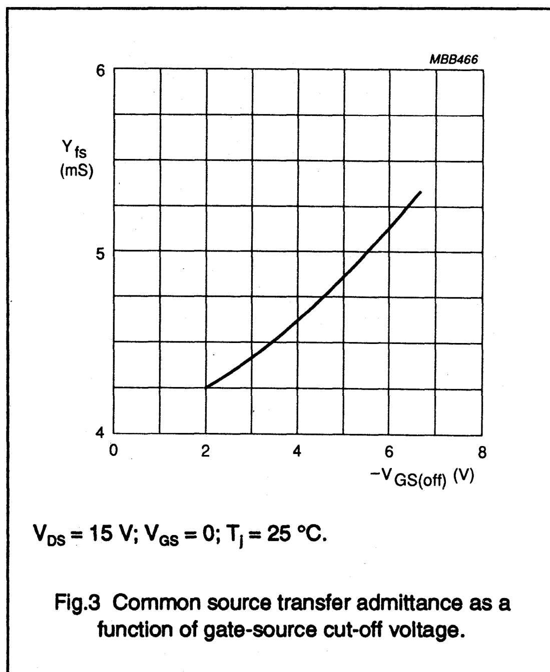
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	1.7	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	3	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	15	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	300	µS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	2	mS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	1.8	mS
$-g_{rs}$	common source feedback conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	6	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	40	µS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	30	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	60	µS



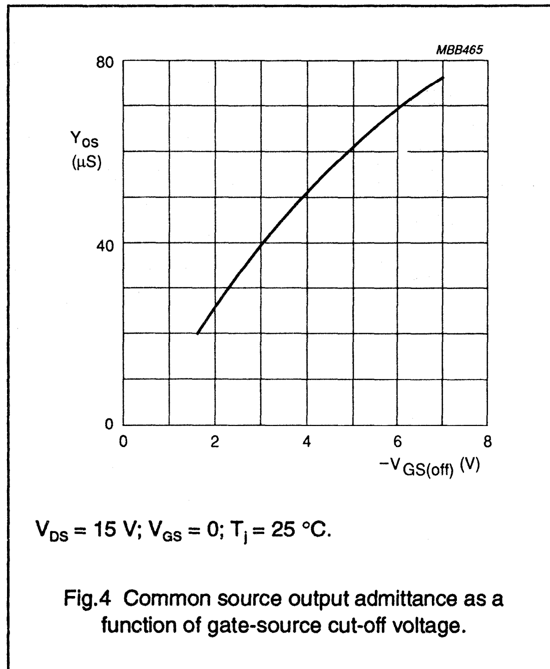
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage.



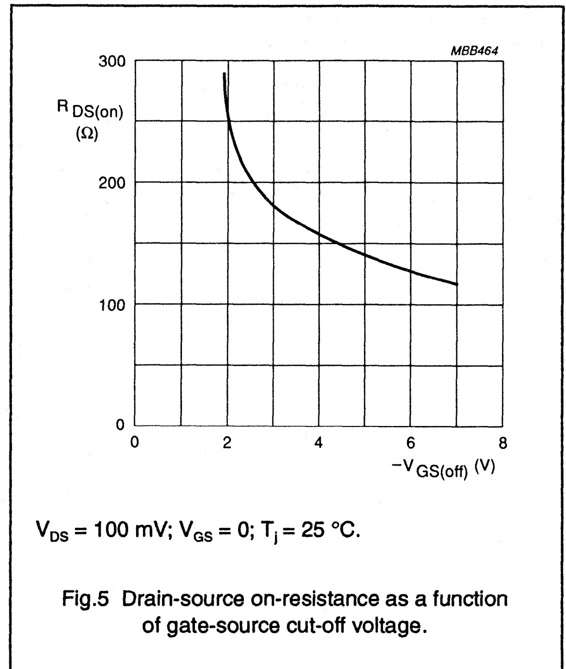
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



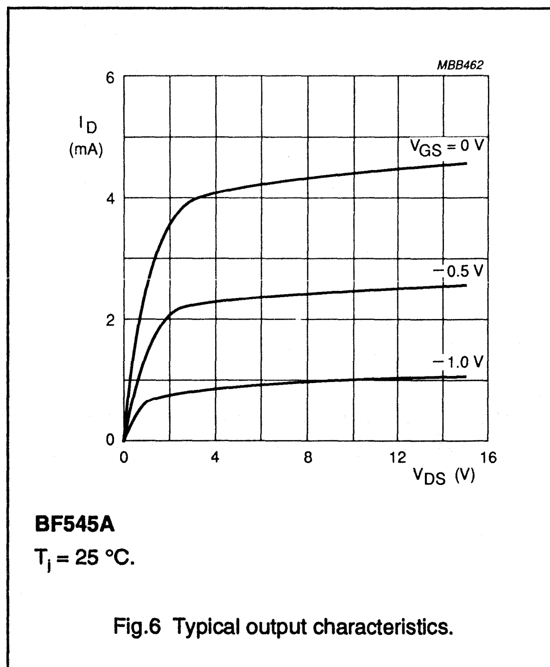
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.4 Common source output admittance as a function of gate-source cut-off voltage.



V_{DS} = 100 mV; V_{GS} = 0; T_j = 25 °C.

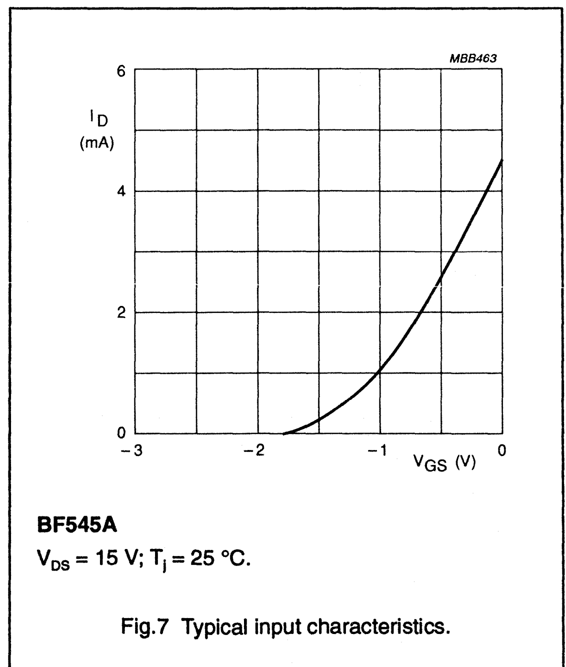
Fig.5 Drain-source on-resistance as a function of gate-source cut-off voltage.



BF545A

T_j = 25 °C.

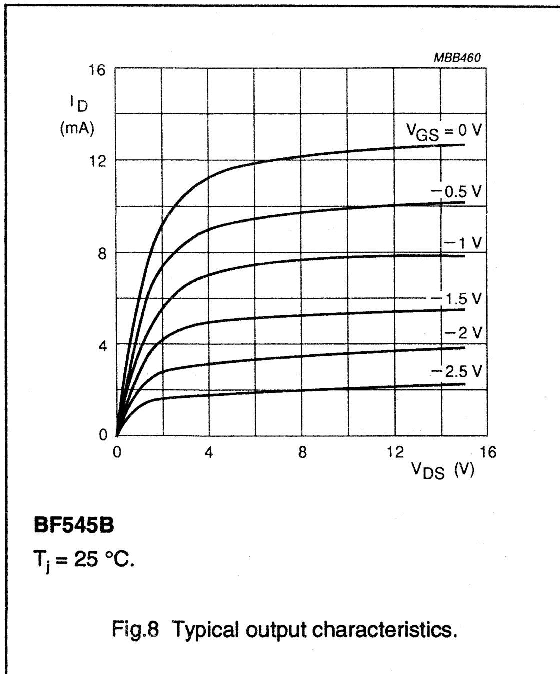
Fig.6 Typical output characteristics.



BF545A

V_{DS} = 15 V; T_j = 25 °C.

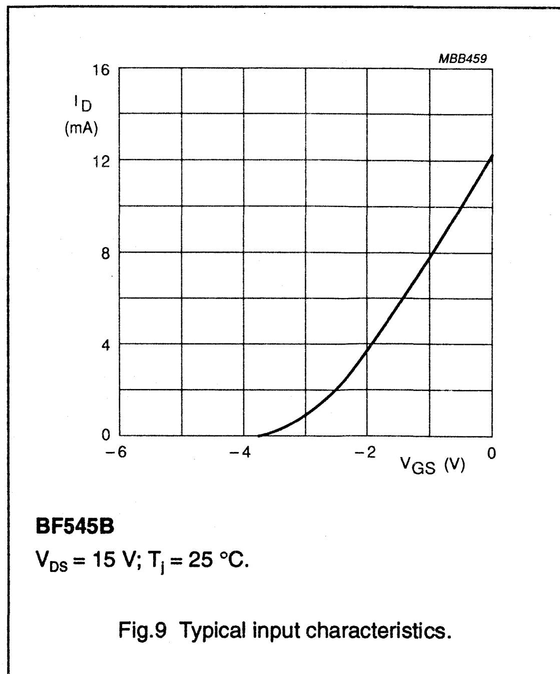
Fig.7 Typical input characteristics.



BF545B

T_j = 25 °C.

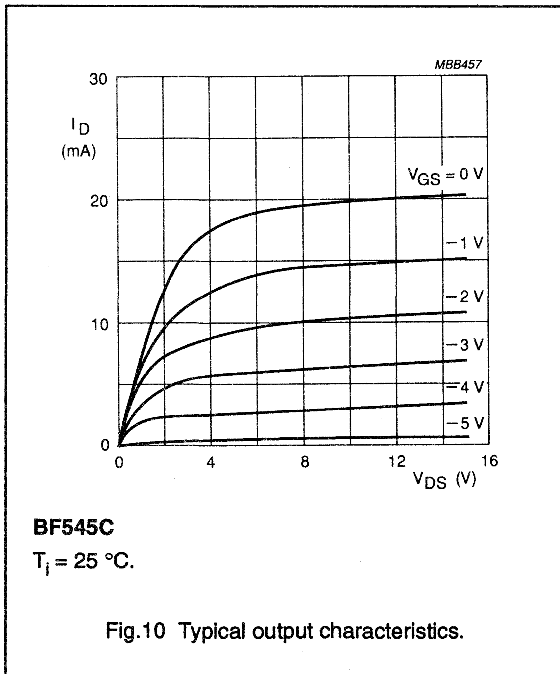
Fig.8 Typical output characteristics.



BF545B

V_{DS} = 15 V; T_j = 25 °C.

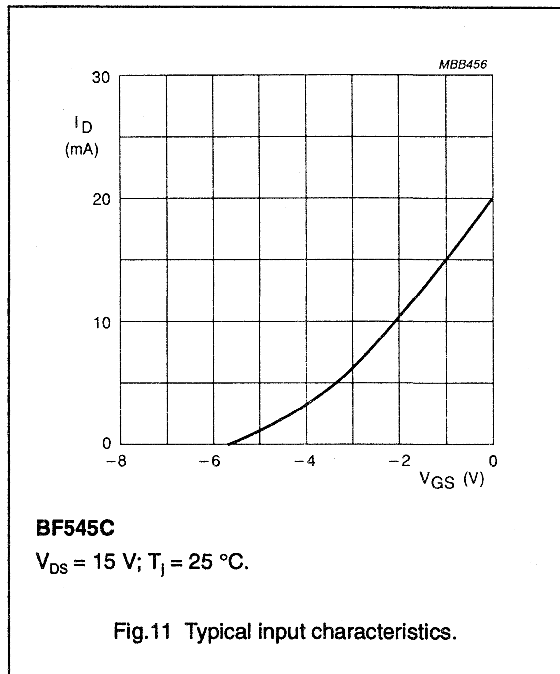
Fig.9 Typical input characteristics.



BF545C

T_j = 25 °C.

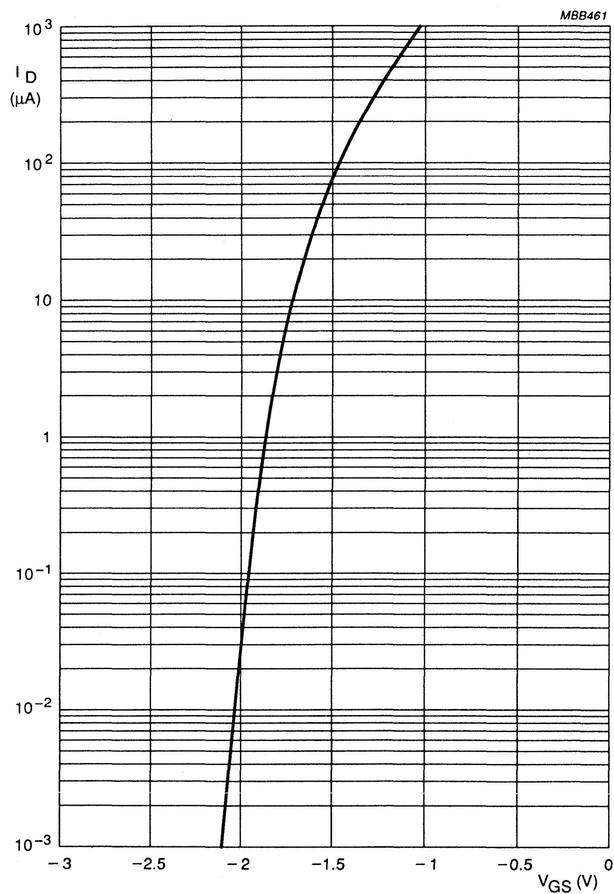
Fig.10 Typical output characteristics.



BF545C

V_{DS} = 15 V; T_j = 25 °C.

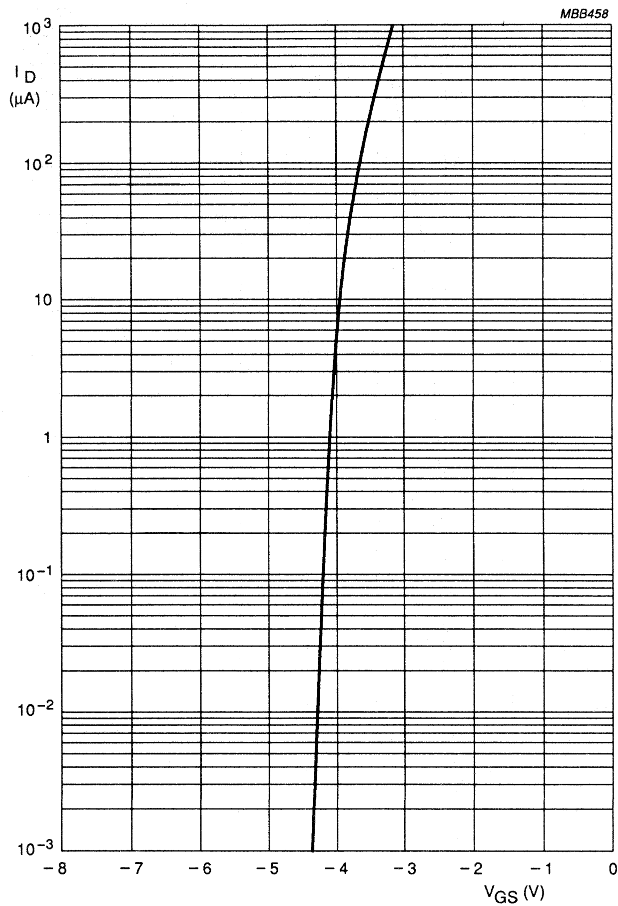
Fig.11 Typical input characteristics.



BF545A

V_{DS} = 15 V; T_j = 25 °C.

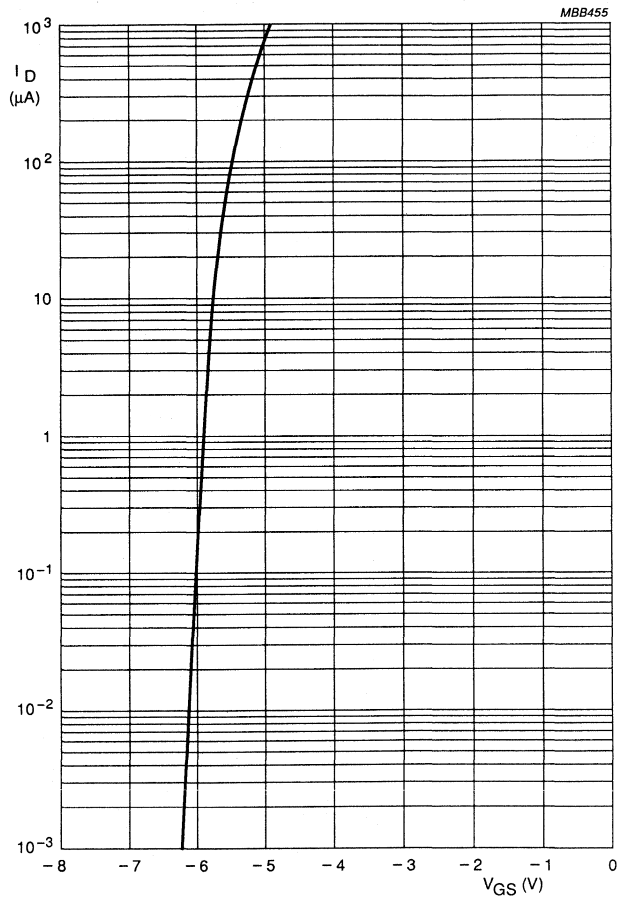
Fig.12 Drain current as a function of gate-source voltage; typical values.



BF545B

V_{DS} = 15 V; T_j = 25 °C.

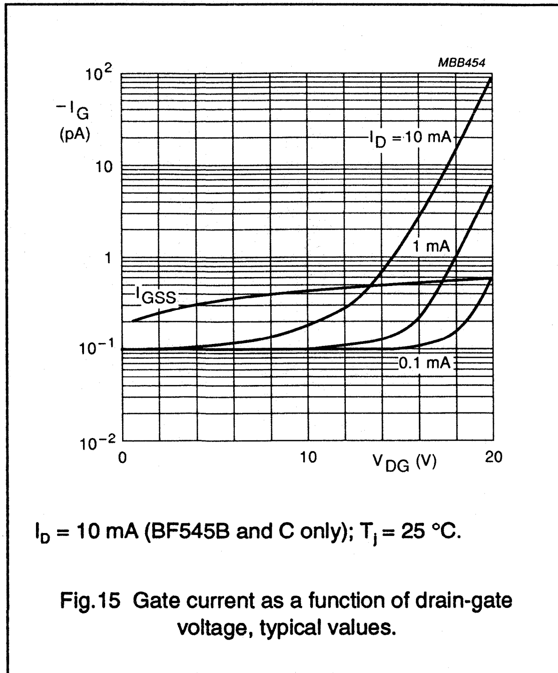
Fig.13 Drain current as a function of gate-source voltage; typical values.



BF545C

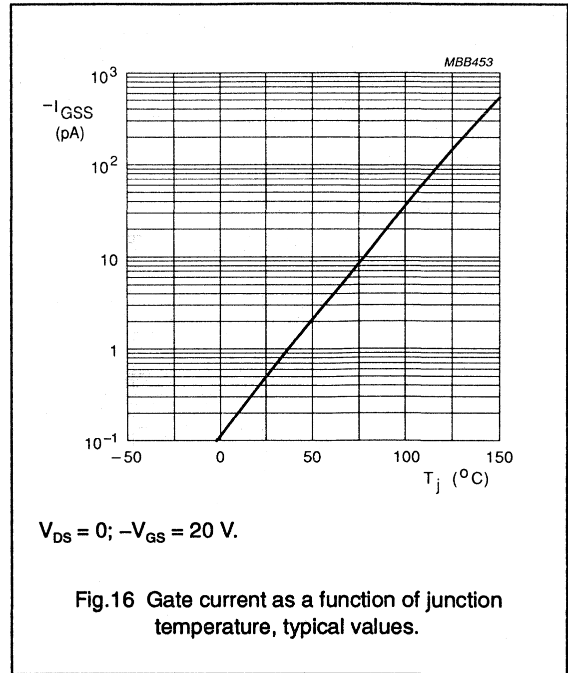
V_{DS} = 15 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage; typical values.



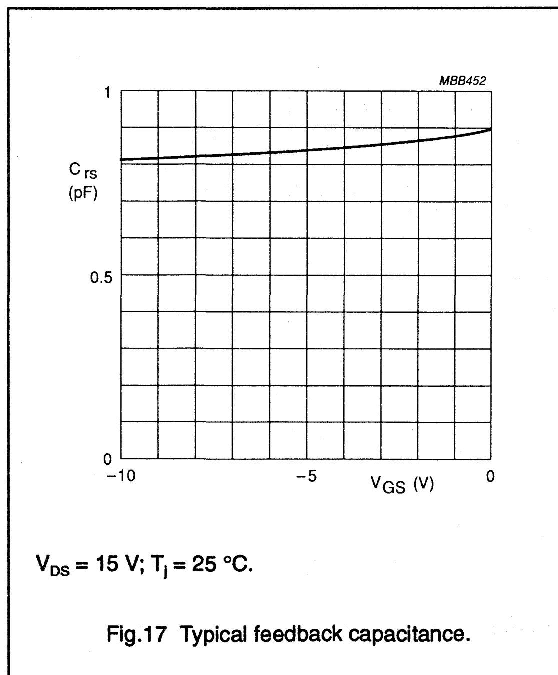
I_D = 10 mA (BF545B and C only); T_j = 25 °C.

Fig.15 Gate current as a function of drain-gate voltage, typical values.



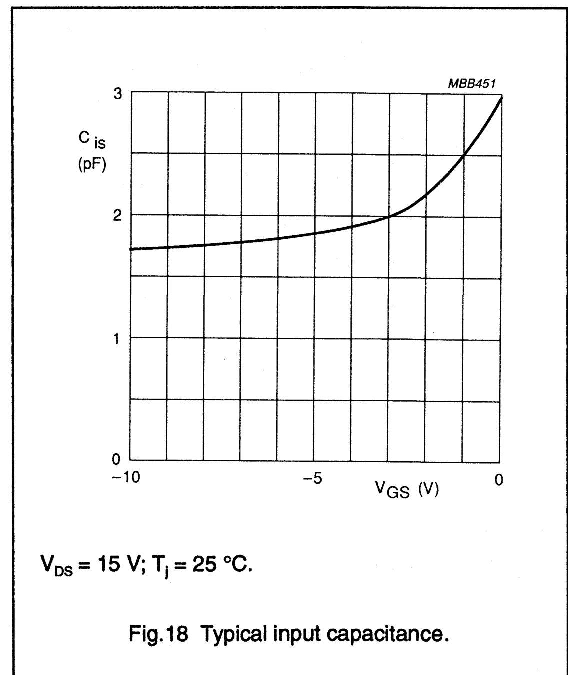
V_{DS} = 0; $-V_{GS}$ = 20 V.

Fig.16 Gate current as a function of junction temperature, typical values.



V_{DS} = 15 V; T_j = 25 °C.

Fig.17 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.18 Typical input capacitance.

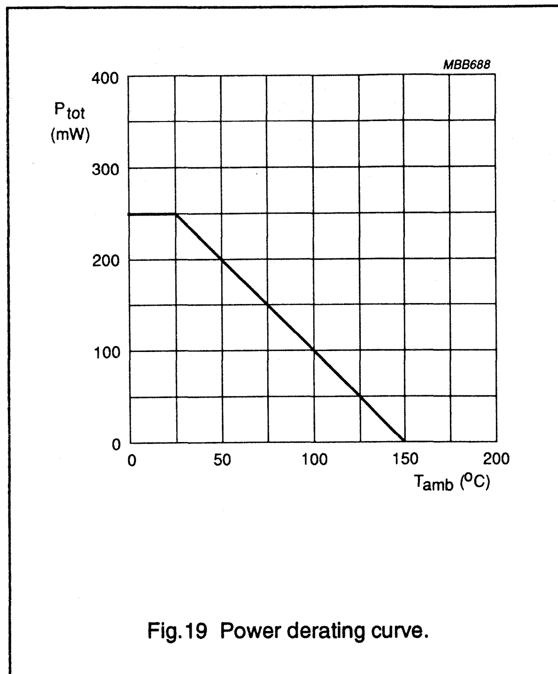
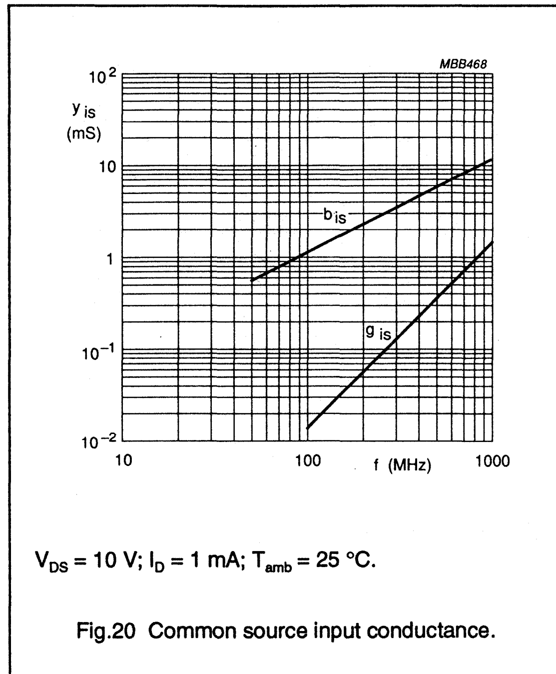
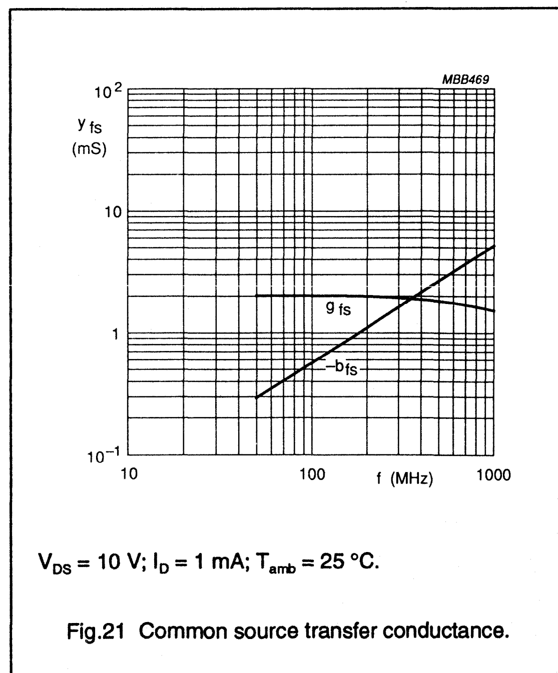


Fig.19 Power derating curve.



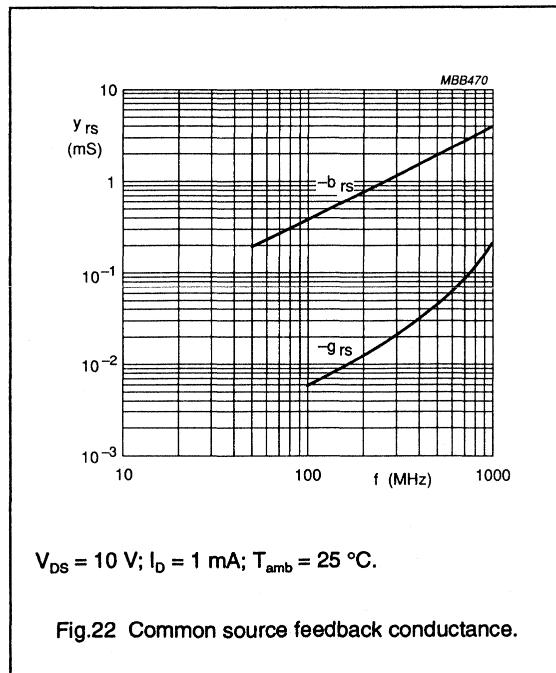
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.20 Common source input conductance.



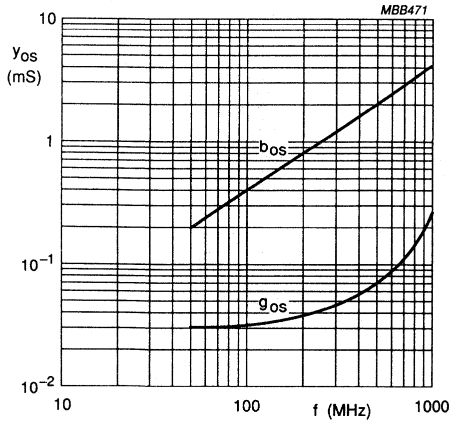
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.21 Common source transfer conductance.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.22 Common source feedback conductance.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.23 Common source output conductance.

N-channel field-effect transistors BF556A;BF556B;BF556C

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are specially designed for use as impedance converters in (for example) electret microphones and infra-red detectors, and as VHF amplifiers in oscillators and mixers.

PINNING - SOT23

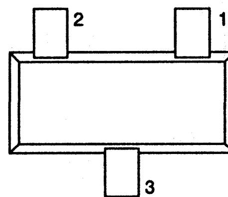
PIN	DESCRIPTION
1	source
2	drain
3	gate

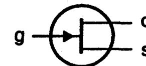
CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BF556A		3	7	mA
	BF556B		6	13	mA
	BF556C		11	18	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 μA	0.5	7.5	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	–	mS





MAM036

Marking codes:
BF556A: M84.
BF556B: M85.
BF556C: M86.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
$-V_{GSO}$	gate-source voltage		–	30	V
$-V_{GDO}$	gate-drain voltage		–	30	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm^2.

STATIC CHARACTERISTICS

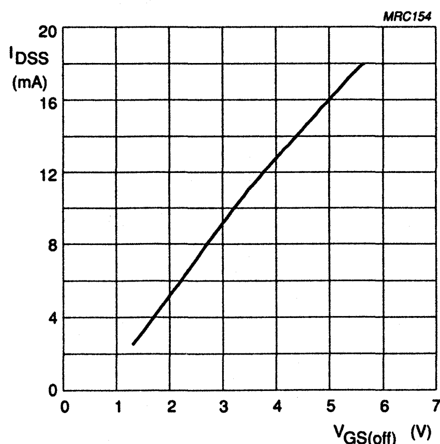
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; $-I_G$ = 1 μA	30	–	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF556A		3	–	7	mA
	BF556B		6	–	13	mA
	BF556C		11	–	18	mA
$-I_{GSS}$	reverse gate leakage current	V_{DS} = 0; $-V_{GS}$ = 20 V	–	0.5	5000	pA
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 μA	0.5	–	7.5	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	–	–	mS
$\lvert Y_{os} \rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0	–	40	–	μS

DYNAMIC CHARACTERISTICS

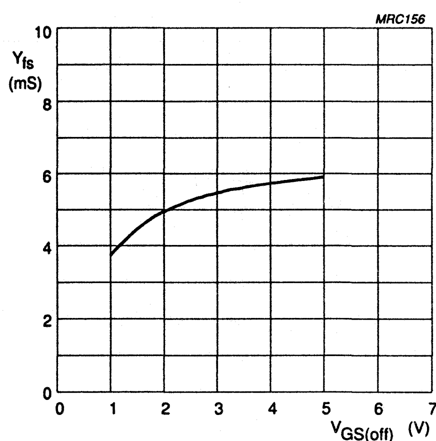
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	1.7	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	3	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	15	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	300	µS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	2	mS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	1.8	mS
$-g_{rs}$	common source feedback conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	6	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	40	µS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	30	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	60	µS
V_n	equivalent input noise voltage	VDS = 10 V; I_D = 1 mA; f = 100 Hz	40	nV/√Hz



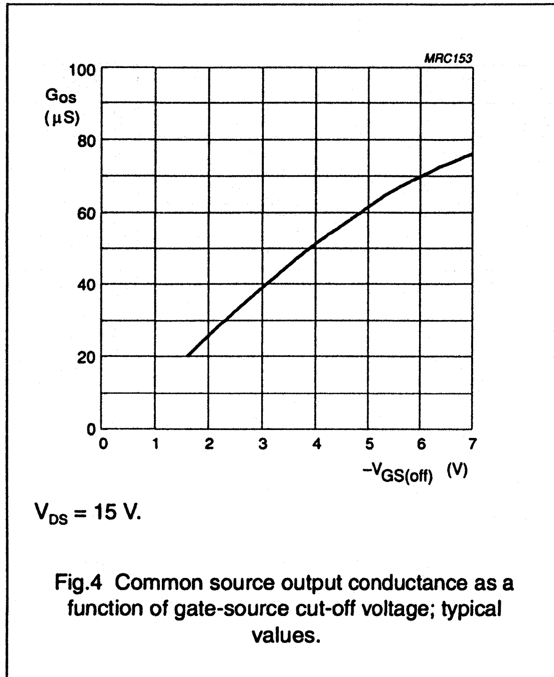
V_{DS} = 15 V.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



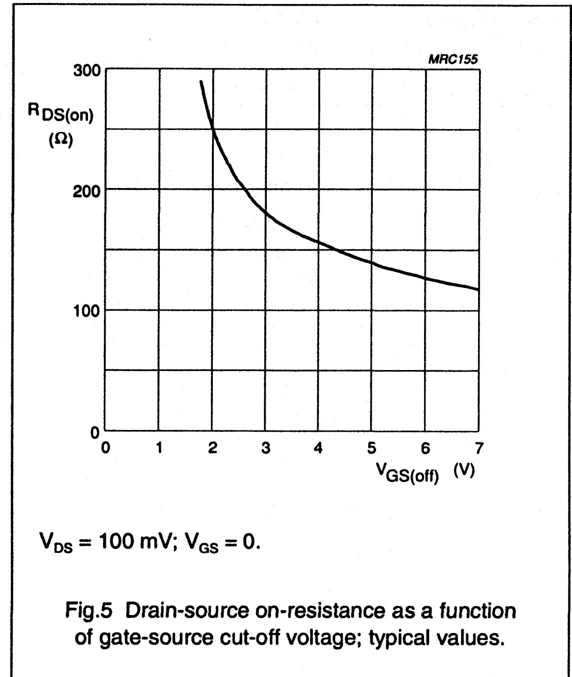
V_{DS} = 15 V; I_D = 1 µA.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



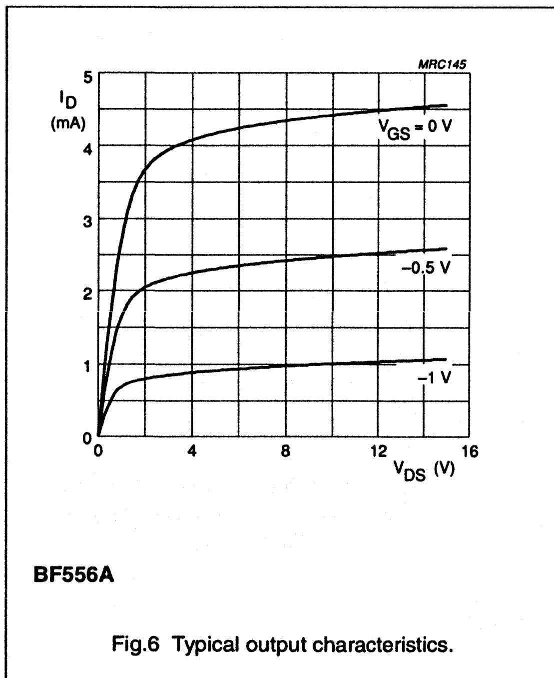
V_{DS} = 15 V.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



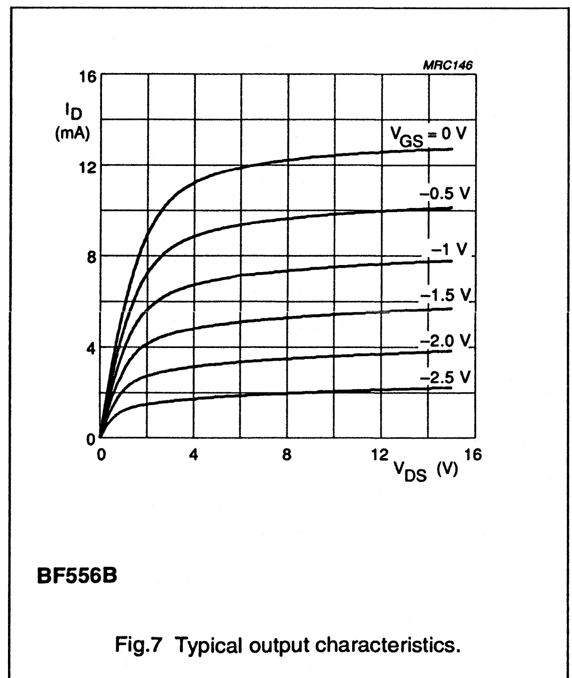
V_{DS} = 100 mV; V_{GS} = 0.

Fig.5 Drain-source on-resistance as a function of gate-source cut-off voltage; typical values.



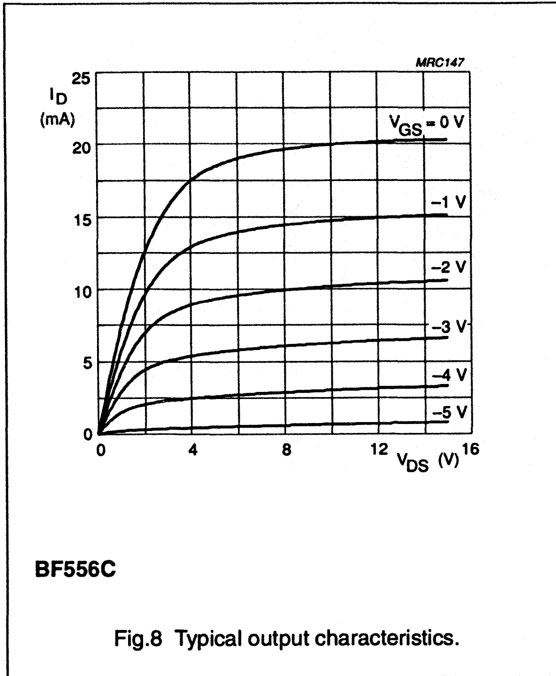
BF556A

Fig.6 Typical output characteristics.



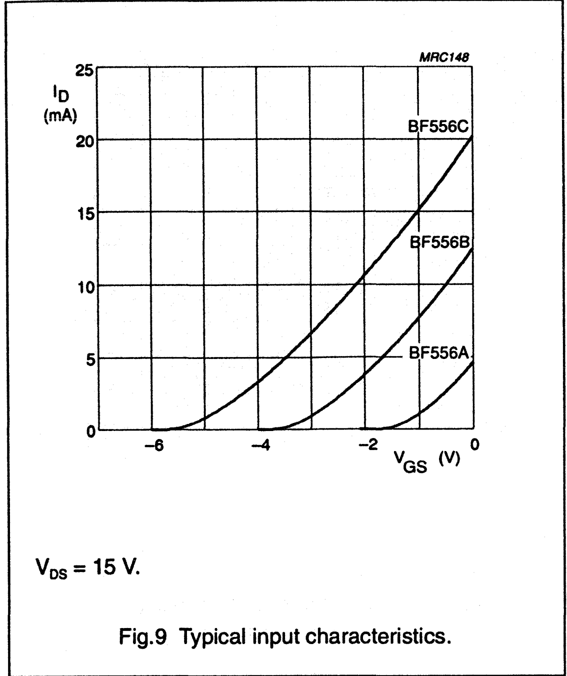
BF556B

Fig.7 Typical output characteristics.



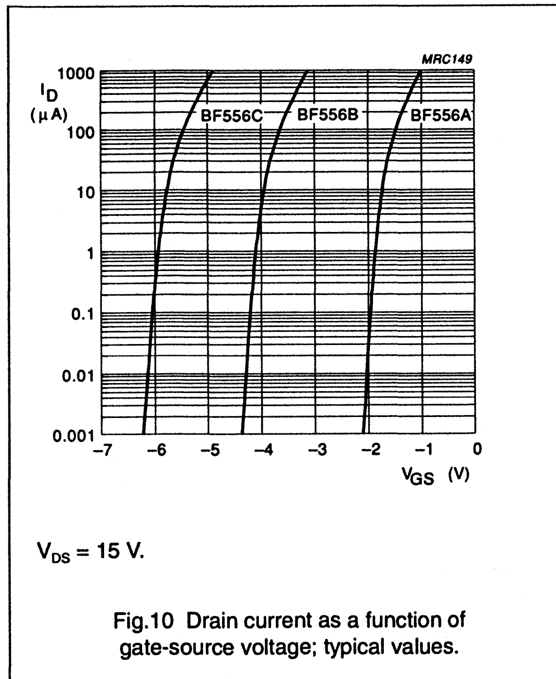
BF556C

Fig.8 Typical output characteristics.



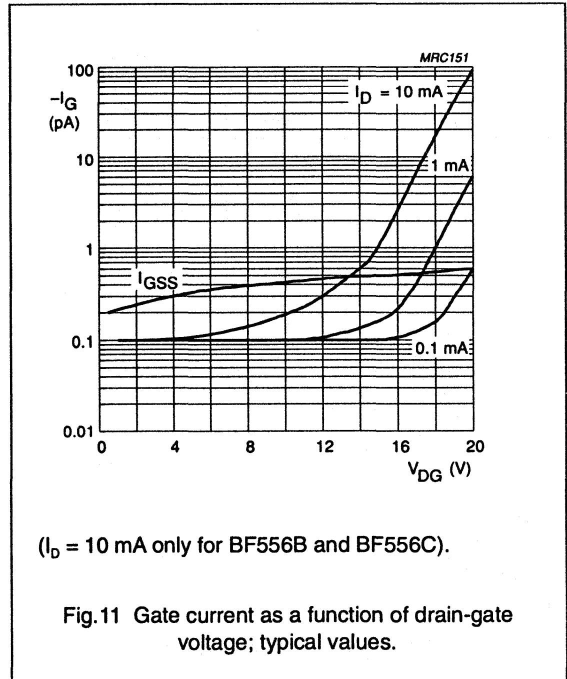
V_{DS} = 15 V.

Fig.9 Typical input characteristics.



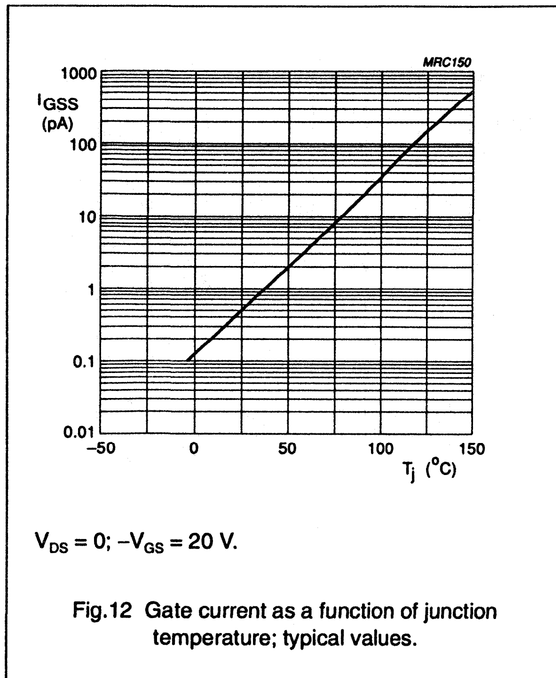
V_{DS} = 15 V.

Fig.10 Drain current as a function of gate-source voltage; typical values.



(I_D = 10 mA only for BF556B and BF556C).

Fig.11 Gate current as a function of drain-gate voltage; typical values.



$V_{DS} = 0$; $-V_{GS} = 20$ V.

Fig.12 Gate current as a function of junction temperature; typical values.

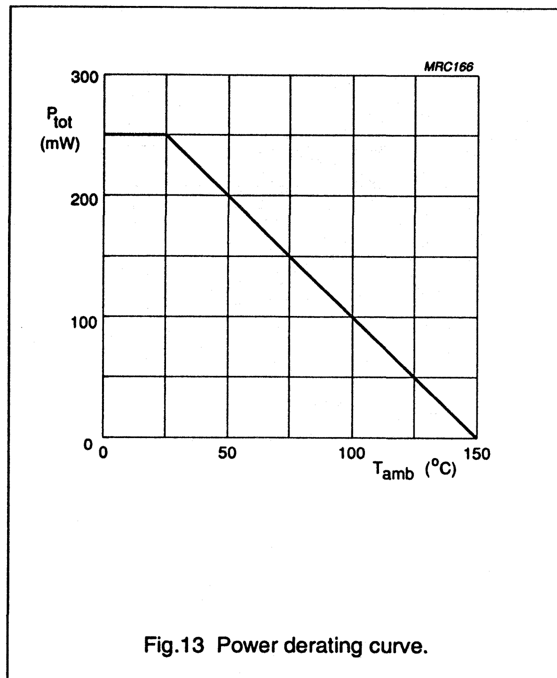
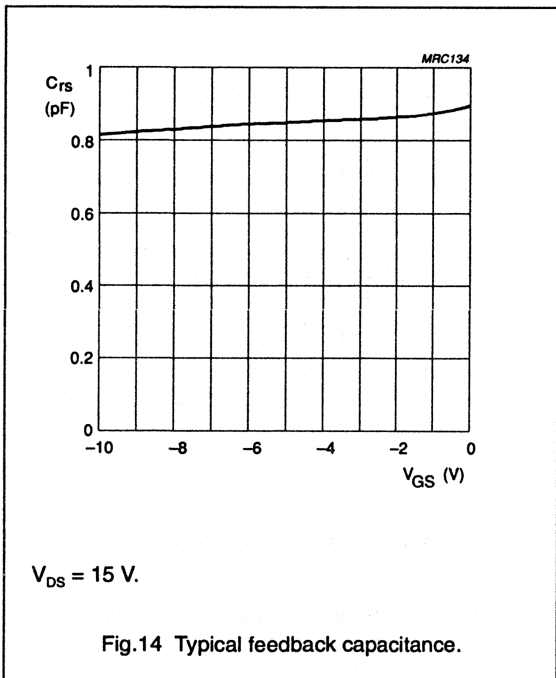
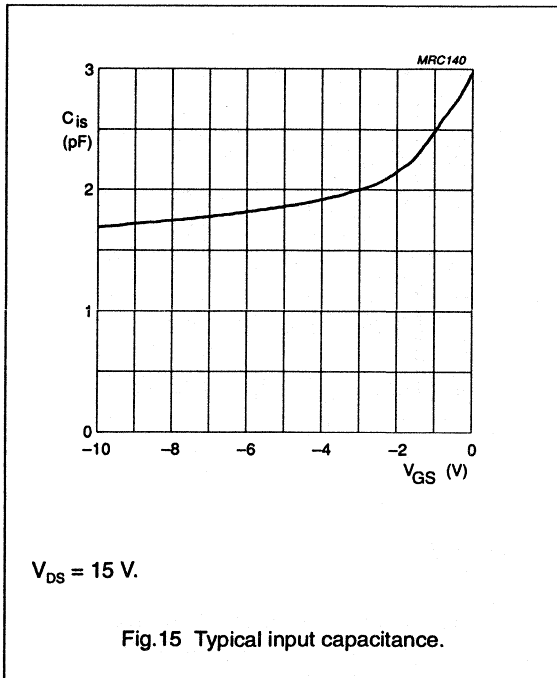


Fig.13 Power derating curve.



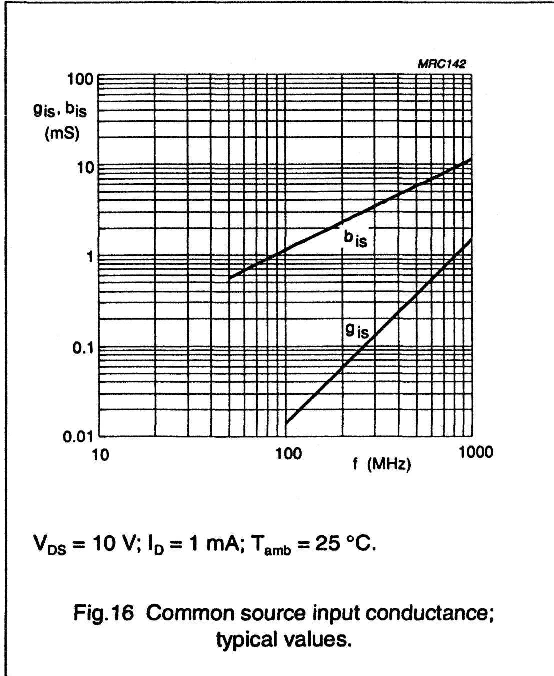
$V_{DS} = 15$ V.

Fig.14 Typical feedback capacitance.



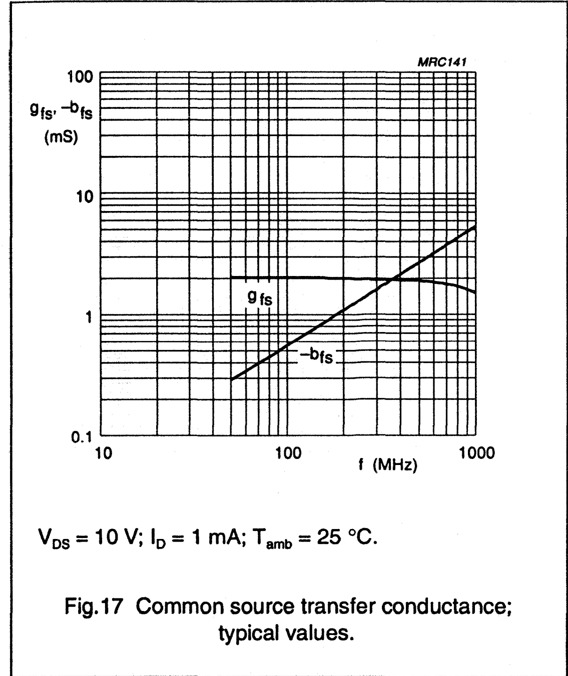
$V_{DS} = 15$ V.

Fig.15 Typical input capacitance.



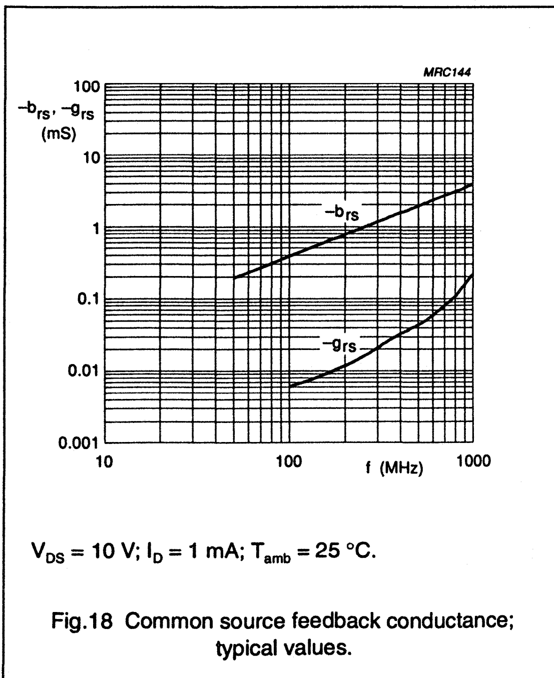
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.16 Common source input conductance; typical values.



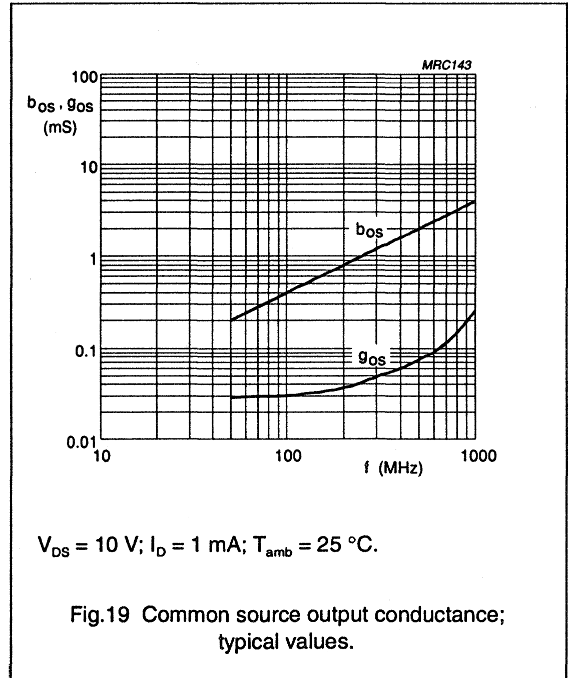
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.17 Common source transfer conductance; typical values.



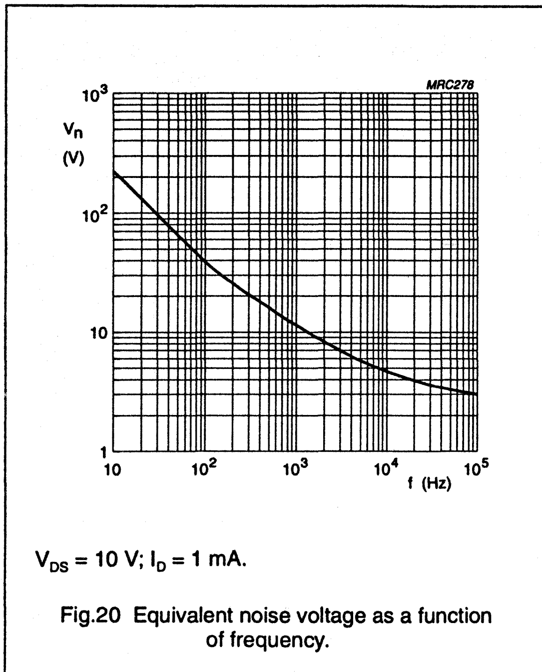
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.18 Common source feedback conductance; typical values.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.19 Common source output conductance; typical values.



V_{DS} = 10 V; I_D = 1 mA.

Fig.20 Equivalent noise voltage as a function of frequency.

Silicon n-channel dual gate MOS-FETs

BF901; BF901R

FEATURES

- Intended for low voltage operation
- Short channel transistor with high ratio $|Y_{fs}|:C_{is}$
- Low noise gain-controlled amplifier to 1 GHz
- BF901R has reverse pinning.

DESCRIPTION

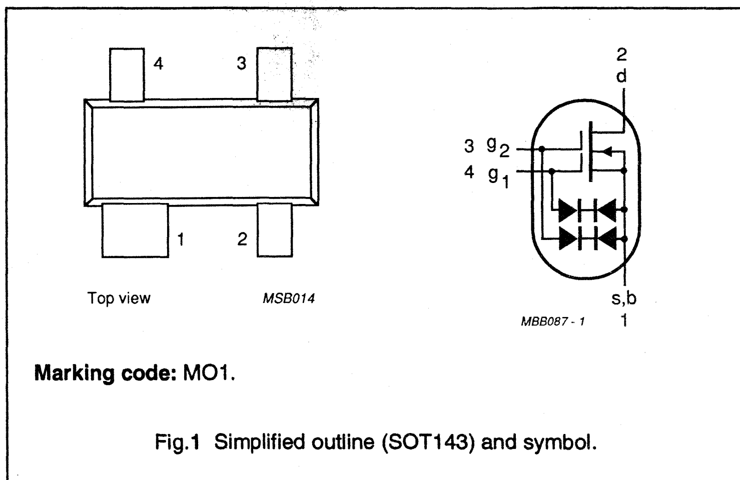
Enhancement type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes, with source and substrate interconnected. They are intended for UHF and VHF applications, such as television tuners and professional communications equipment especially suited for low voltage operation. These MOS-FET tetrodes are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

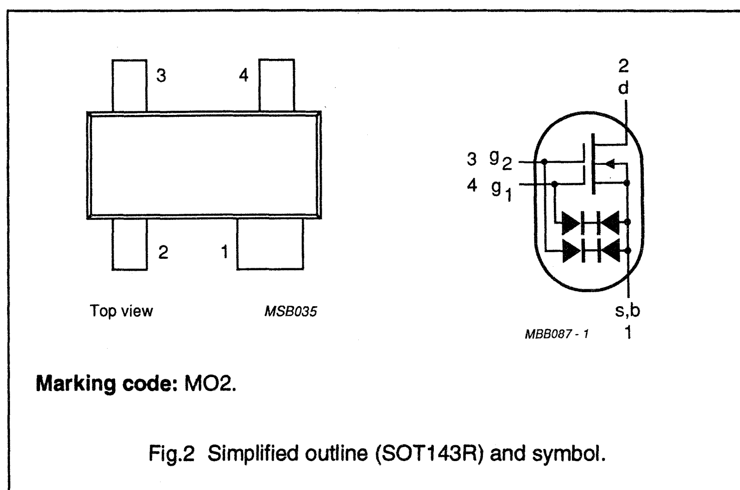
QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	12	V
I_D	drain current	–	30	mA
P_{tot}	total power dissipation	–	200	mW
T_j	junction temperature	–	150	°C
$\|Y_{fs}\|$	transfer admittance	28	35	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	2.35	2.75	pF
C_{rs}	feedback capacitance	25	–	fF
F	noise figure at 800 MHz	1.7	–	dB



Marking code: MO1.

Fig.1 Simplified outline (SOT143) and symbol.



Marking code: MO2.

Fig.2 Simplified outline (SOT143R) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
$V_{D\text{-}G2}$	drain-gate 2 voltage		–	6	V
I_D	DC drain current		–	30	mA
$\pm I_{G1\text{-}S}$	gate 1-source current		–	10	mA
$\pm I_{G2\text{-}S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation				
	BF901	up to T_{amb} = 50 °C (note 1)	–	200	mW
	BF901R	up to T_{amb} = 40 °C (note 1)	–	200	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient (note 1)	
	BF901	500 K/W
	BF901R	550 K/W

Note

1. Device mounted on an FR4 printboard.

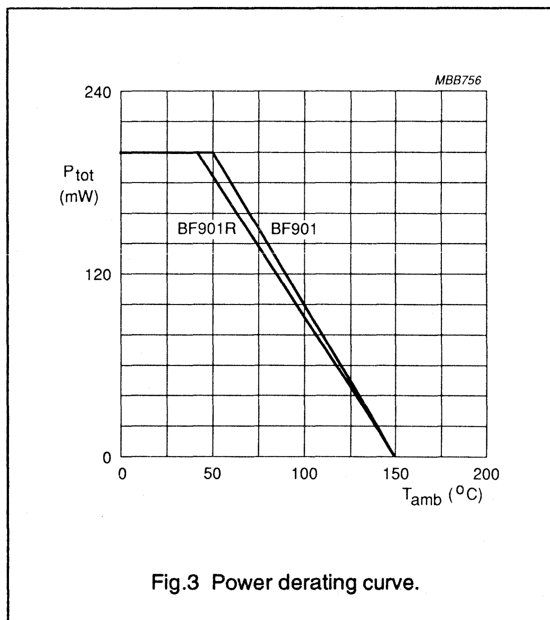


Fig.3 Power derating curve.

STATIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	–	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	–	50	nA
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	6	20	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$I_D = 20$ µA; $V_{DS} = 8$ V; $V_{G2\text{-}S} = 4$ V	0	0.7	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$I_D = 20$ µA; $V_{DS} = 8$ V; $V_{G1\text{-}S} = 0$	0.3	1	V
I_{DSX}	drain-source current	$V_{DS} = 4$ V; $V_{G1\text{-}S} = 1.1$ V; $V_{G2\text{-}S} = 3.4$ V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 14$ mA; $V_{DS} = 5$ V; $V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs}\rvert$	transfer admittance	pulsed; $T_j = 25$ °C	25	28	35	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.35	2.75	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	output capacitance	f = 1 MHz	–	1.4	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; $G_s = 2$ mS; $B_s = B_{sopt.}$	–	0.7	–	dB
		f = 800 MHz; $G_s = 3.3$ mS; $B_s = B_{sopt.}$	–	1.7	–	dB

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high $|Y_{fs}| : C_{is}$ ratio
- Low-noise gain-controlled amplifier to 1 GHz
- Superior cross-modulation performance during AGC.

DESCRIPTION

Enhancement type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes. They are intended for UHF and VHF applications, such as television tuners and professional communications equipment. These transistors consist of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

PINNING

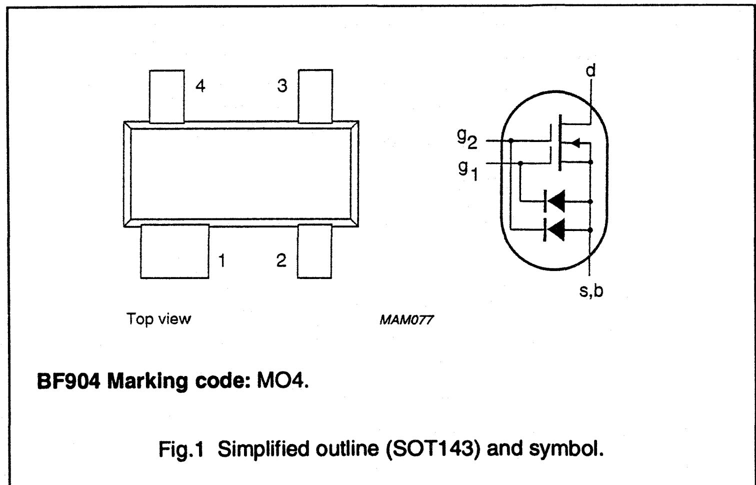
PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

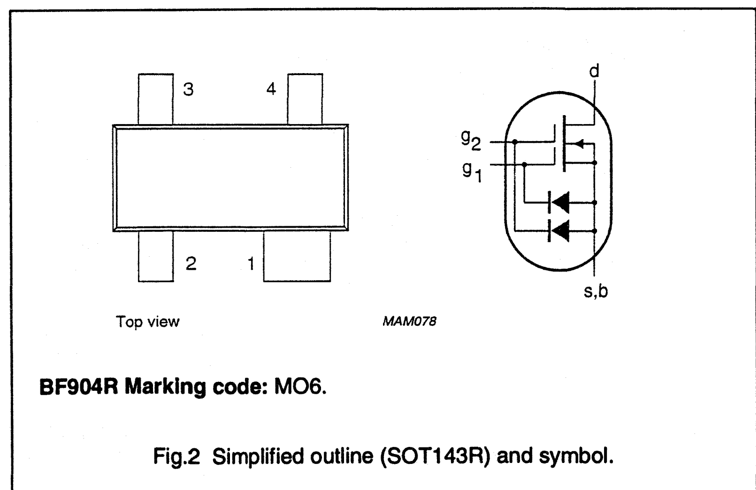
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	–	7	V
I_D	drain current	–	–	30	mA
P_{tot}	total power dissipation	–	–	200	mW
T_j	junction temperature	–	–	150	°C
$\|Y_{fs}\|$	transfer admittance	22	25	30	mS
C_{ig1-s}	input capacitance at gate 1	–	2.2	2.6	pF
C_{rs}	feedback capacitance	–	25	35	pF
F	noise figure at 800 MHz	–	2	–	dB



BF904 Marking code: MO4.

Fig.1 Simplified outline (SOT143) and symbol.



BF904R Marking code: MO6.

Fig.2 Simplified outline (SOT143R) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	DC drain current		–	30	mA
$\pm I_{G1\text{-}S}$	gate 1-source current		–	10	mA
$\pm I_{G2\text{-}S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation				
	BF904	up to T_{amb} = 50 °C (note 1)	–	200	mW
	BF904R	up to T_{amb} = 40 °C (note 1)	–	200	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	
	BF904	500 K/W
	BF904R	550 K/W

Note

1. Device mounted on a printed-circuit board.

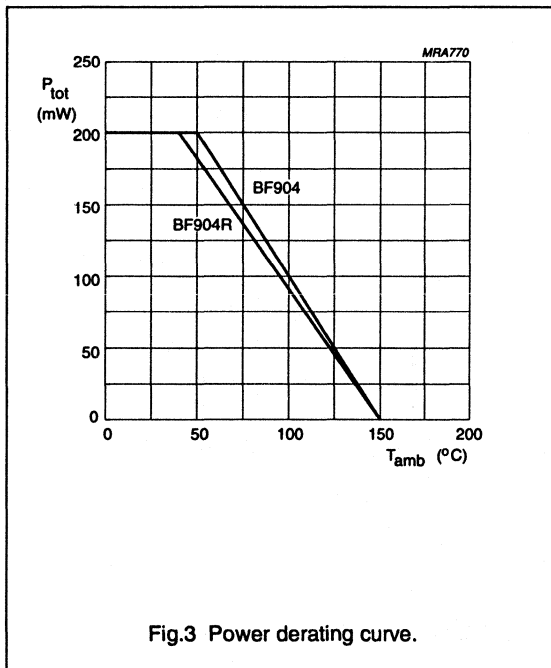
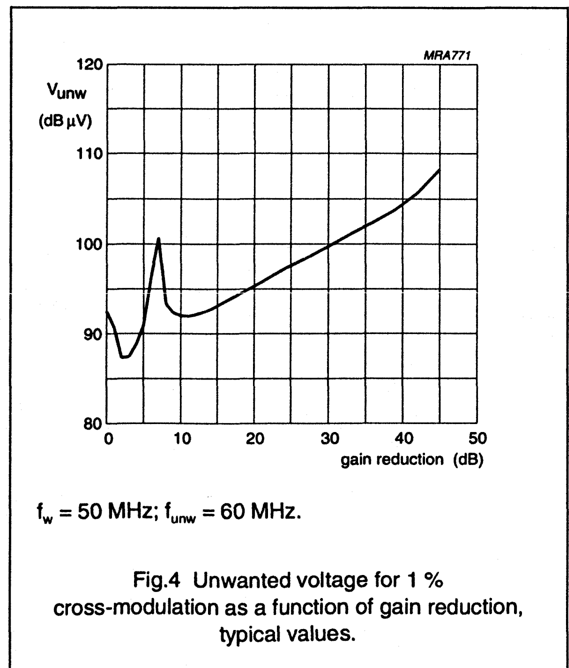


Fig.3 Power derating curve.



f_w = 50 MHz; f_{unw} = 60 MHz.

Fig.4 Unwanted voltage for 1 % cross-modulation as a function of gain reduction, typical values.

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{G1-S}	gate 1 cut-off current	V_{G1-S} = 5 V; $V_{G2-S} = V_{DS}$ = 0	–	50	nA
I_{G2-S}	gate 2 cut-off current	V_{G2-S} = 5 V; $V_{G1-S} = V_{DS}$ = 0	–	50	nA
$V_{(BR)G1-S}$	gate 1-source breakdown voltage	I_{G1-S} = 10 mA; $V_{G2-S} = V_{DS}$ = 0	6	15	V
$V_{(BR)G2-S}$	gate 2-source breakdown voltage	I_{G2-S} = 10 mA; $V_{G1-S} = V_{DS}$ = 0	6	15	V
$V_{(F)S-G1}$	source-gate 1 forward voltage	I_{S-G1} = 10 mA; $V_{G2-S} = V_{DS}$ = 0	0.5	1.5	V
$V_{(F)S-G2}$	source-gate 2 forward voltage	I_{S-G2} = 10 mA; $V_{G1-S} = V_{DS}$ = 0	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	I_D = 20 μA; V_{DS} = 5 V; V_{G2-S} = 4 V	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	I_D = 20 μA; V_{DS} = 5 V; V_{G1-S} = 5 V	0.3	1.2	V
I_{DSX}	drain-source cut-off current	V_{DS} = 5 V; V_{G2-S} = 4 V; R_G = 120 kΩ (note 1)	8	13	mA

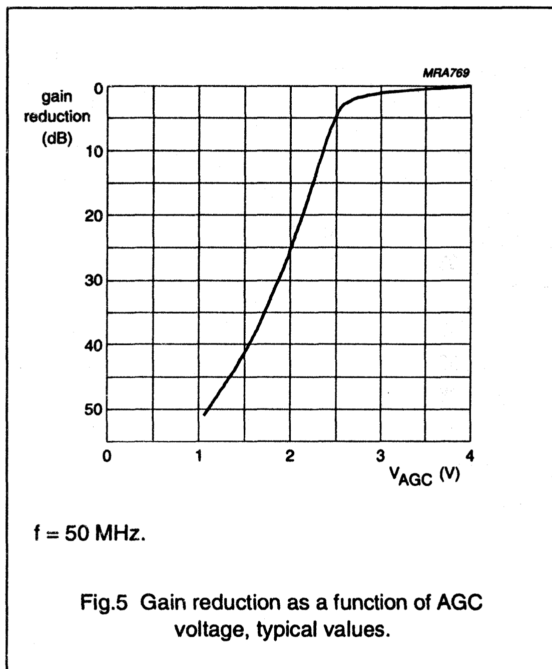
Note

1. R_G connects gate 1 to 5 V.

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 5 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Y_{fs}\|$	transfer admittance	pulsed; T_j = 25 °C	22	25	30	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	1	1.5	2	pF
C_{os}	output capacitance	f = 1 MHz	1	1.3	1.6	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{opt.}$	–	1	1.5	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{opt.}$	–	2	2.8	dB



f = 50 MHz.

Fig.5 Gain reduction as a function of AGC voltage, typical values.

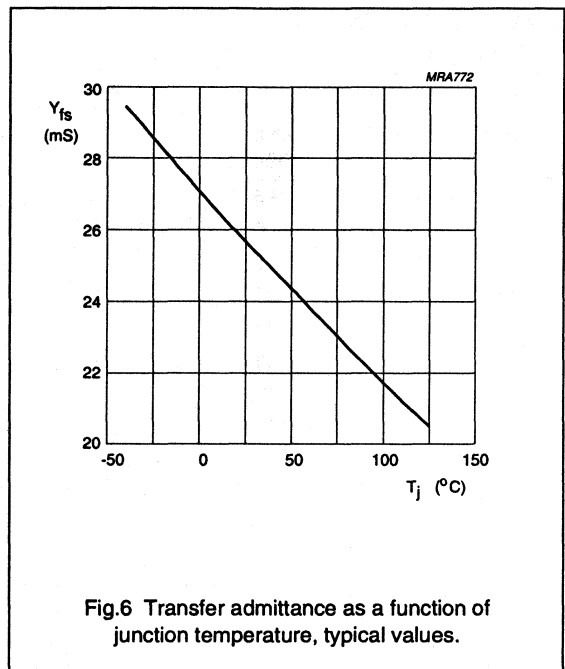


Fig.6 Transfer admittance as a function of junction temperature, typical values.

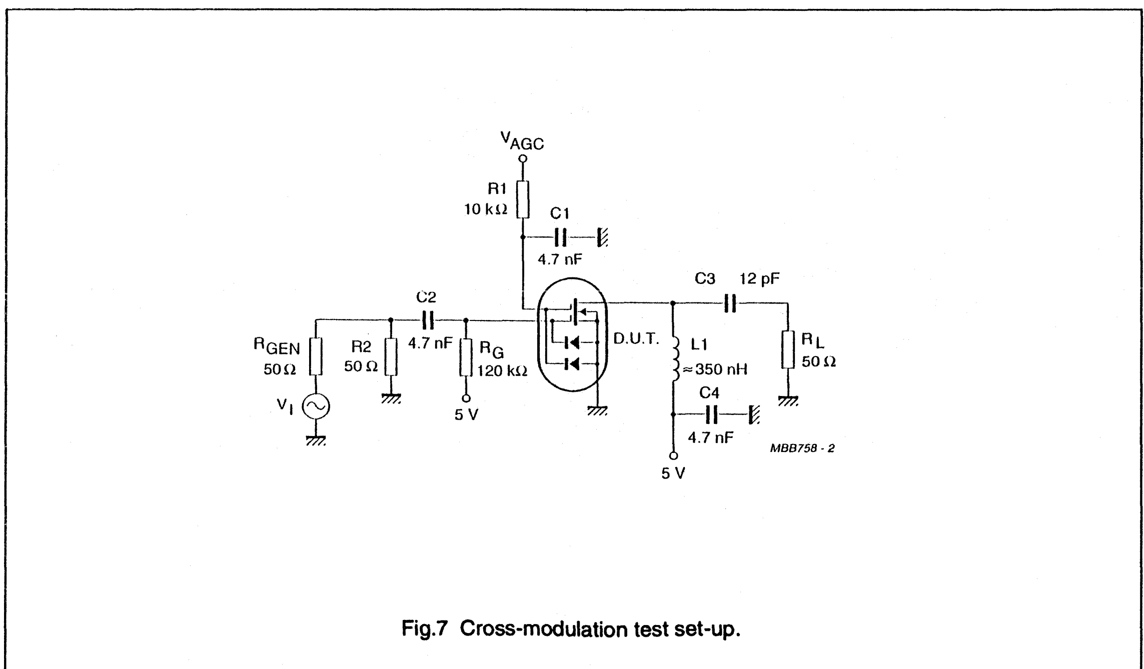


Fig.7 Cross-modulation test set-up.

Table 1 Scattering parameters.
V_{DS} = 5 V; I_D = 10 mA; V_{G2-S} = 4 V; R_{G1} = 120 KΩ.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)
40	0.989	−3.4	2.420	175.7	0.000	79.9	0.993	−1.6
100	0.985	−8.3	2.414	169.1	0.001	78.3	0.992	−3.9
200	0.976	−16.4	2.368	158.8	0.003	80.3	0.987	−7.8
300	0.958	−24.1	2.301	148.5	0.004	73.7	0.980	−11.4
400	0.942	−32.0	2.251	138.8	0.005	70.7	0.974	−15.2
500	0.918	−39.3	2.170	129.5	0.005	67.2	0.966	−18.7
600	0.899	−46.0	2.080	120.7	0.005	67.8	0.958	−22.2
700	0.876	−52.6	2.001	112.1	0.005	68.6	0.951	−25.5
800	0.852	−58.8	1.924	103.2	0.005	72.9	0.944	−28.9
900	0.823	−64.9	1.829	94.7	0.005	78.7	0.937	−32.1
1000	0.800	−70.9	1.747	86.5	0.005	88.3	0.933	−35.2
1200	0.750	−82.4	1.621	70.7	0.005	120.5	0.928	−41.7
1400	0.719	−92.7	1.535	54.6	0.008	139.8	0.930	−48.4
1600	0.682	−102.5	1.424	39.4	0.010	137.8	0.924	−54.9
1800	0.642	−109.8	1.349	22.5	0.013	156.8	0.928	−62.9
2000	0.602	−116.5	1.283	1.1	0.018	175.1	0.928	−73.1
2200	0.547	−124.9	1.130	−15.1	0.014	172.6	0.887	−81.0
2400	0.596	−128.7	1.018	−49.1	0.040	−163.9	0.837	−95.8
2600	0.682	−132.6	0.979	−79.4	0.077	−164.0	0.778	−109.6
2800	0.771	−142.5	0.804	−116.2	0.120	178.8	0.629	−119.5
3000	0.793	−157.5	0.541	−153.5	0.149	158.3	0.479	−119.9

Table 2 Noise data.
V_{DS} = 5 V; I_D = 10 mA; V_{G2-S} = 4 V; R_{G1} = 120 KΩ.

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n
		(RAT)	(DEG)	
800	2.00	0.686	49.6	50.40

Dual gate MOS-FETs

BF908; BF908R

FEATURES

- High $|Y_{fs}|$ dual gate MOS-FET
- Short channel transistor with high $|Y_{fs}| : C_{is}$ ratio
- Low noise gain-controlled amplifier to 1 GHz

DESCRIPTION

Depletion type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes. They are intended for UHF and VHF applications with 12 V supply voltage such as television tuners and professional communications equipment. These transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	–	12	V
I_D	drain current	–	–	40	mA
P_{tot}	total power dissipation	–	–	200	mW
T_j	junction temperature	–	–	150	°C
$\|Y_{fs}\|$	transfer admittance	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	2.4	3.1	4	pF
C_{rs}	feedback capacitance	20	30	45	pF
F	noise figure at 800 MHz	–	1.5	2.5	dB

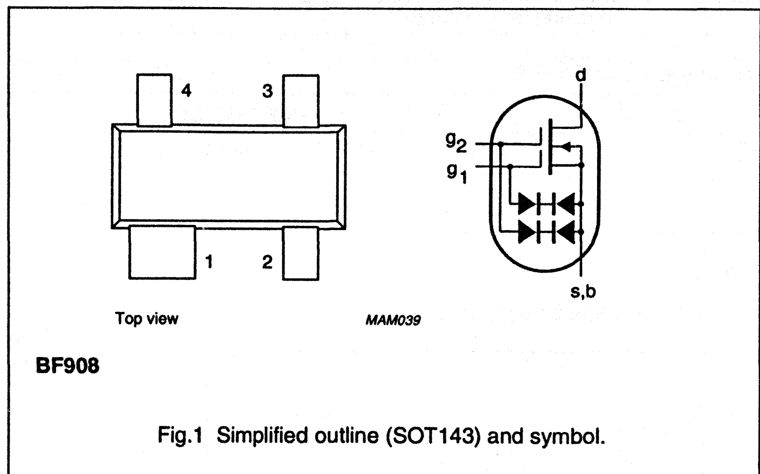


Fig.1 Simplified outline (SOT143) and symbol.

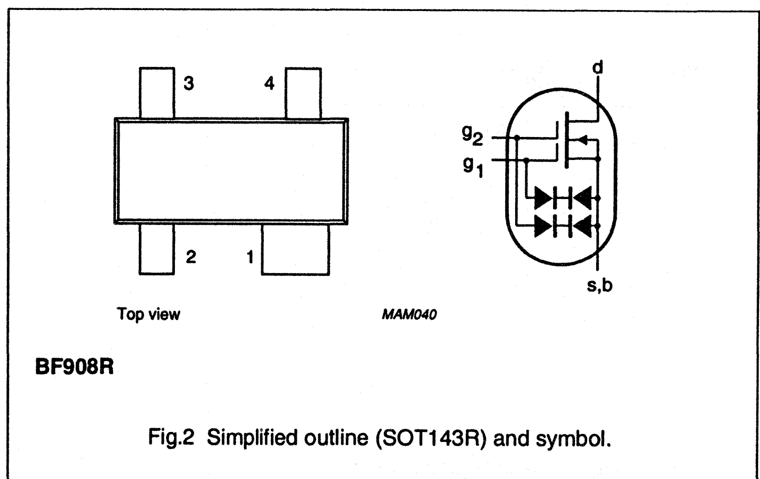


Fig.2 Simplified outline (SOT143R) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	DC drain current		–	40	mA
$\pm I_{G1-S}$	gate 1-source current		–	10	mA
$\pm I_{G2-S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation				
	BF908	up to T_{amb} = 50 °C (note 1)	–	200	mW
	BF908R	up to T_{amb} = 40 °C (note 1)	–	200	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient (note 1)	
	BF908	500 K/W
	BF908R	550 K/W

Note

1. Device mounted on a printed-circuit board.

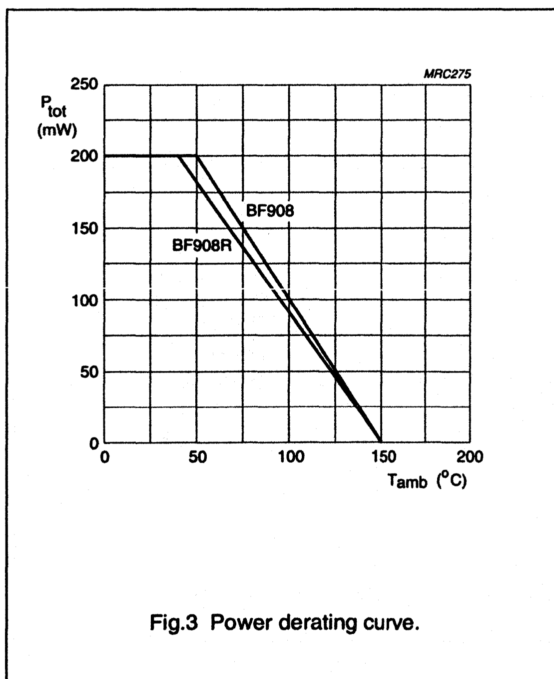


Fig.3 Power derating curve.

STATIC CHARACTERISTICS

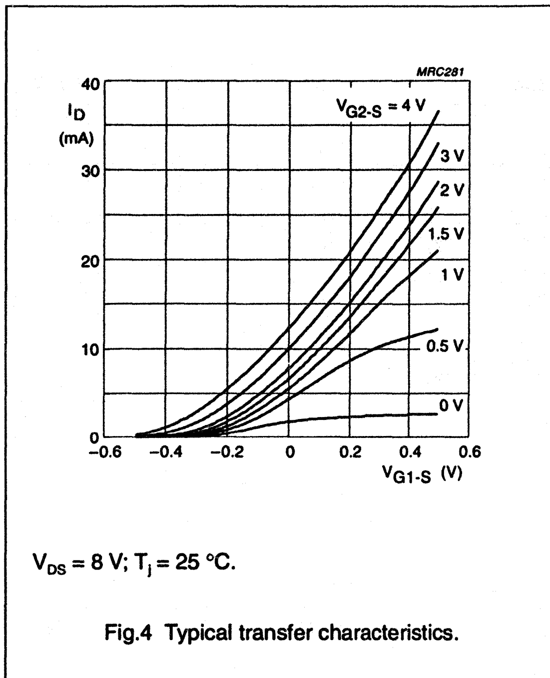
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm I_{G1-S}$	gate 1 cut-off current	V_{G1-S} = 5 V; $V_{G2-S} = V_{DS}$ = 0	–	–	50	nA
$\pm I_{G2-S}$	gate 2 cut-off current	V_{G2-S} = 5 V; $V_{G1-S} = V_{DS}$ = 0	–	–	50	nA
$V_{(BR)G1-S}$	gate 1-source breakdown voltage	I_{G1-S} = 10 mA; $V_{G2-S} = V_{DS}$ = 0	8	–	20	V
$V_{(BR)G2-S}$	gate 2-source breakdown voltage	I_{G2-S} = 10 mA; $V_{G1-S} = V_{DS}$ = 0	8	–	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 μA; V_{DS} = 8 V; V_{G2-S} = 4 V	–	–	2	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 μA; V_{DS} = 8 V; V_{G1-S} = 4 V	–	–	1.5	V
I_{DSS}	drain current	V_{DS} = 8 V; V_{G1-S} = 0; V_{G2-S} = 4 V	3	15	27	mA

DYNAMIC CHARACTERISTICS

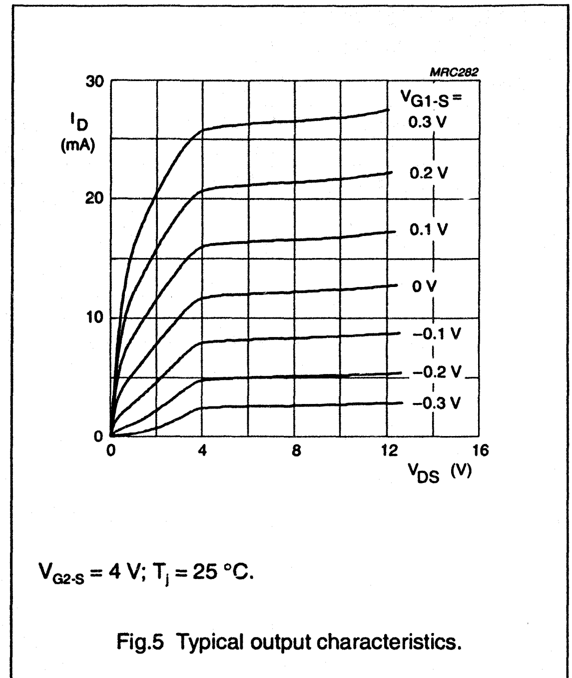
Measuring conditions (common source): I_D = 15 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	pulsed; T_j = 25 °C; f = 1 kHz	36	43	50	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	2.4	3.1	4	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	1.2	1.8	2.5	pF
C_{os}	output capacitance	f = 1 MHz	1.2	1.7	2.2	pF
C_{rs}	feedback capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt.}$	–	0.6	1.2	dB
		f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt.}$	–	1.5	2.5	dB



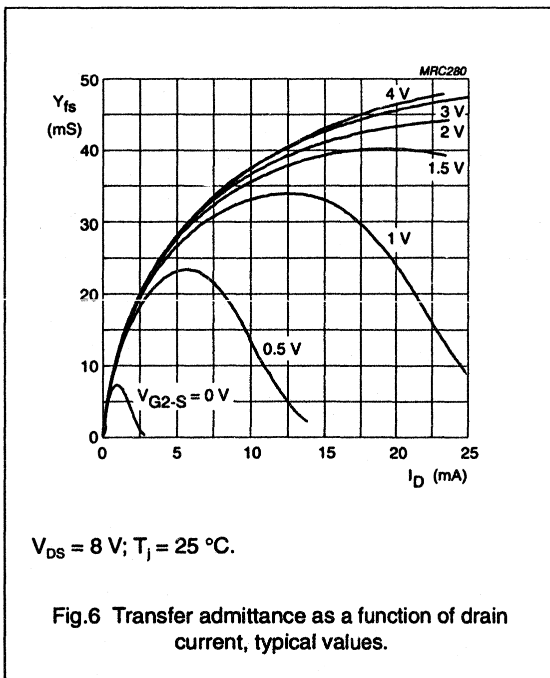
V_{DS} = 8 V; T_j = 25 °C.

Fig.4 Typical transfer characteristics.



V_{G2-S} = 4 V; T_j = 25 °C.

Fig.5 Typical output characteristics.



V_{DS} = 8 V; T_j = 25 °C.

Fig.6 Transfer admittance as a function of drain current, typical values.

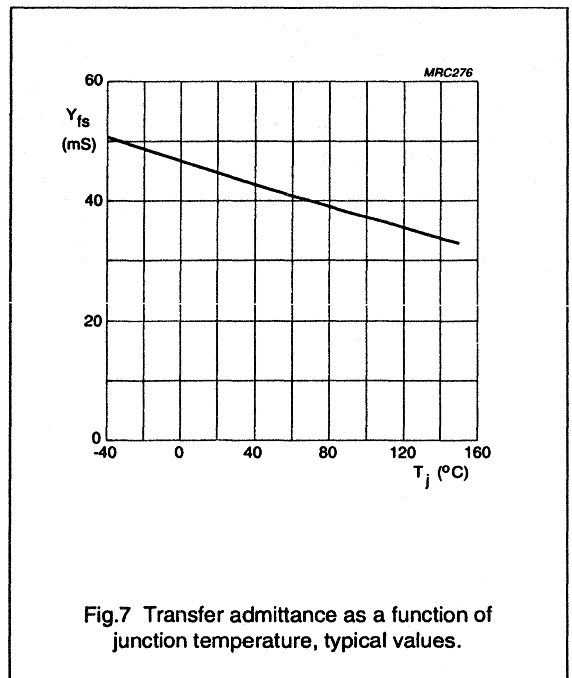


Fig.7 Transfer admittance as a function of junction temperature, typical values.

Table 1 Scattering parameters.
I_D = 10 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)
50	0.998	−5.1	3.537	173.5	0.001	98.2	0.996	−2.4
100	0.994	−10.4	3.502	167.7	0.001	88.8	0.994	−4.9
200	0.979	−20.8	3.450	154.9	0.003	74.6	0.987	−9.5
300	0.962	−30.3	3.318	143.7	0.004	69.5	0.983	−13.9
400	0.939	−40.1	3.234	131.9	0.005	65.6	0.980	−18.5
500	0.914	−49.1	3.093	120.7	0.006	64.4	0.974	−22.8
600	0.892	−57.1	2.912	111.1	0.005	63.1	0.969	−27.0
700	0.865	−64.4	2.774	101.0	0.005	65.2	0.966	−31.2
800	0.837	−71.6	2.616	91.4	0.004	70.8	0.965	−35.4
900	0.811	−78.1	2.479	81.9	0.004	87.4	0.965	−39.4
1000	0.785	−84.5	2.329	72.5	0.003	108.0	0.966	−43.7

Table 2 Noise data.
I_D = 10 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n
		(RAT)	(DEG)	
800	1.50	0.720	56.7	0.580

Table 3 Scattering parameters.
I_D = 15 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)
50	0.998	−5.3	3.983	173.4	0.001	95.5	0.994	−2.4
100	0.994	−10.9	3.943	167.5	0.001	93.6	0.991	−5.0
200	0.976	−21.6	3.878	154.7	0.003	74.3	0.984	−9.7
300	0.957	−31.7	3.722	143.3	0.004	70.0	0.979	−14.2
400	0.934	−41.7	3.614	131.6	0.005	63.5	0.975	−18.8
500	0.907	−51.1	3.446	120.4	0.006	62.2	0.969	−23.2
600	0.885	−59.1	3.240	110.9	0.005	59.6	0.964	−27.4
700	0.851	−66.8	3.072	100.9	0.005	64.8	0.961	−31.6
800	0.826	−73.9	2.891	91.3	0.004	67.8	0.959	−35.9
900	0.797	−80.7	2.733	81.9	0.004	85.0	0.958	−40.0
1000	0.773	−87.0	2.569	72.8	0.004	102.9	0.958	−44.2

Table 4 Noise data.
I_D = 15 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n
		(RAT)	(DEG)	
800	1.50	0.700	59.2	0.520

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\|y_{fs}\|$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 800 MHz	F	typ.	2.8 dB

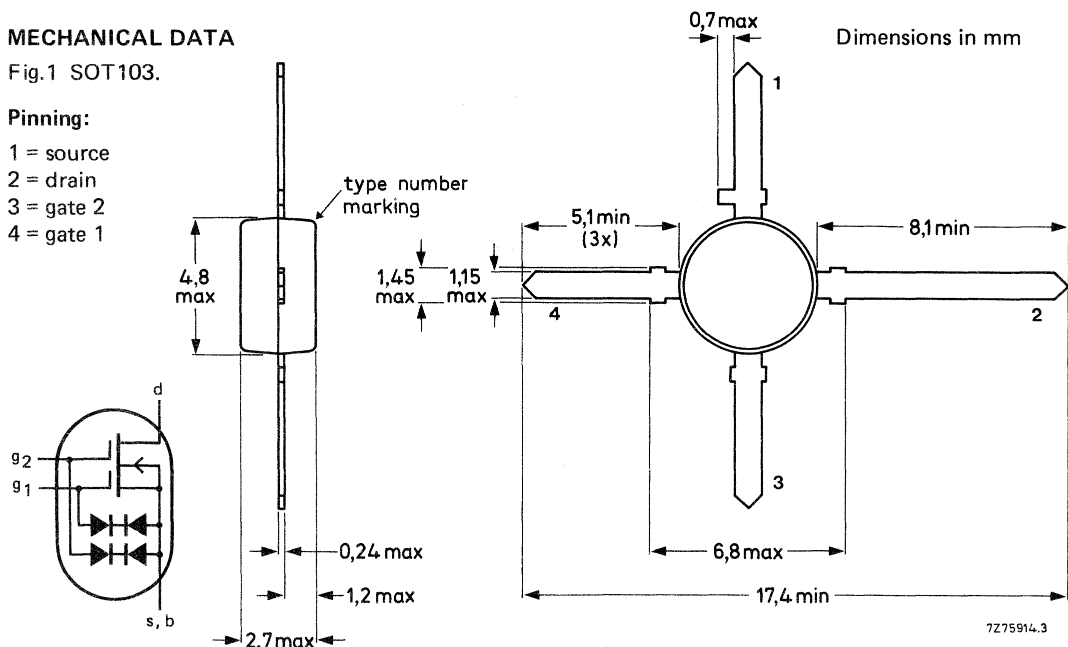
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

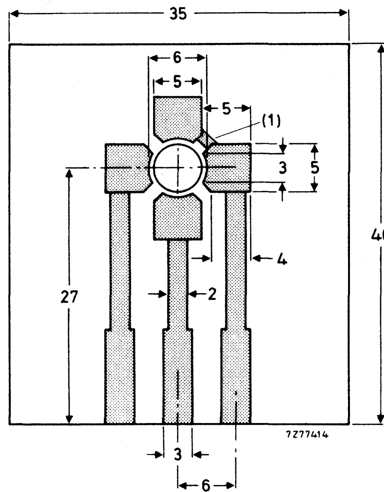
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board	$R_{th\ j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	25 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		2 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.7 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	9.5 mS
		typ.	12 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1.8 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9 pF
Noise figure at G_S = 2 mS; $B_S = B_S$ opt			
f = 200 MHz	F	typ.	1.6 dB
f = 800 MHz	F	typ.	2.8 dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt			
G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	23 dB
G_L = 1 mS; $B_L = B_L$ opt; f = 800 MHz	G_p	typ.	16.5 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications in television tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\|y_{fs}\|$	typ.	18	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 3.0	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0	dB

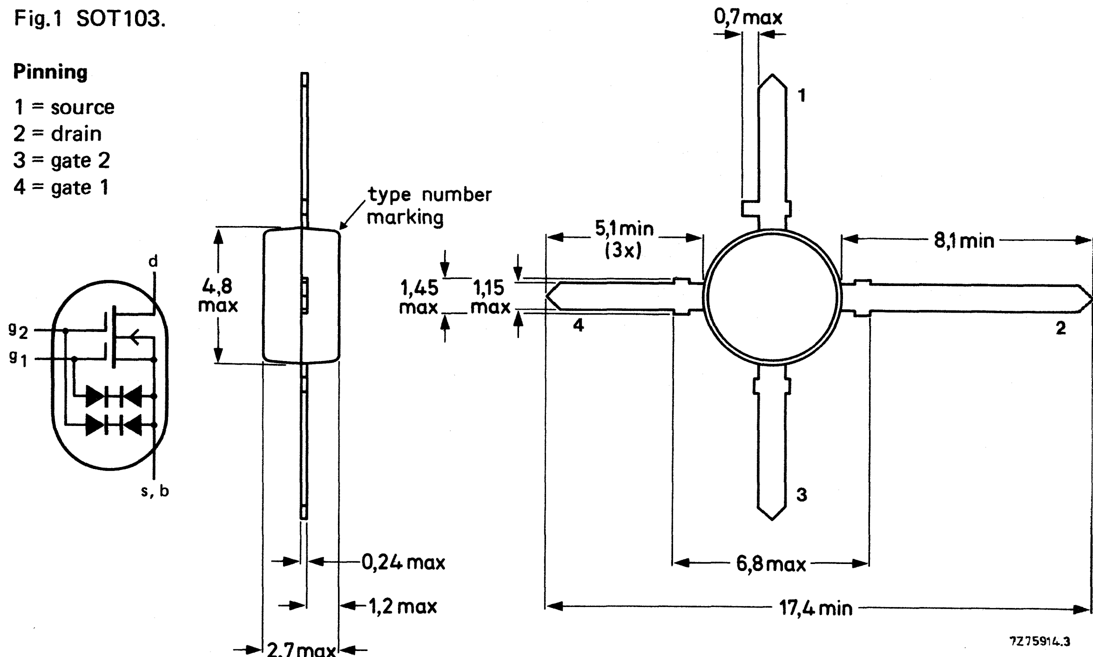
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

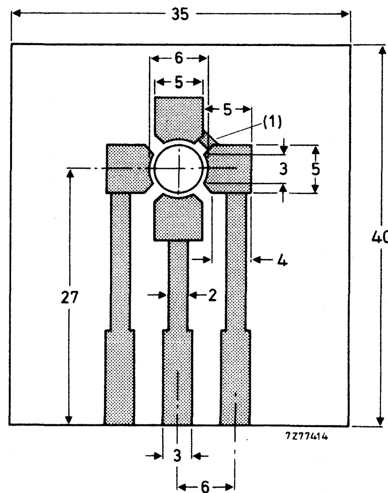
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2) $R_{th\,j\text{-}a}$ = 335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6.0 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6.0 to 20 V
Drain current			
$V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
$I_D = 20\ \mu A$; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	max.	2.5 V
$I_D = 20\ \mu A$; $V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2.5 pF
		max.	3.0 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at $G_S = 2$ mS ; $B_S = B_S$ opt f = 200 MHz	F	typ.	1.0 dB
Power gain at $G_S = 2$ mS ; $B_S = B_S$ opt $G_L = 0.5$ mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

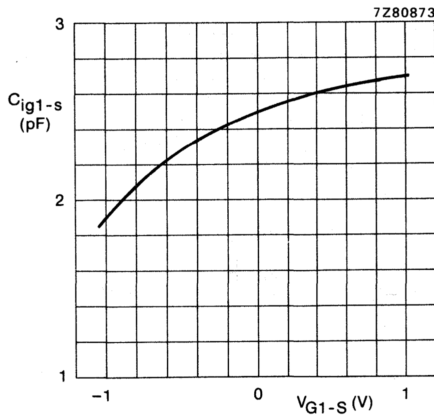


Fig. 3 V_{G2-S} = 4 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

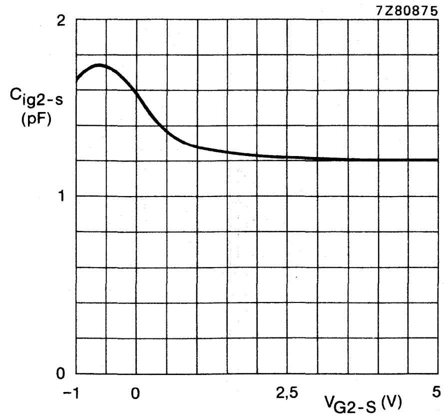


Fig. 4 V_{G1-S} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

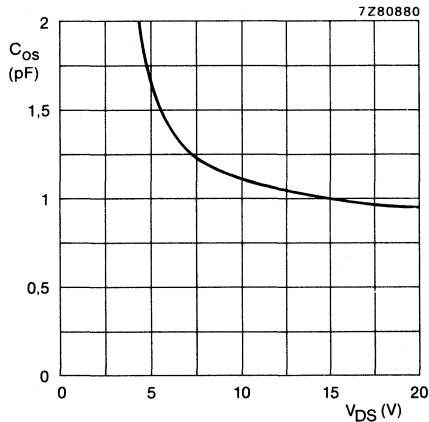


Fig. 5 V_{G2-S} = 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C; typical values.

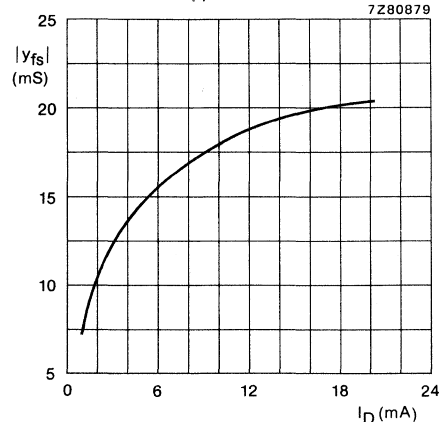


Fig. 6 V_{G2-S} = 4; V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

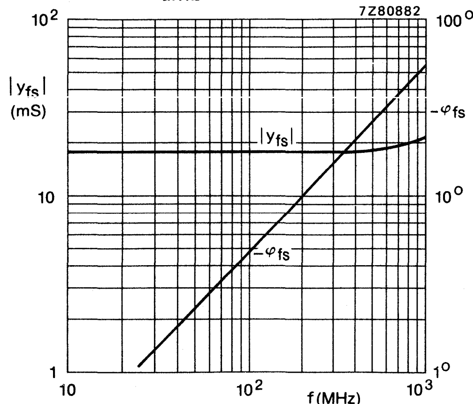


Fig. 7 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

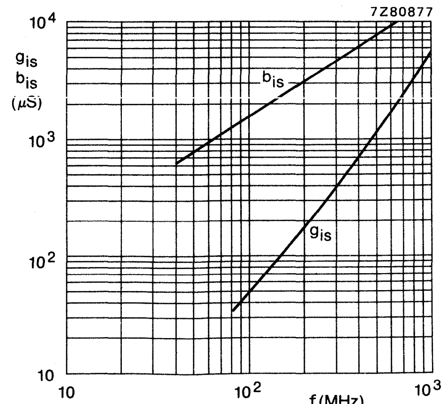


Fig. 8 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

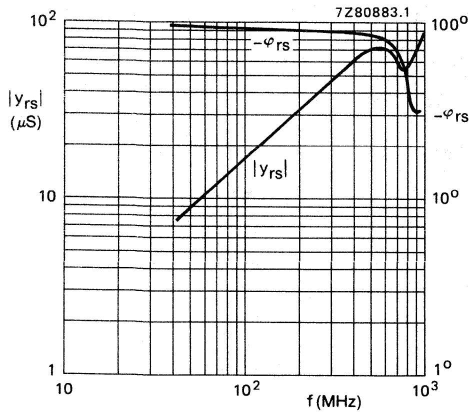


Fig. 9 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

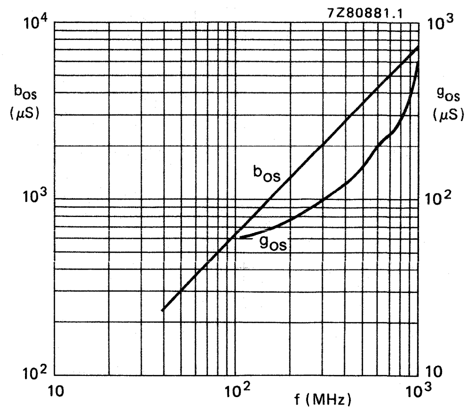


Fig. 10 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

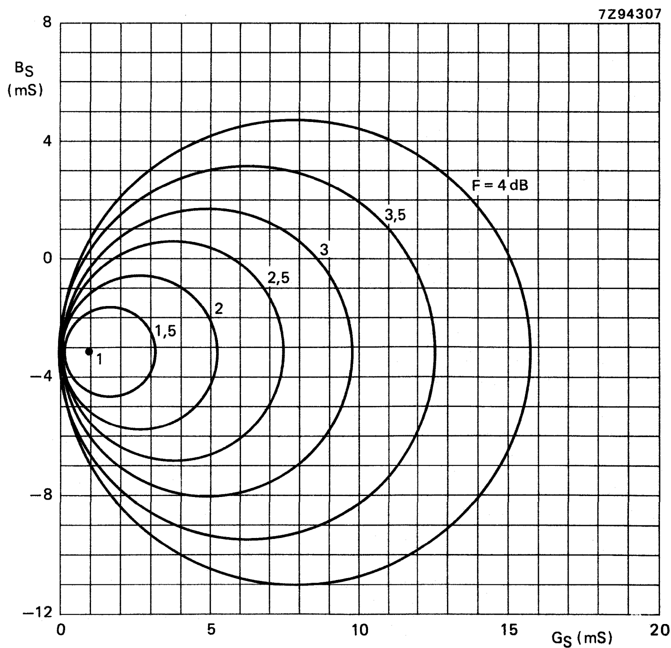


Fig. 11 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with large tuning ranges up to 500 MHz.

QUICK REFERENCE DATA

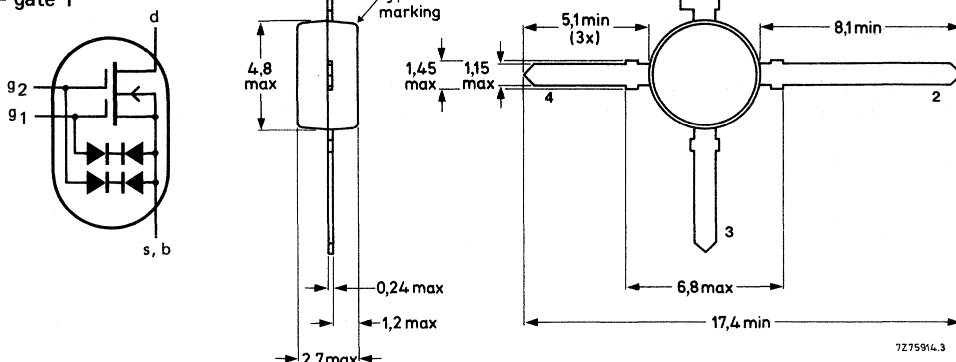
Parameter	Symbol		Value
Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_{Sopt} I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,0 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT103.

Pinning
1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

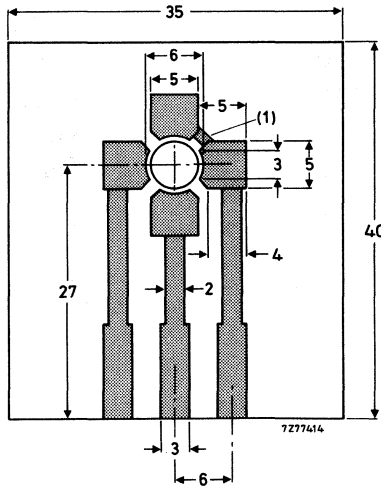
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-current (DC or average)	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on a printed-circuit board (see Fig. 2)	$R_{th\ j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless stated otherwise

Gate cut-off currents			
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	<	50 nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	<	50 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		6,0 to 20 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		6,0 to 20 V
Drain current V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		2,0 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	<	2,5 V
I_D = 20 μA; V_{DS} = 15 V; + V_{G1-S} = 0	$-V_{(P)G2-S}$	<	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA;
V_{DS} = 15 V; V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	> typ.	15 mS 18 mS
Input capacitance at gate 1 at f = 1 MHz	C_{ig1-s}	typ.	2,5 pF
Input capacitance at gate 2 at f = 1 MHz	C_{ig2-s}	typ.	1,2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0 pF
Noise figure at G_S = 2 mS; $B_S = B_{Sopt}$ and f = 200 MHz	F	typ.	1,0 dB
Power gain at G_S = 2 mS; $B_S = B_{Sopt}$ G_L = 0,5 mS; $B_L = B_{Lopt}$; f = 200 MHz	G_P	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 pF 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 3.3 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	1.8 dB

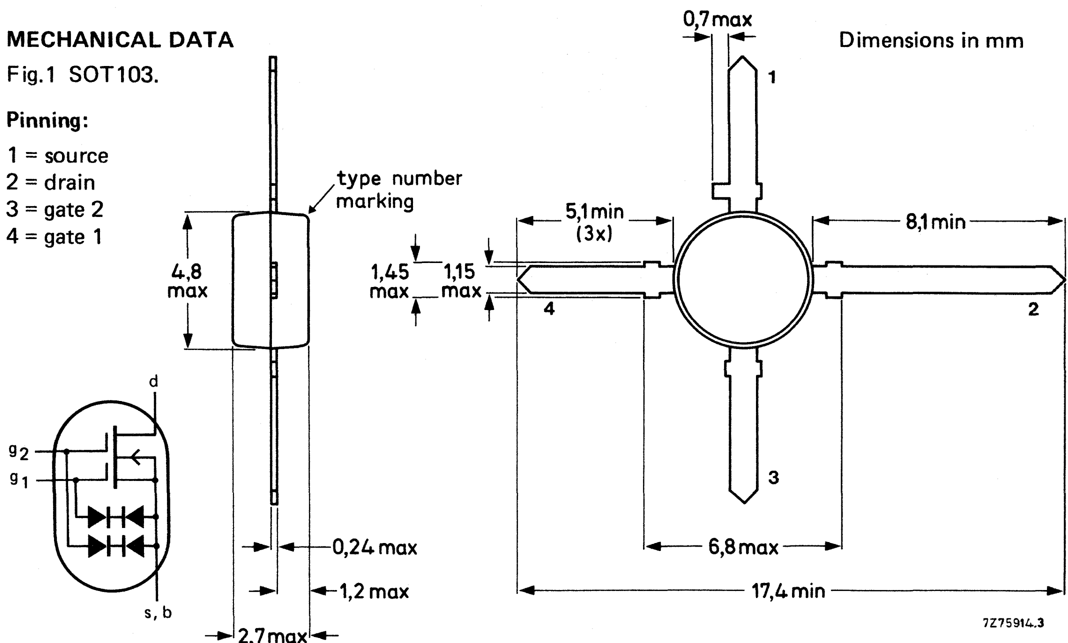
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



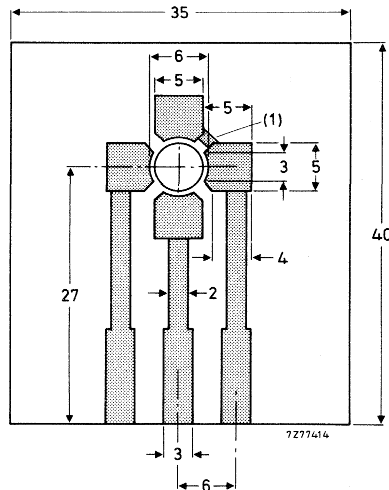
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig.2) $R_{th\ j\text{-}a}$ = 335 K/W



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2.3 pF
		max.	2.6 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.1 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8 pF
Noise figure			
f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0 dB
f = 800 MHz; G_S = 3.3 mS; $B_S = B_S$ opt	F	typ.	1.8 dB
Power gain			
f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS; B_S = opt; B_L = opt	G_p	typ.	25 dB
f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS; B_S = opt; B_L = opt	G_p	typ.	18 dB

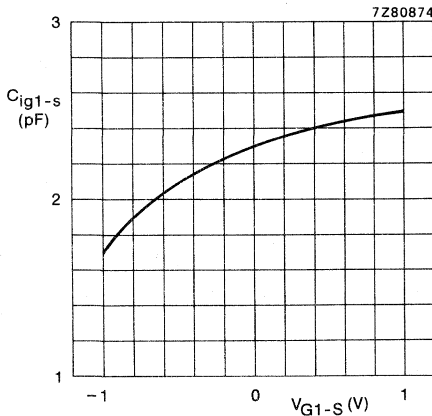


Fig.3 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

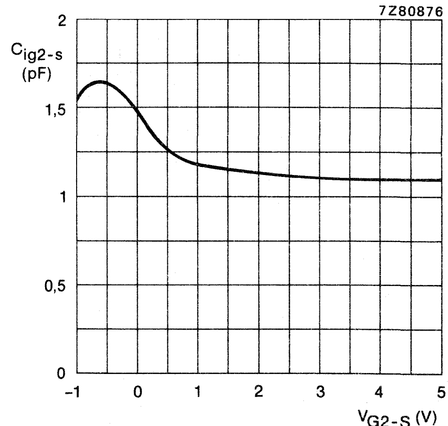


Fig.4 $V_{G1\text{-}S}$ = 0 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

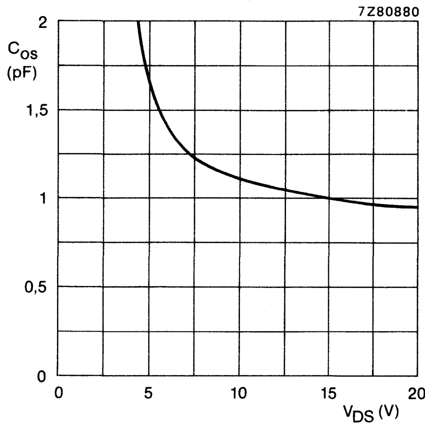


Fig. 5 $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C; typical values.

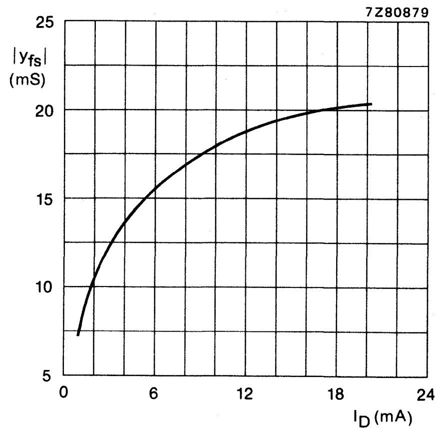


Fig. 6 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

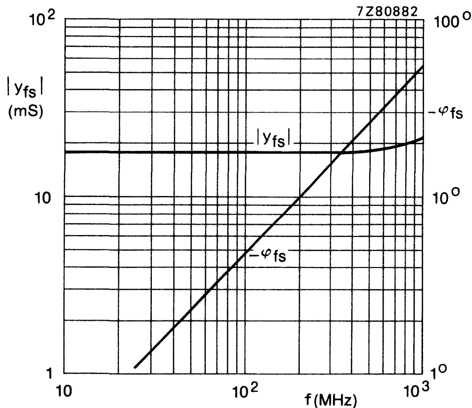


Fig. 7 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

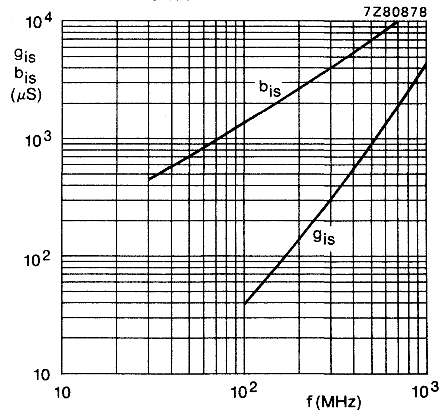


Fig. 8 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

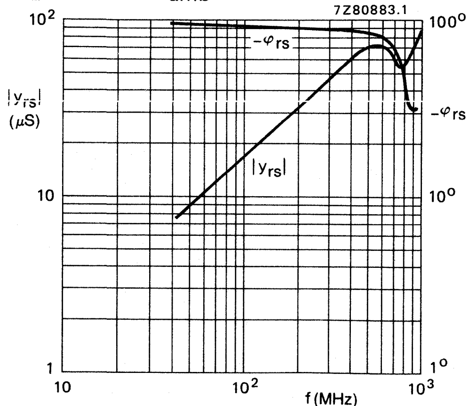


Fig. 9 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

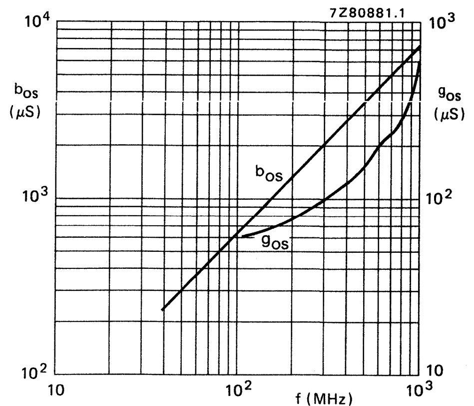


Fig. 10 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

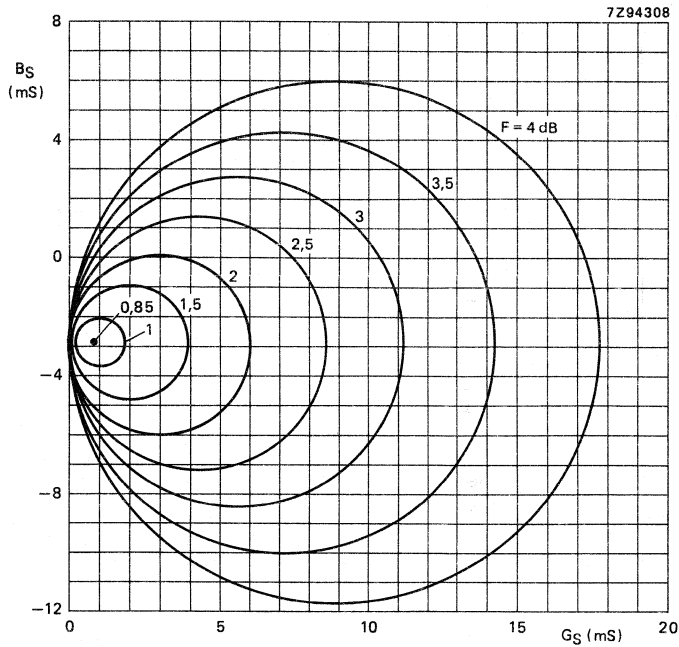


Fig. 11 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; typical values.

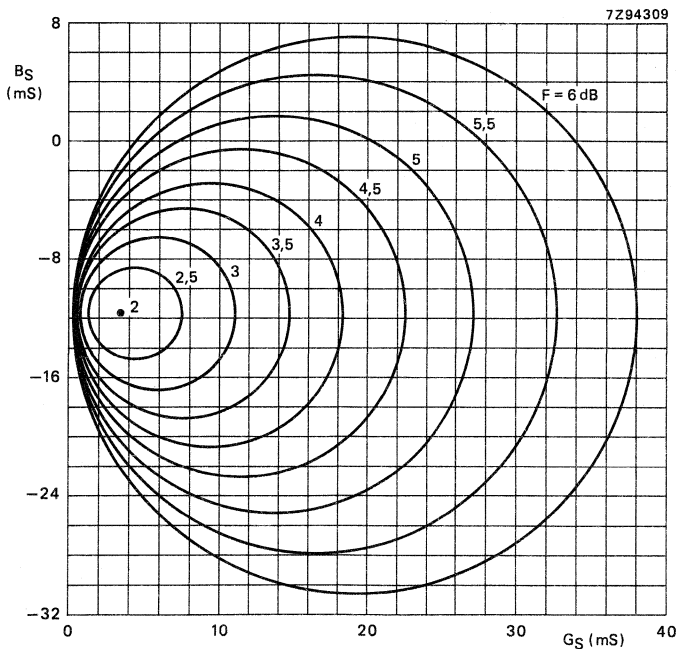


Fig. 12 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 800 MHz; T_{amb} = 25 °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected. Intended for UHF applications, such as UHF television tuners, with 12 V supply voltage and professional communication equipment.
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	18	V
Drain current (DC)	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\|y_{fs}\|$	typ.	19	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. max.	2.6 3.0	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 5 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 800 MHz	F	typ.	2.0	dB

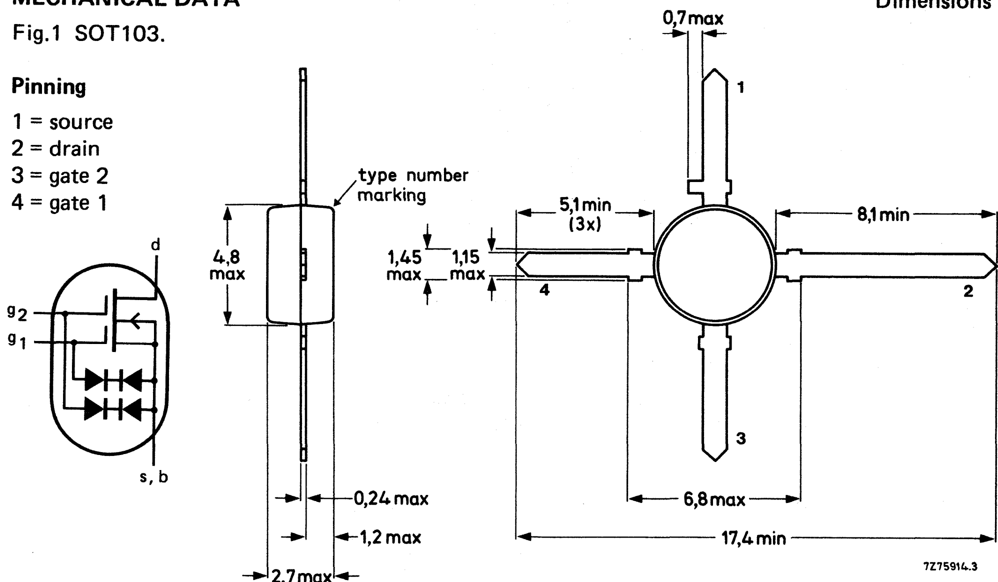
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

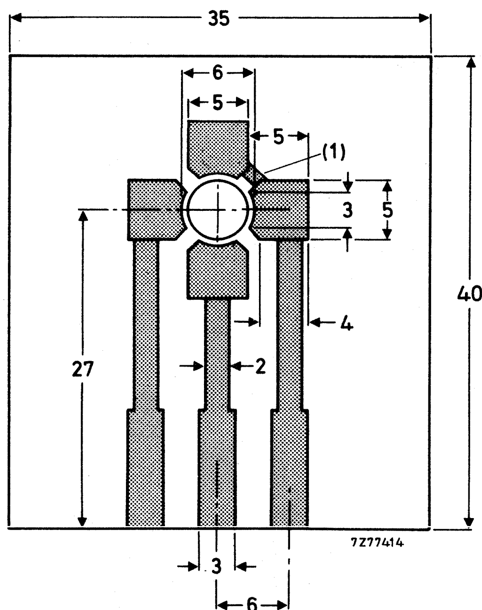
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\ j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
± V_{G1-S} = 7 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	max.	25 nA
± V_{G2-S} = 7 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	max.	25 nA
Gate-source breakdown voltages			
± I_{G1-SS} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		8 to 20 V
± I_{G2-SS} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	min.	0.2 V
		max.	1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	min.	0.2 V
		max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	18 mS
		typ.	19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2.6 pF
		max.	3.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
		max.	35 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.1 pF
Noise figure at f = 800 MHz; G_S = 5 mS; B_S = B_S opt	F	typ.	2.0 dB
		max.	3.0 dB

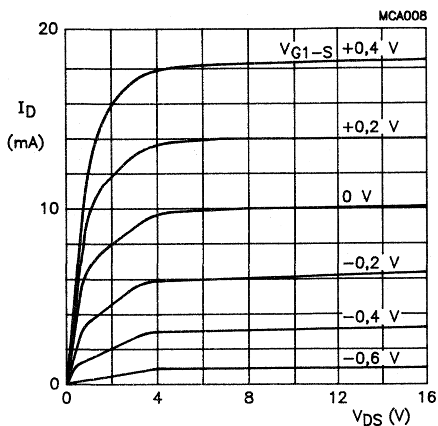


Fig.3 Output characteristics.
$V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

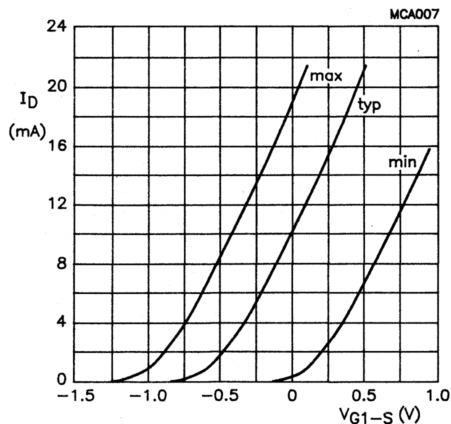


Fig.4 Transfer characteristics.
V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

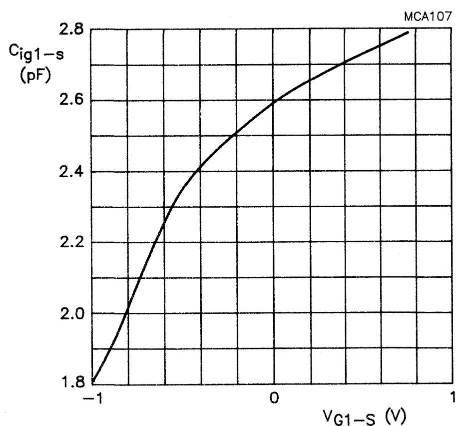


Fig.5 Gate 1 input capacitance as a function of gate 1 source voltage;
f = 1 MHz; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

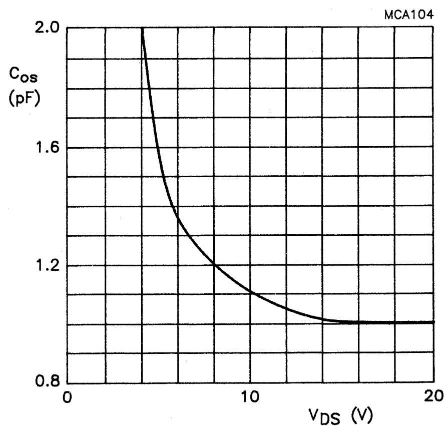


Fig.6 Output capacitance as a function of drain voltage; f = 1 MHz;
I_D = 10 mA; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

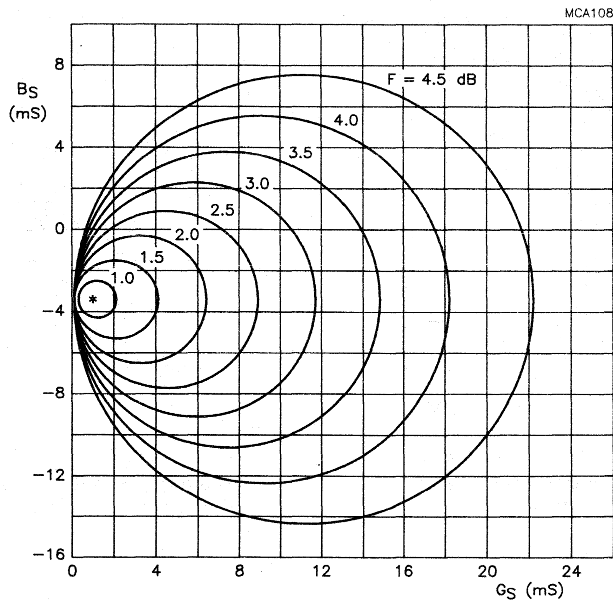


Fig.7 Circles of constant noise figures; f = 200 MHz; T_{amb} = 25 °C; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

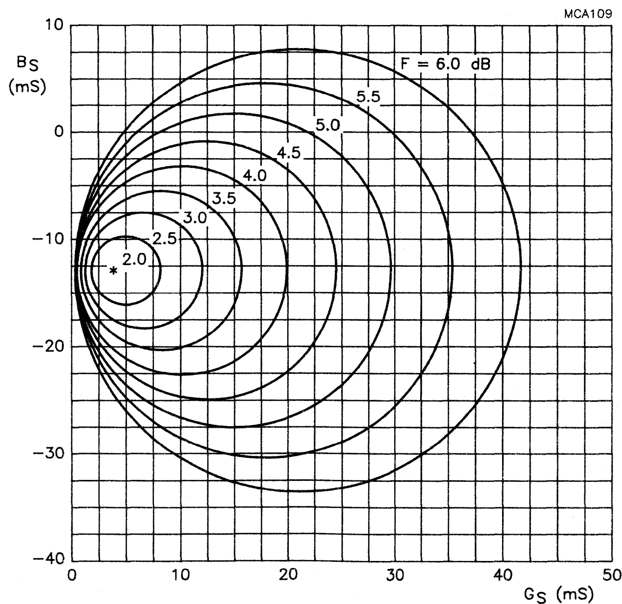


Fig.8 Circles of constant noise figures; f = 800 MHz; T_{amb} = 25 °C; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

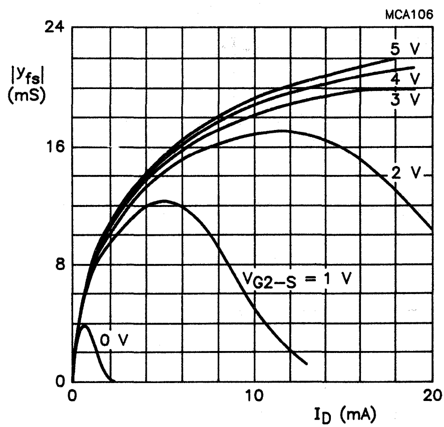


Fig.9 Forward transfer admittance as a function of drain current; f = 1 kHz; V_{DS} = 10 V; T_{amb} = 25 °C.

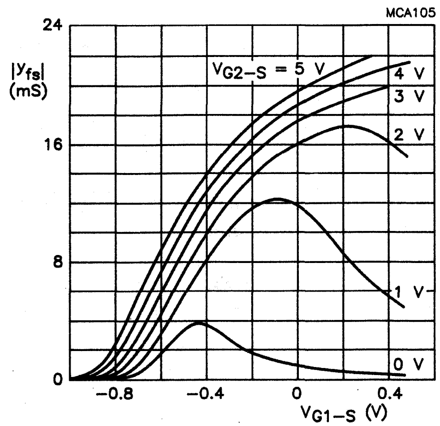


Fig.10 Forward transfer admittance as a function of gate 1 source voltage; f = 1 kHz; V_{DS} = 10 V; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\|y_{fs}\|$	typ.	14	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	2.1	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	0.7	dB

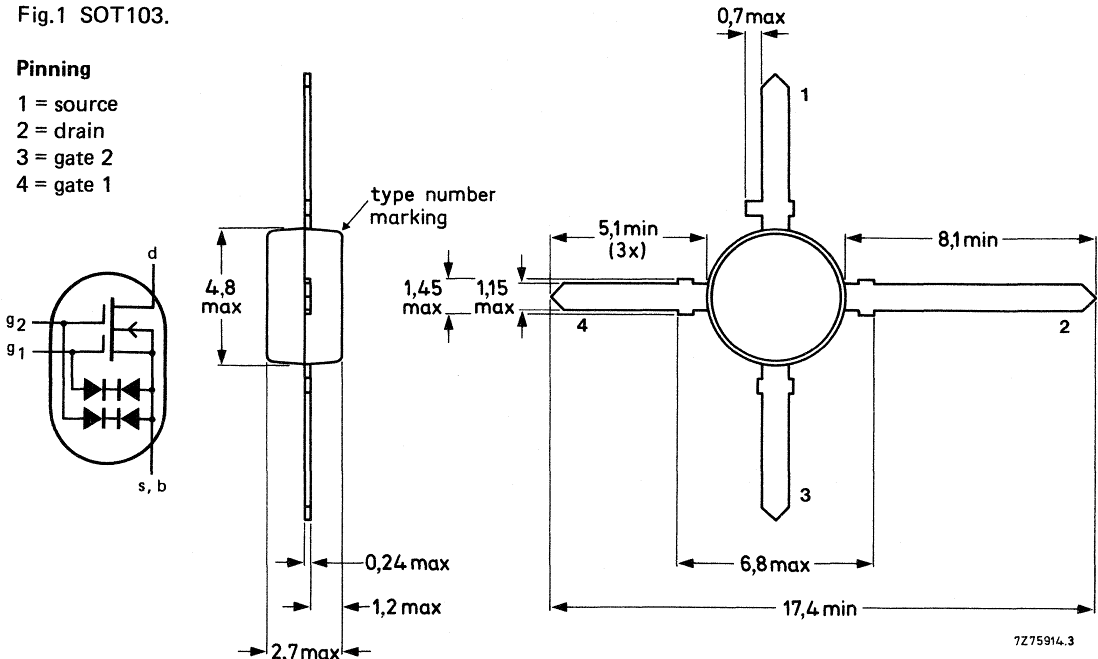
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



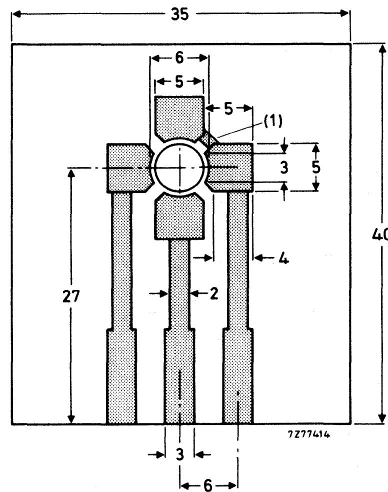
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\,j\text{-}a}$	=	335	K/W



Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 µm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$

Parameter	Symbol		Value
Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	<	25 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	<	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V	I_{DSS}		4 to 25 mA
Gate-source cut-off voltages			
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	<	2.5 V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	<	2.5 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^oC$

Parameter	Symbol		Value
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	10 mS
		typ.	14 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2.1 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.1 pF
Noise figure at f = 100 MHz; $G_S = 1$ mS; $B_S = B_S$ opt	F	typ.	0.7 dB
		<	1.7 dB
Noise figure at f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt	F	typ.	1.0 dB
		<	2.0 dB
Transducer gain at f = 100 MHz; $G_S = 1$ mS; $B_S = B_S$ opt; $G_L = 0.5$ mS; $B_L = B_L$ opt	G_{tr}	typ.	29 dB
Transducer gain at f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt; $G_L = 0.5$ mS; $B_L = B_L$ opt	G_{tr}	typ.	26 dB

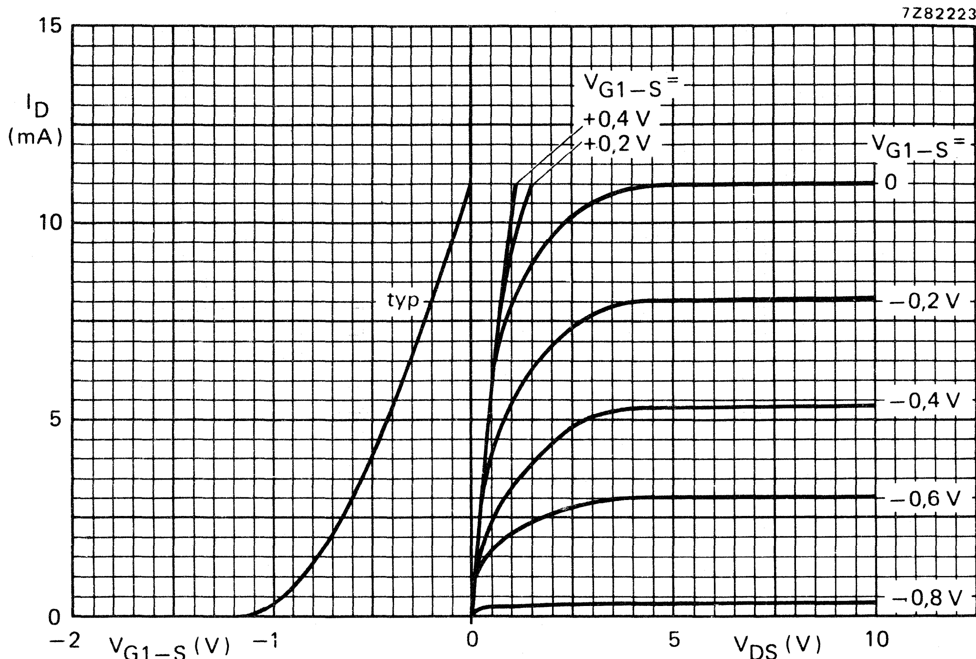


Fig. 3 **Left-hand graph:** V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C. **Right-hand graph:** $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C.

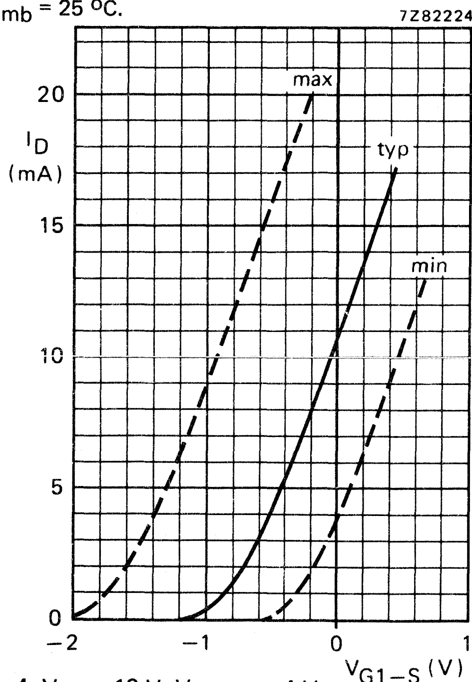


Fig. 4 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C.

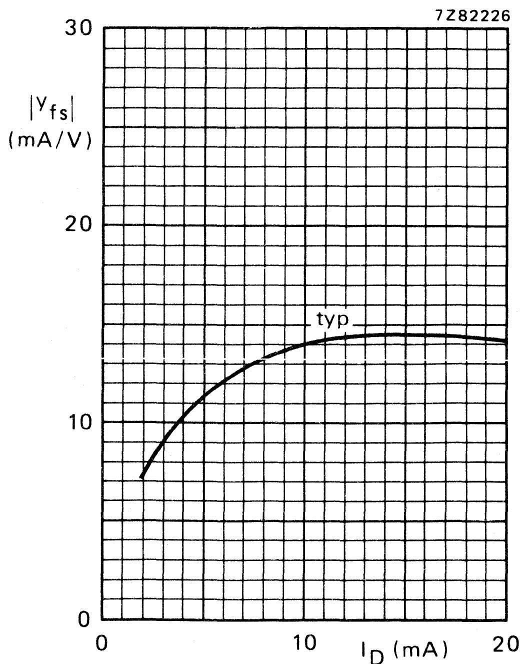


Fig. 5 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; f = 1 kHz; T_{amb} = 25 °C.

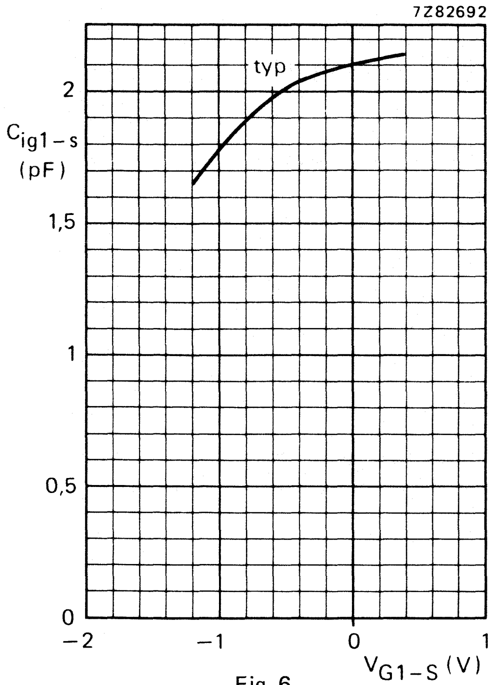


Fig. 6.

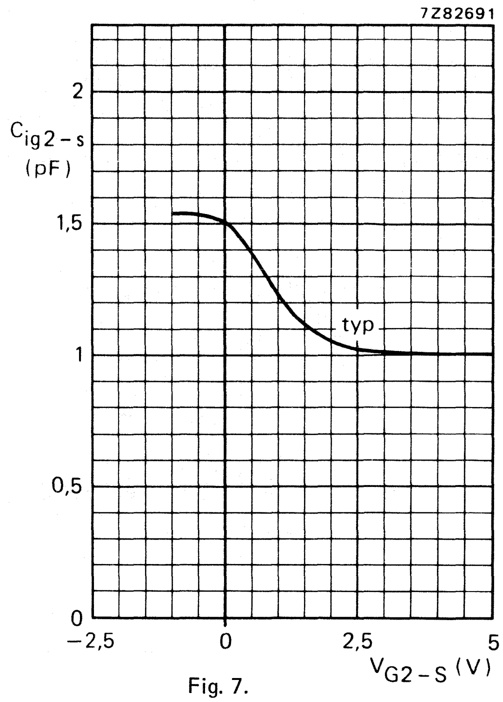


Fig. 7.

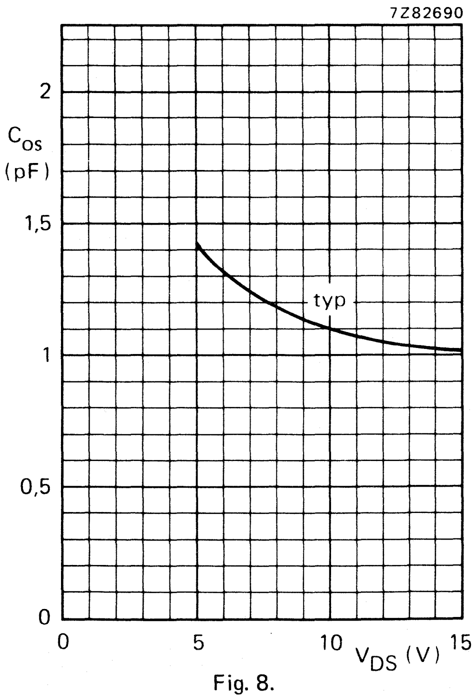


Fig. 8.

Measuring conditions:

Fig. 6 V_{DS} = 10 V; V_{G2-S} = + 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig. 7 V_{DS} = 10 V; V_{G1-S} = 0; f = 1 MHz; T_{amb} = 25 °C.

Fig. 8 V_{G2-S} = + 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C.

Measuring conditions for Figs 9 to 12: V_{DS} = 10 V; I_D = 10 mA; V_{G2-S} = + 4 V; T_{amb} = 25 °C.

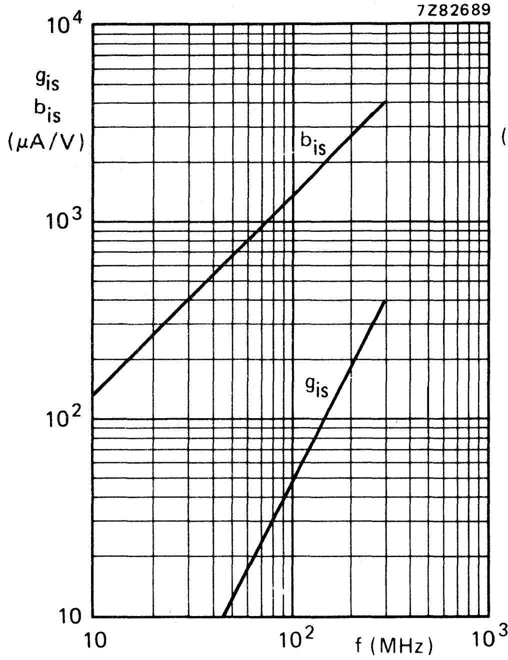


Fig. 9.

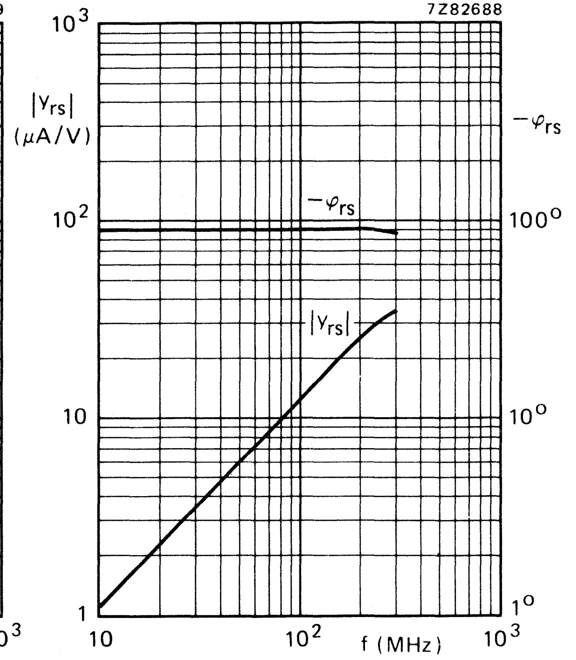


Fig. 10.

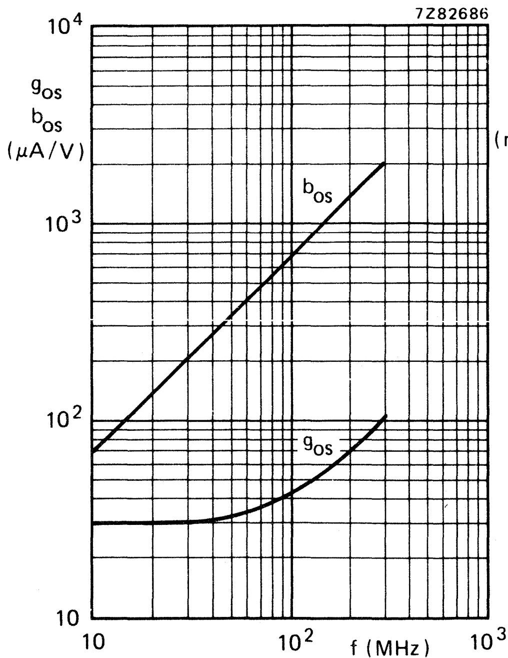


Fig. 11.

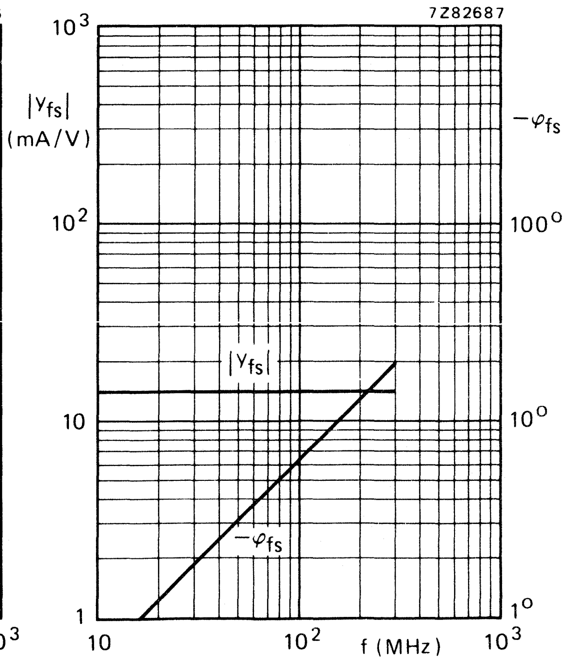


Fig. 12.

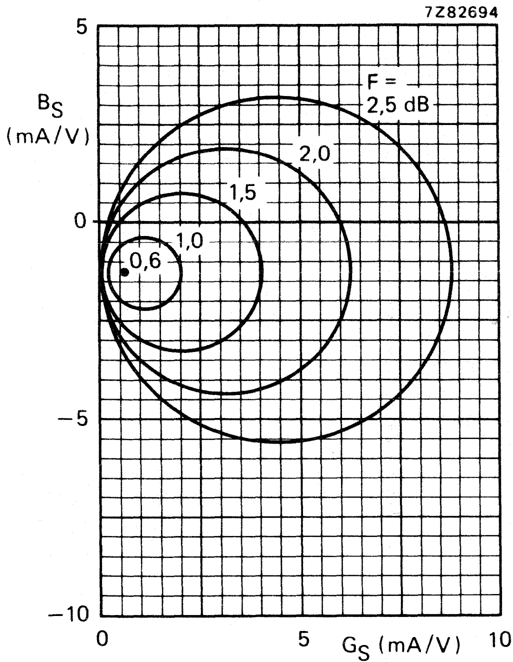


Fig. 13 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 100 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

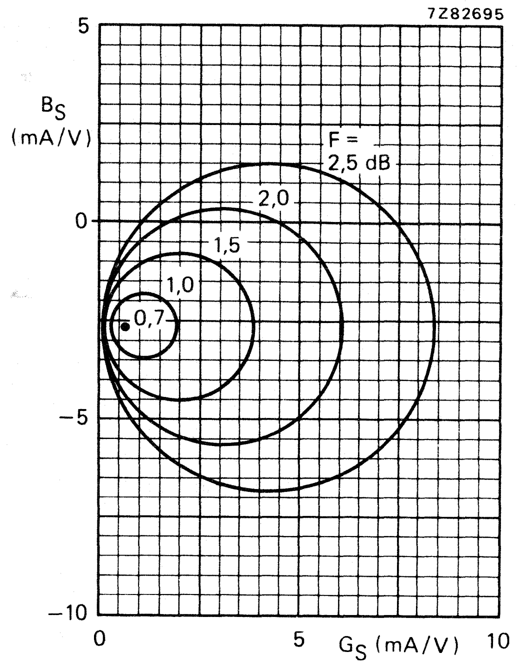


Fig. 14 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

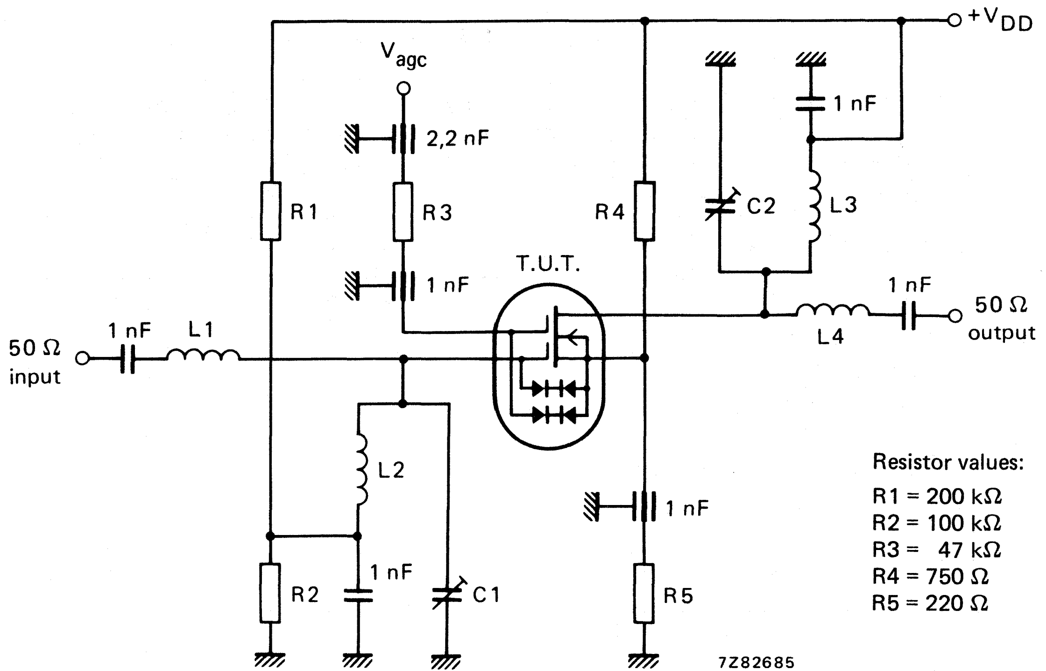


Fig. 15 Automatic gain control test circuit at f = 200 MHz (see also Fig. 16).
V_{DD} = 16 V; G_S = 2 mA/V; G_L = 0,5 mA/V.

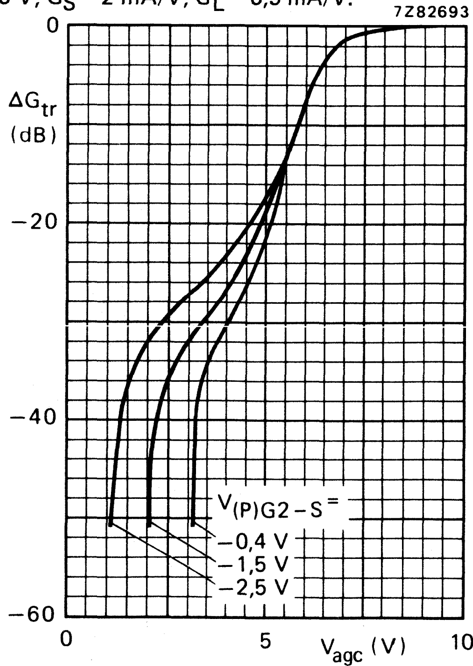


Fig. 16 V_{DD} = 16 V; f = 200 MHz; T_{amb} = 25 °C; typical values; see also Fig. 15.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\|y_{fs}\|$	typ.	25	mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	4.0	pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V: f = 200 MHz	F	typ.	1.2	dB

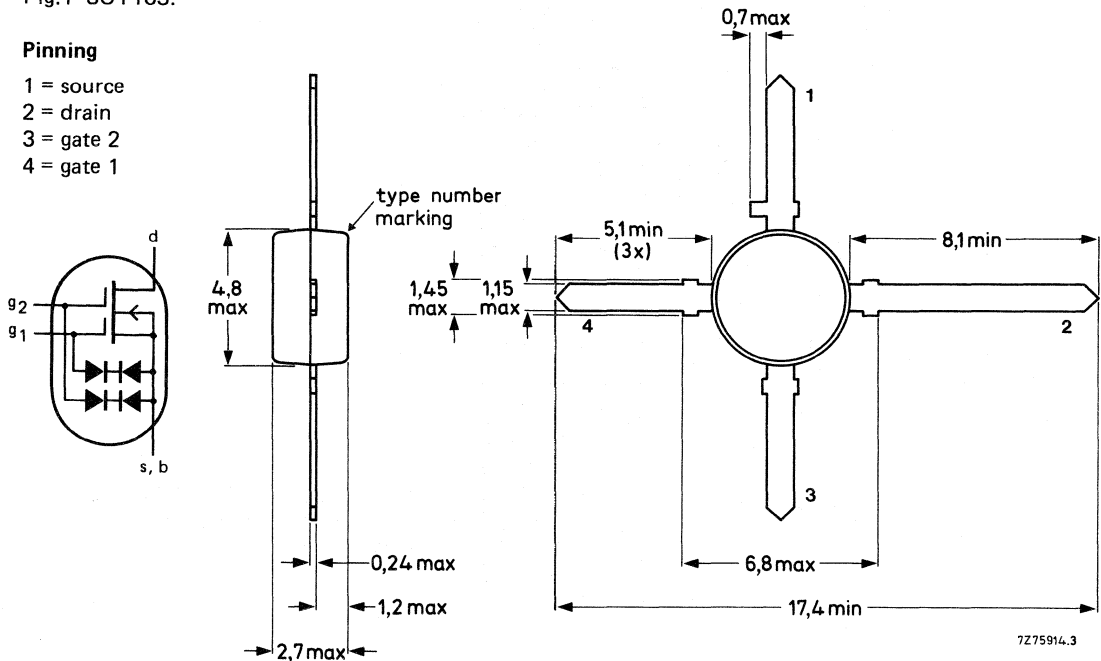
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

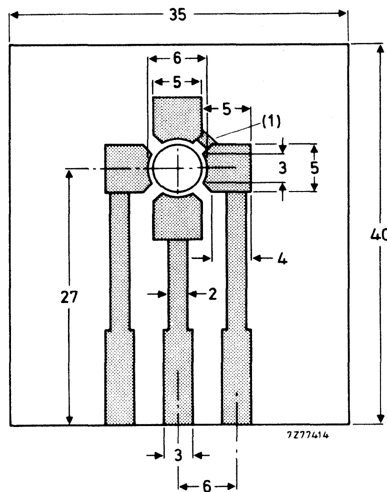
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2) $R_{th\ j\text{-}a}$ = 335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 7$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	<	25 nA
$\pm V_{G2\text{-}S} = 7$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	<	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$	>	8 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$	>	8 to 20 V
Gate-source cut-off voltages			
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	<	1.3 V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	<	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 15$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	> typ.	20 mS 25 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	4.0 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2.0 pF
Noise figure at f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt	F	typ.	1.2 dB

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October 1990

BF988

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	225	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure	1	-	dB

MECHANICAL DATA

Dimensions in mm

type number marking

4.8 max

1.2 max

1.05 max

0.7 max

5.1 min (3x)

8.1 min

1

2

3

4

0.24 max

1.2 max

2.7 max

6.8 max

17.4 min

7Z75914.4

Fig.1 SOT103.

PIN CONFIGURATION

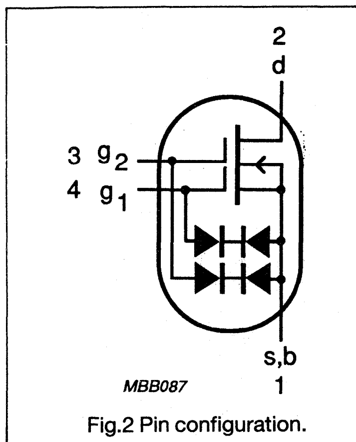


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Silicon n-channel dual gate MOS-FET BF988

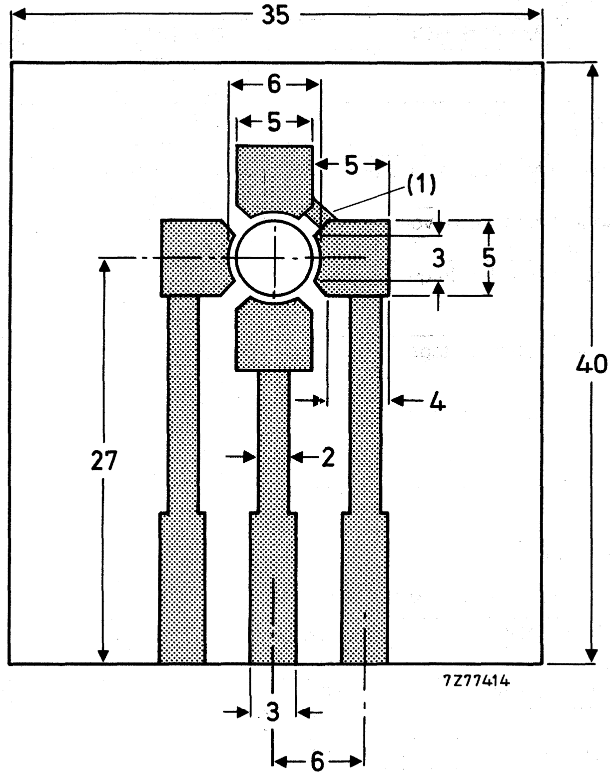
LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1\text{-}S}$	gate 1-source current		-	10	mA
$\pm I_{G2\text{-}S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	-	225	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air mounted on the printed circuit board (see Fig.3)	335	K/W



(1) Connection made by a strip or copper wire.

Tracks are fully tin-lead plated. Board in horizontal position for thermal resistance measurement.

Fig.3 Single-sided 35 μm copper-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm.

Silicon n-channel dual gate MOS-FET BF988

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$\pm V_{G1\text{-}S}$ = 5 V $V_{G2S} = V_{DS}$ = 0	-	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$\pm V_{G2\text{-}S}$ = 5 V $V_{G1S} = V_{DS}$ = 0	-	50	nA
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$\pm I_{G1\text{-}SS}$ = 10 mA $V_{G2\text{-}S} = V_{DS}$ = 0	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$\pm I_{G2\text{-}SS}$ = 10 mA $V_{G1\text{-}S} = V_{DS}$ = 0	6	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	I_D = 20 μA V_{DS} = 8 V $+V_{G2\text{-}S}$ = 4 V	-	2.5	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	I_D = 20 μA V_{DS} = 8 V $V_{G1\text{-}S}$ = 0	-	2.0	V
I_{DSS}	drain current	V_{DS} = 8 V $V_{G1\text{-}S}$ = 0 $+V_{G2\text{-}S}$ = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_s = 2 mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_s = 3.3 mS $B_s = B_{sopt}$	-	1	-	dB

Silicon n-channel dual gate MOS-FET

BF988

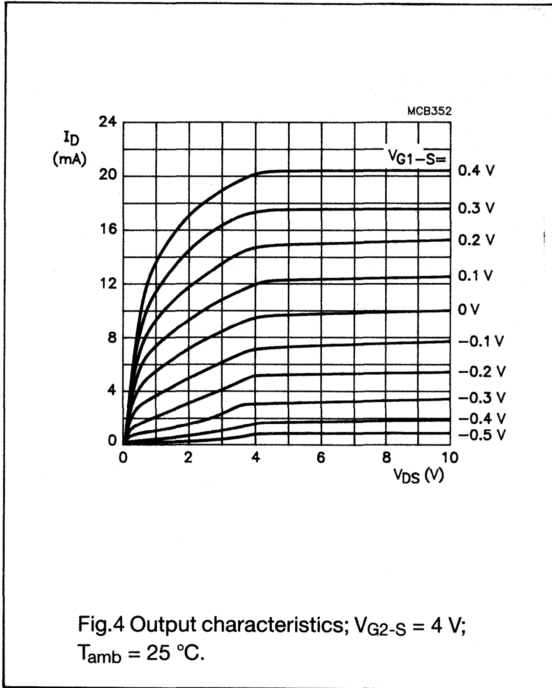


Fig.4 Output characteristics; V_{G2-S} = 4 V; T_{amb} = 25 °C.

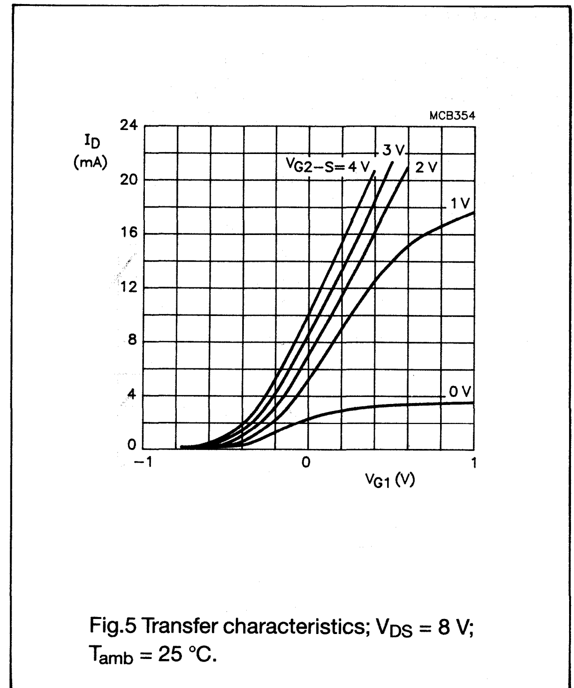


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

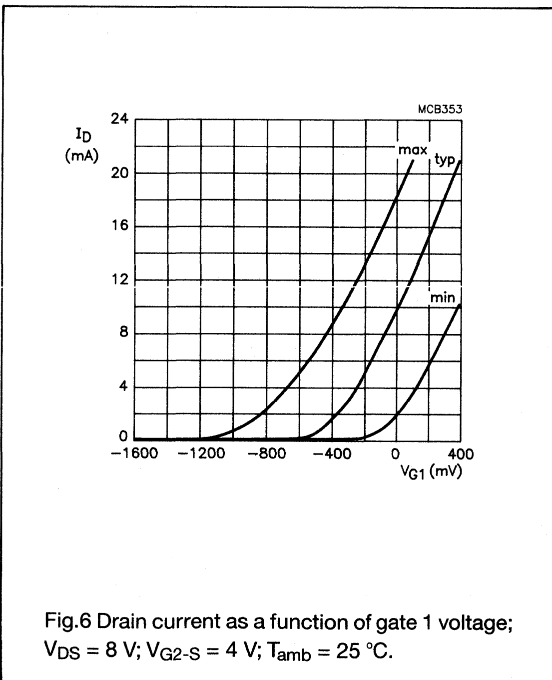


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

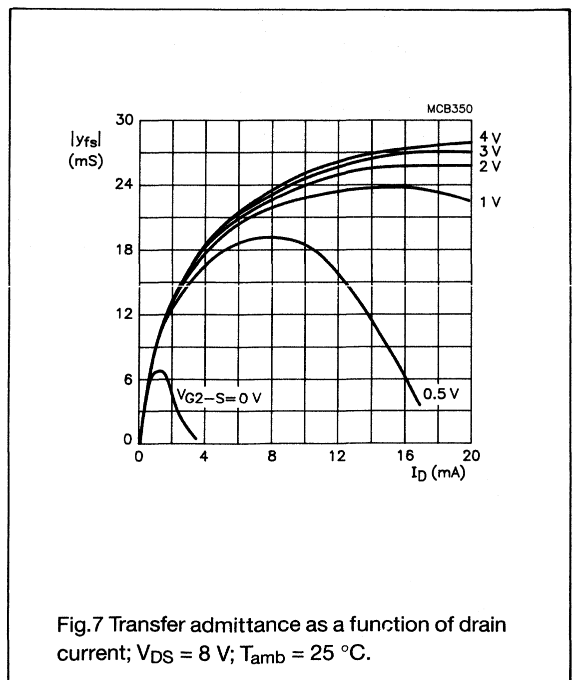


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

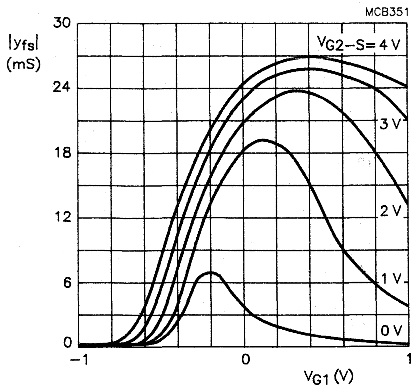


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

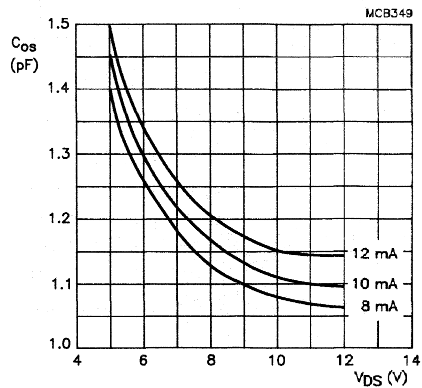


Fig.9 Output capacitance as a function of drain-source voltage; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

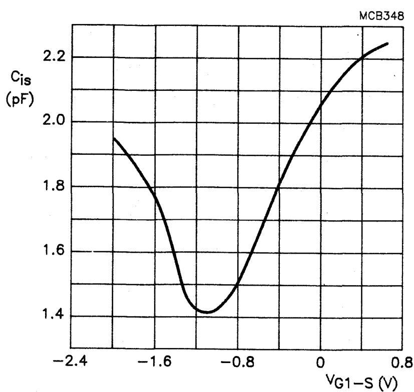


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

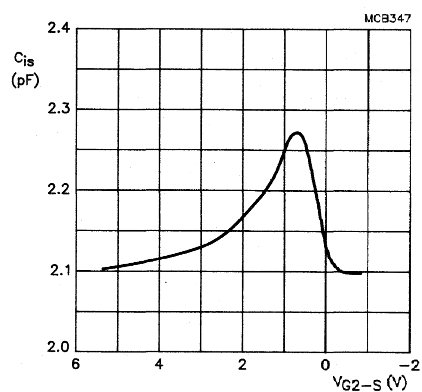


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

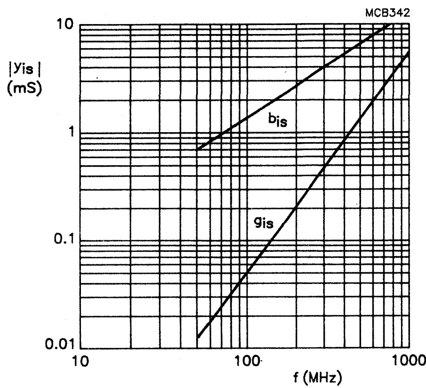


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

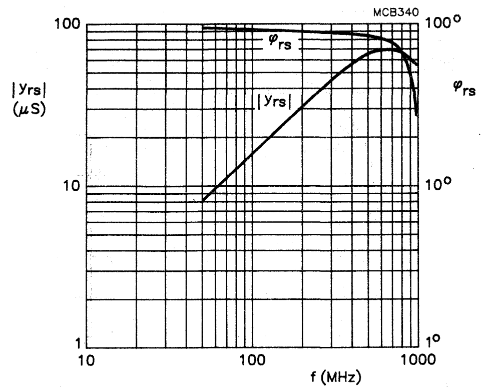


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

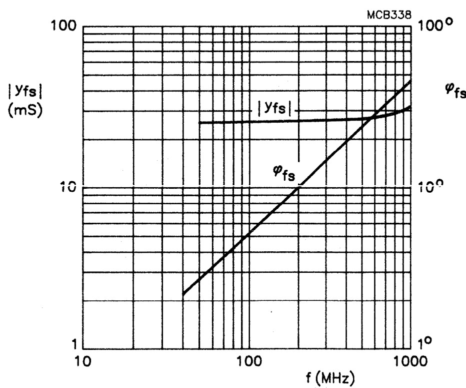


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

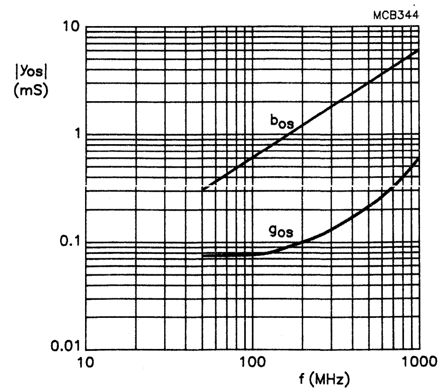


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

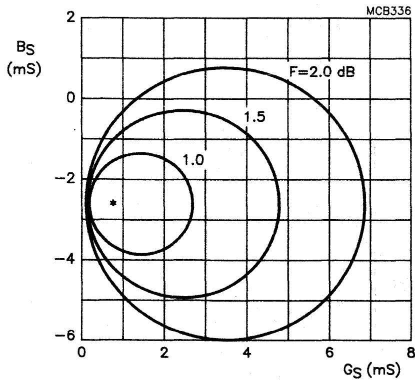


Fig.16 Circles of typical constant noise figures, 200 MHz; F_{opt} = 0.6 dB; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

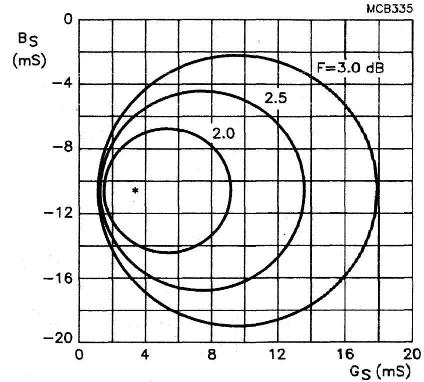
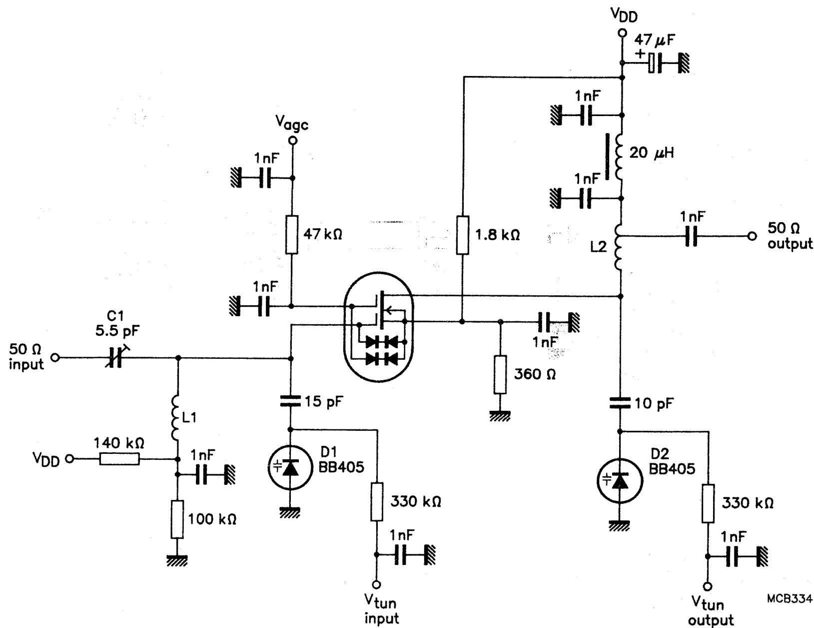


Fig.17 Circles of typical constant noise figures, 800 MHz; F_{opt} = 1.5 dB; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET **BF988**



L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.
L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.18 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.

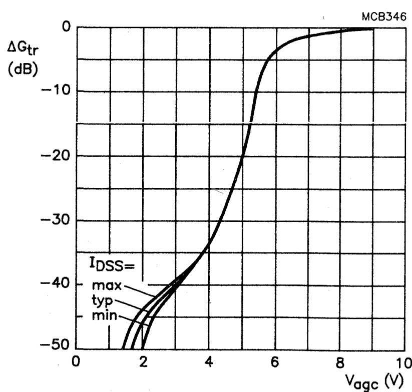
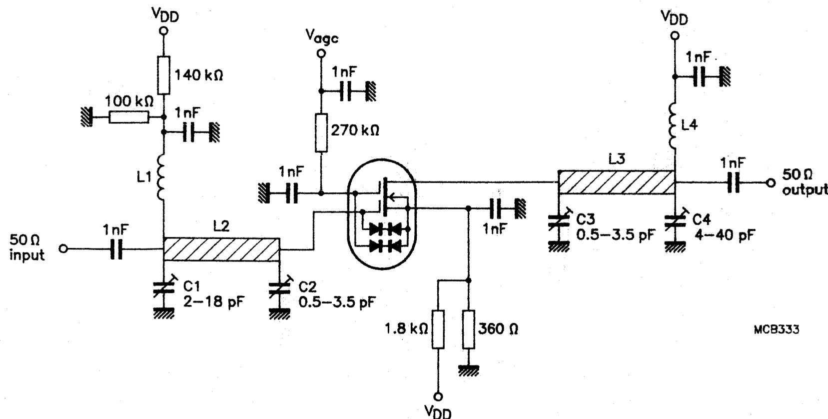


Fig.19 Automatic gain control characteristics measured in circuit of Fig.18; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.20 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

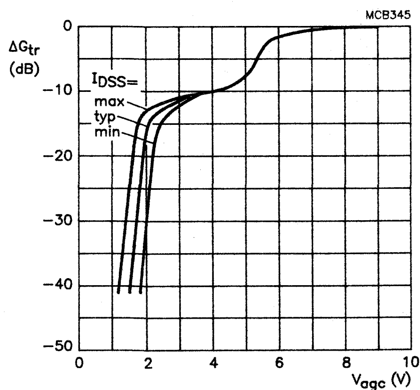


Fig.21 Automatic gain control characteristics measured in circuit of Fig.20; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\|y_{fs}\|$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 800 MHz	F	typ.	2.8 dB

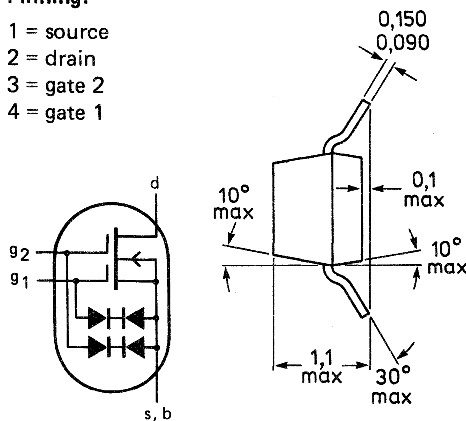
MECHANICAL DATA

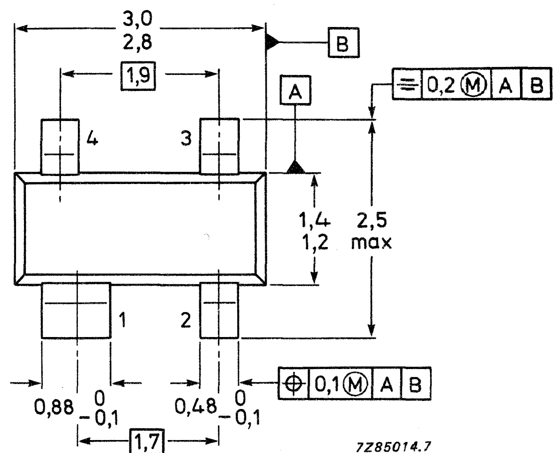
Dimensions in mm

Fig.1 SOT143.

Marking code:
BF989 = MAp

Pinning:
1 = source
2 = drain
3 = gate 2
4 = gate 1





TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460	K/W

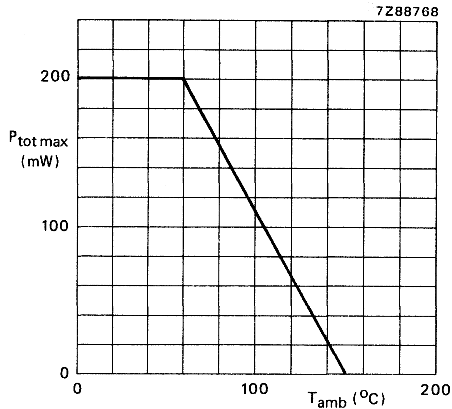


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	max.	50 nA
Drain current			
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+ V_{G2\text{-}S} = 4$ V	I_{DSS}		2 to 20 mA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Gate-source cut-off voltages			
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+ V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	max.	2.7 V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	max.	2.7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 7$ mA; $V_{DS} = 10$ V; $+ V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	9.5 mS
		typ.	12 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1.8 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9 pF
Noise figure at $G_S = 2$ mS; $B_S = B_S$ opt			
f = 200 MHz	F	typ.	1.6 dB
f = 800 MHz	F	typ.	2.8 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners with 12 V supply voltage and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\|y_{fs}\|$	typ.	19 mS
Input capacitance at gate; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ. max.	2.0 dB 3.0 dB

MECHANICAL DATA

Fig.1 SOT143.

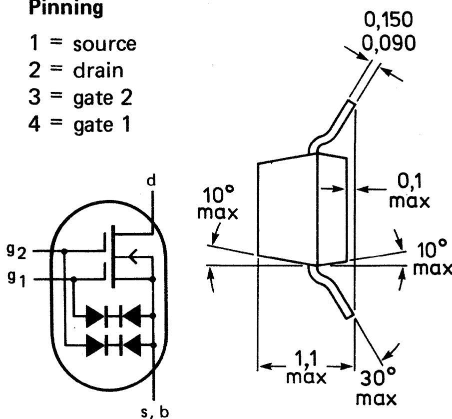
Marking code

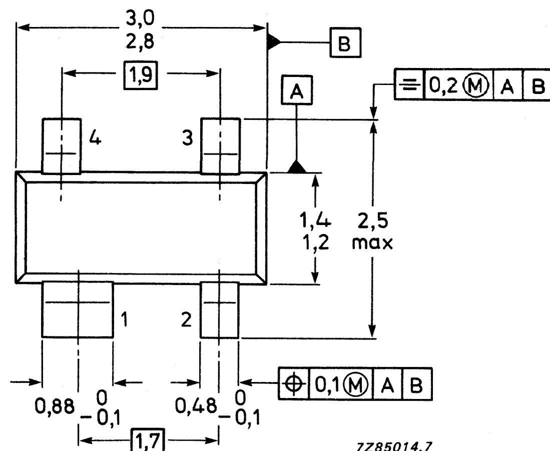
BF990A = M87

Dimensions in mm

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1





See also *Soldering recommendations.*

TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18	V
Drain current	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460	K/W

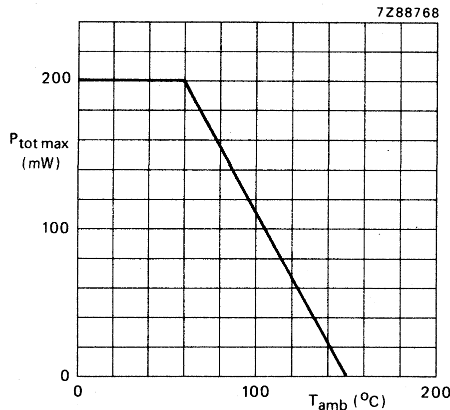


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1;			
$\pm V_{G1\text{-}S}$ = 7 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	25 nA
gate 2;			
$\pm V_{G2\text{-}S}$ = 7 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	25 nA
Gate-source breakdown voltages			
gate 1;			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		8 to 20 V
gate 2;			
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		8 to 20 V
Gate-source cut-off voltages			
gate 1;			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	1.3 V
gate 2;			
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	18 mS 19 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2 pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ. max.	2.0 dB 3.0 dB

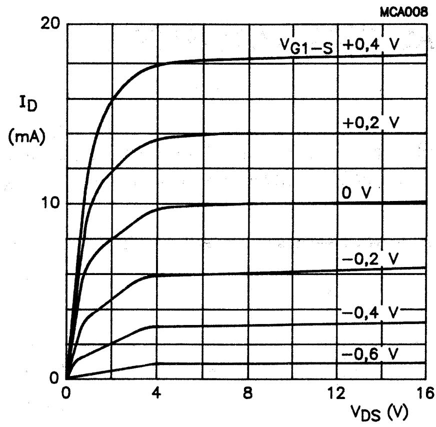


Fig.3 Output characteristics.
$V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

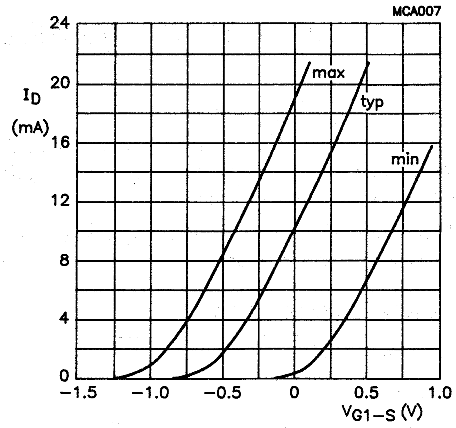


Fig.4 Transfer characteristics.
V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; 3 $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.0 dB

MECHANICAL DATA

Fig.1 SOT143R.

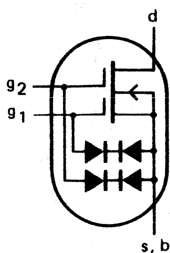
Marking code

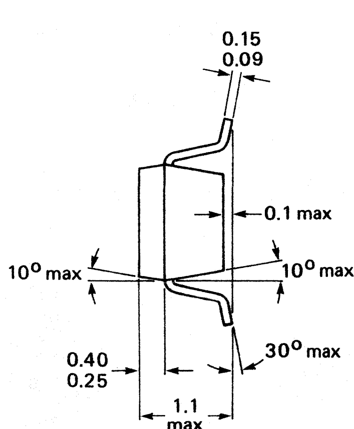
BF990AR = M85

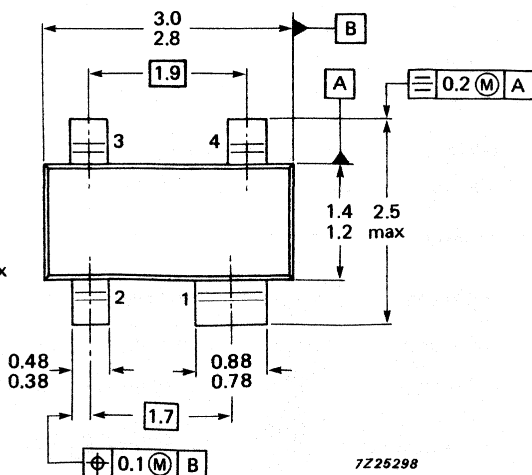
Dimensions in mm

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1







See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1\text{-}S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2\text{-}S}$	max.	10 mA
Total power dissipation up to T_{amb} = 50 °C*	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	500 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1\text{-}S}$ = 7 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	25 nA
gate 2; $\pm V_{G2\text{-}S}$ = 7 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	25 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$	min.	8 to 20 V
gate 2; $\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$	min.	8 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	1.3 V
gate 2; I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	18 mS
		typ.	19 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2.6 pF
		max.	3.0 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2 pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ.	2.0 dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\|y_{fs}\|$	typ.	14	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,1	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0,7	dB

MECHANICAL DATA

Dimensions in mm

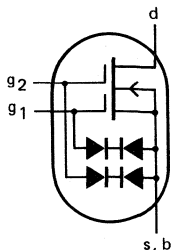
Fig.1 SOT143.

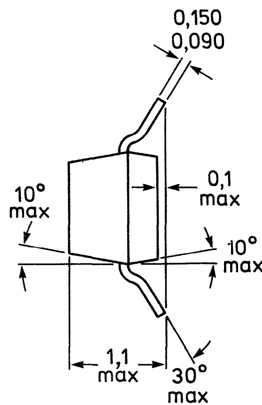
Marking code

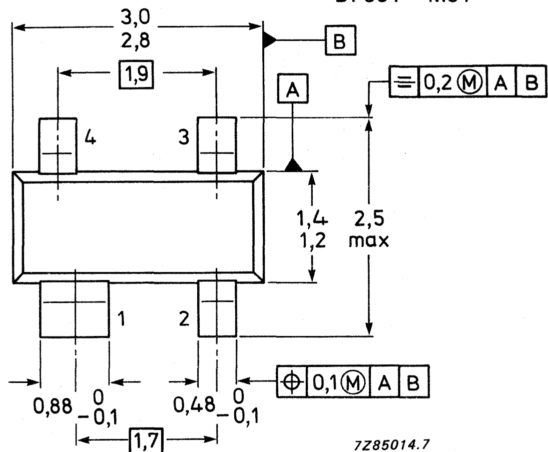
BF991 = M91

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1







See also *Soldering recommendations.*

TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460	K/W

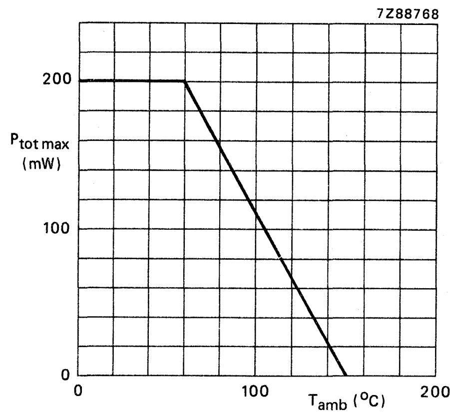


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	<	50 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	<	50 nA
Drain current			
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V	I_{DSS}		4 to 25 mA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Gate-source cut-off voltages			
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	<	2,5 V
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	<	2,5 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	> typ.	10 mS 14 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,1 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1 pF
Noise figure			
f = 100 MHz; $G_S = 1$ mS; $B_S = B_S$ opt	F	typ. <	0,7 dB 1,7 dB
f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt	F	typ. <	1,0 dB 2,0 dB
Transducer gain (note 1)			
f = 100 MHz; $G_S = 1$ mS; $B_S = B_S$ opt; $G_L = 0,5$ mS; $B_L = B_L$ opt	G_{tr}	typ.	29 dB
f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt; $G_L = 0,5$ mS; $B_L = B_L$ opt	G_{tr}	typ.	26 dB

Note

1. Crystal mounted in a SOT103 envelope.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\|y_{fs}\|$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	4 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

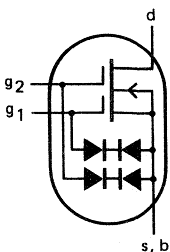
Fig.1 SOT143.

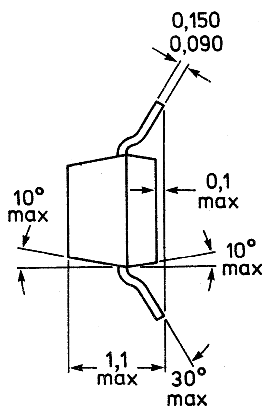
Dimensions in mm

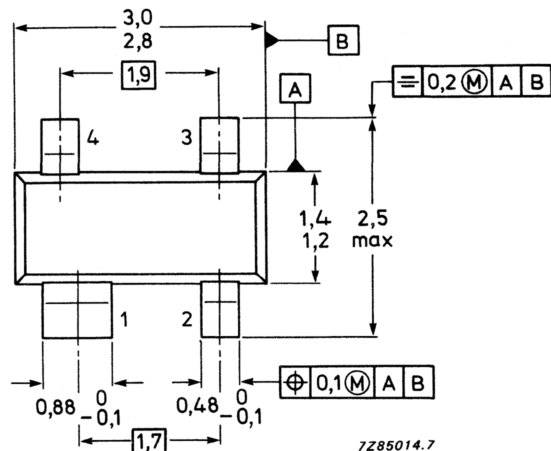
Marking code:
BF992 = M92

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1







See also *Soldering recommendations.*

TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460	K/W

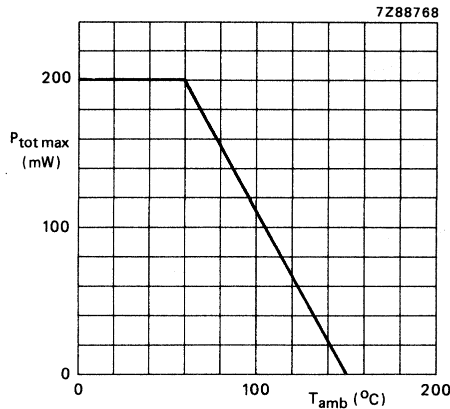


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 7 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	25 nA
$\pm V_{G2\text{-}S}$ = 7 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		8 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$		0.2 to 1.3 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$		0.2 to 1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	20 mS
		typ.	25 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
		max.	40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2 dB

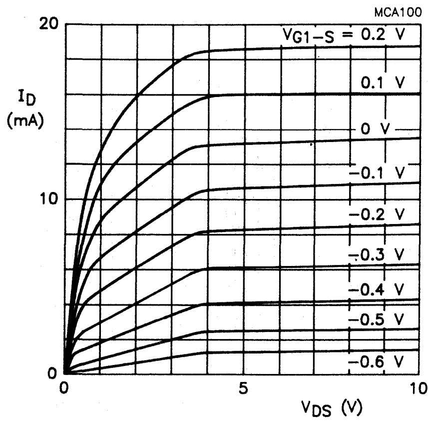


Fig.2 Output characteristics.

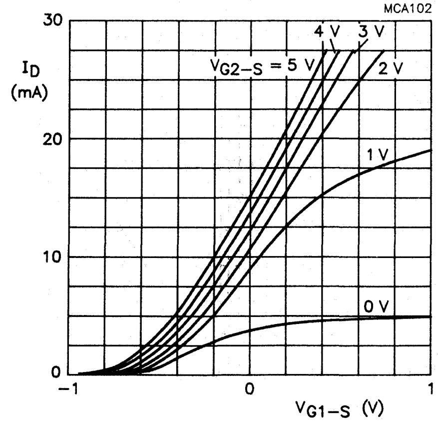


Fig.3 Transfer characteristics.

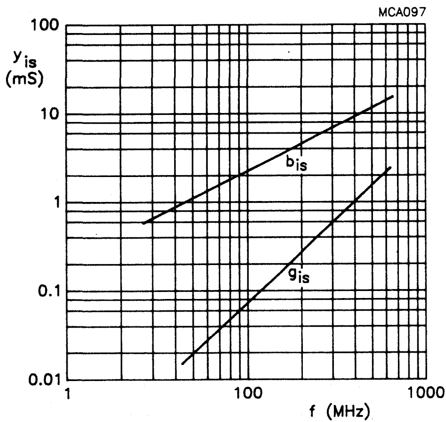


Fig.4 Input admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

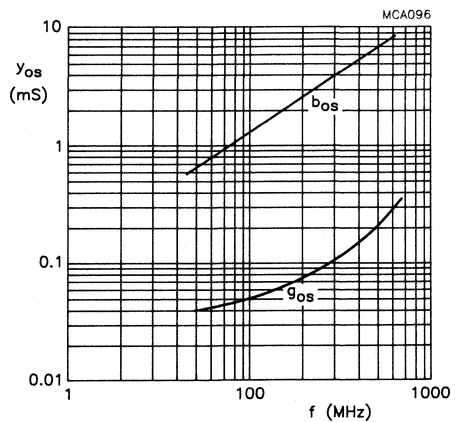


Fig.5 Output admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

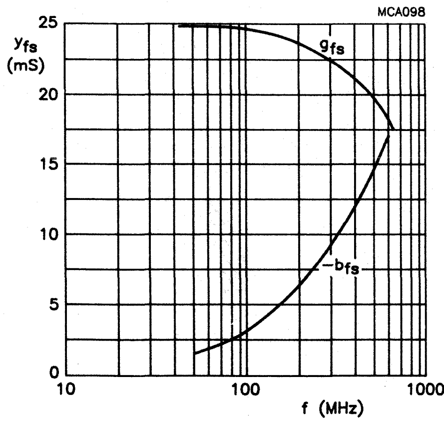


Fig.6 Transfer admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

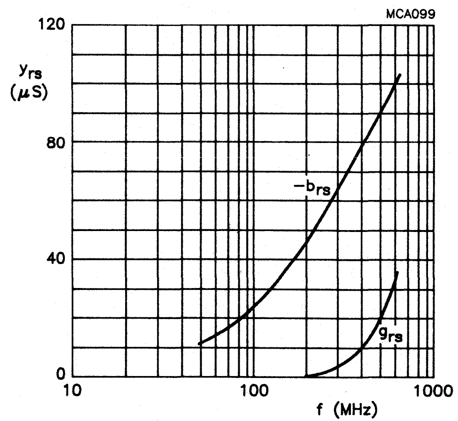


Fig.7 Feedback admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

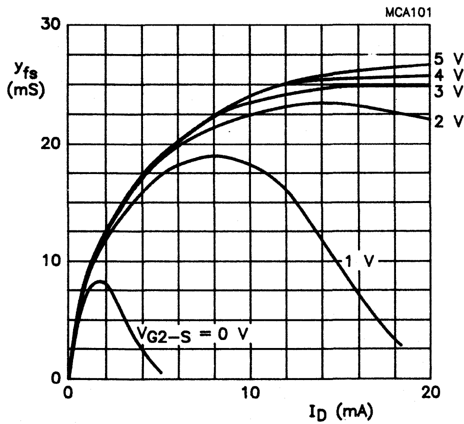


Fig.8 Transfer admittance as a function of drain current.

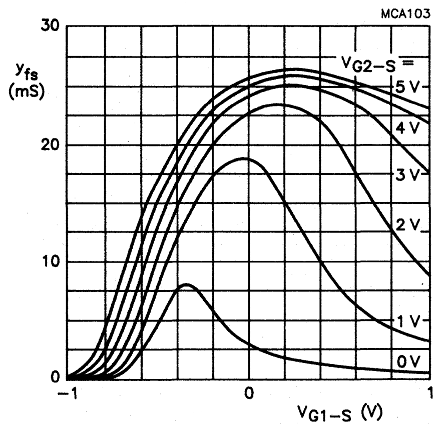


Fig.9 Transfer admittance as a function of gate 2 source voltage.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in VHF applications, such as VHF television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25	mS
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30	fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2	dB

MECHANICAL DATA

Dimensions in mm

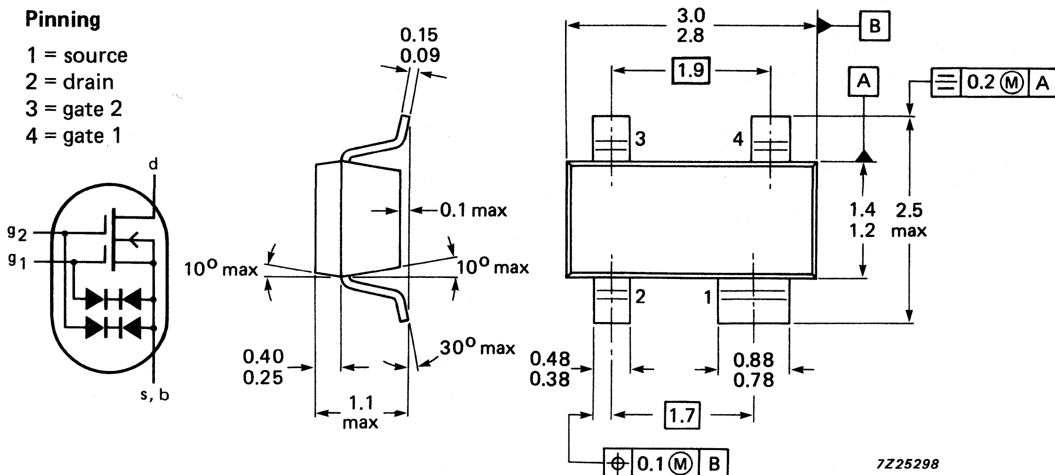
Fig.1 SOT143R.

Marking code

BF992R = M52

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 50 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	500	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1\text{-}S}$ = 7 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	25	nA
$\pm V_{G2\text{-}S}$ = 7 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	25	nA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		8 to 20	V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		8 to 20	V
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$		0.2 to 1.3	V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$		0.2 to 1.1	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	min.	20	mS
		typ.	25	mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	4	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.7	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
		max.	40	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2	pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2	dB

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for VHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\vert y_{fs}\vert$	typ.	18	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 3.0	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0	dB

MECHANICAL DATA

Dimensions in mm

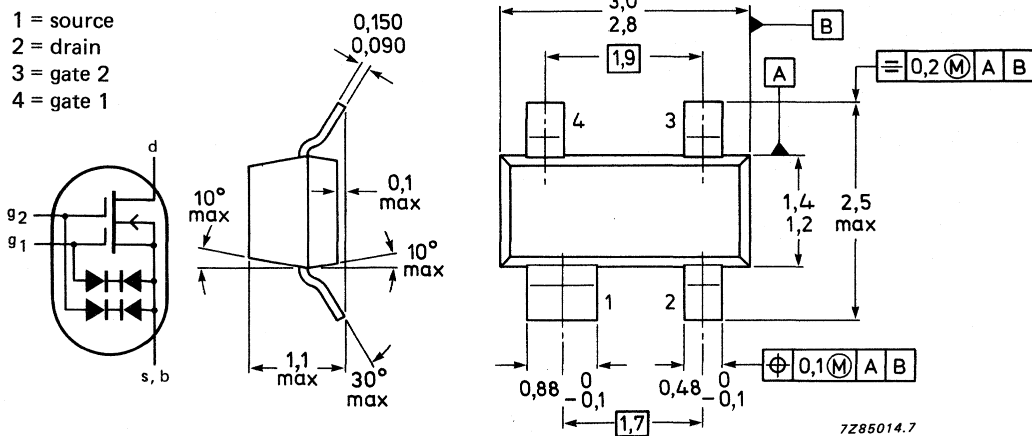
Fig.1 SOT143.

Marking code

BF994S = MGp

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1\text{-}S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2\text{-}S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460 K/W

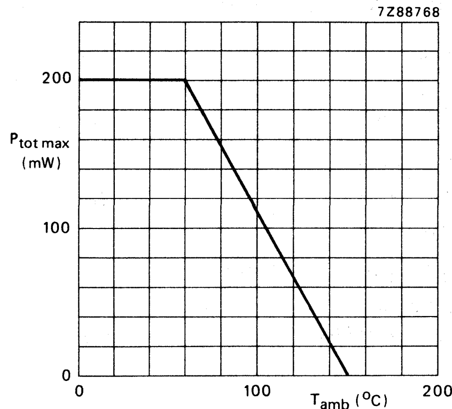


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	50 nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1-S}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-S}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		6 to 20 V
Drain current			
V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ.	2.5 pF
		max.	3.0 pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at G_S = 2 mS; $B_S = B_S$ opt; f = 200 MHz	F	typ.	1.0 dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt			
G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for UHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates ans source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18	mS
Input capacitance at gate 1 : f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 2.6	pF pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.8	dB

MECHANICAL DATA

Dimensions in mm

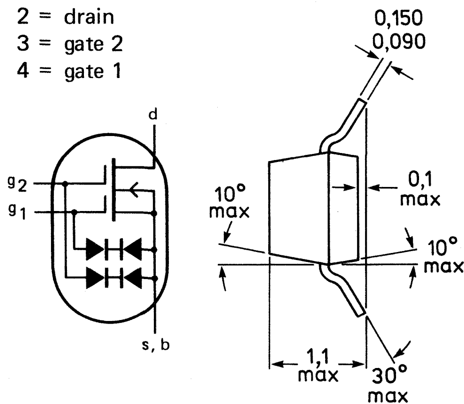
Fig.1 SOT143.

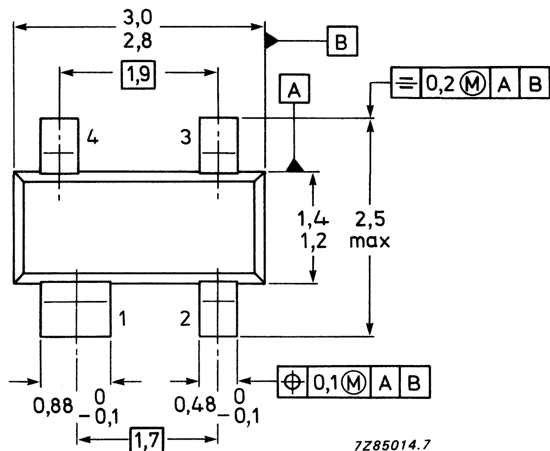
Marking code

BF996S = MHp

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1





TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460	K/W

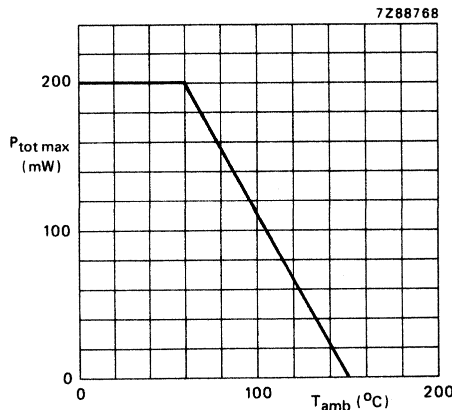


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}S} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}S} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
$V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$; $V_{G2\text{-}S} = 4$ V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	max.	2.5 V
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	15 mS 18 mS
Input capacitance at gate 1: f = 1 MHz	$C_{ig1\text{-}s}$	typ. max.	2.3 pF 2.6 pF
Input capacitance at gate 2: f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8 pF
Noise figure			
f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt f = 800 MHz; $G_S = 3.3$ mS; $B_S = B_S$ opt	F	typ. typ.	1.0 dB 1.8 dB
Power gain			
f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt; $G_L = 0.5$ mS; $B_L = B_L$ opt f = 800 MHz; $G_S = 3.3$ mS; $B_S = B_S$ opt; $G_L = 1.0$ mS; $B_L = B_L$ opt	G_p	typ. typ.	25 dB 18 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with a large tuning range up to 500 MHz.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$\lvert y_{fs}\rvert$	typ.	18	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	2.5	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	1.0	dB

MECHANICAL DATA

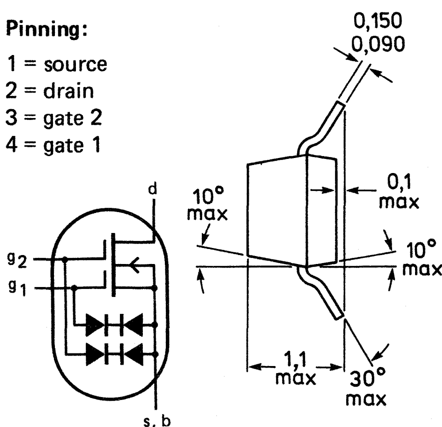
Dimensions in mm

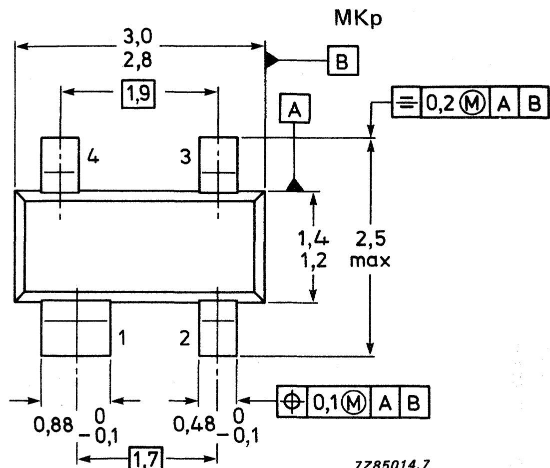
Fig.1 SOT143.

Marking code: MKp

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1





TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j\text{-}a}$	=	460	K/W

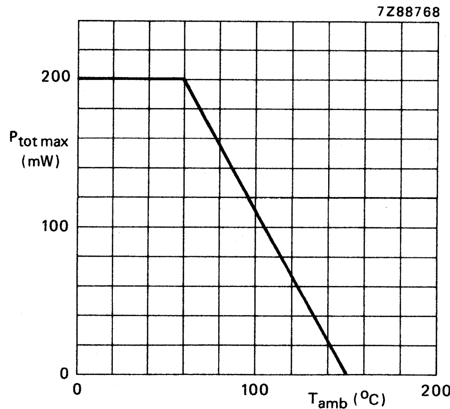


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value
Gate cut-off currents			
gate 1; $\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	50 nA
gate 2; $\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
gate 2; $\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.5 V
gate 2; I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.0 V
Drain-source cut-off voltage V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; $V_{G1\text{-}S}$ = 0	I_{DSS}		2 to 20 mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Parameter	Symbol		Value
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2.5 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0 dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt; G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1991

BF998

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure at 800 MHz	1	-	dB

Silicon n-channel dual gate MOS-FET BF998

MECHANICAL DATA

Dimensions in mm

Marking code

BF998 = MOp

TOP VIEW

See also soldering recommendations.

Fig.1 SOT143.

PIN CONFIGURATION

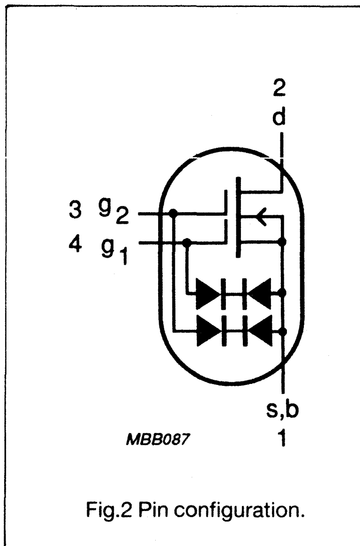


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Silicon n-channel dual gate MOS-FET BF998

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1\text{-}S}$	gate 1-source current		-	10	mA
$\pm I_{G2\text{-}S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C (note 1)	-	200	mW
P_{tot}	total power dissipation	T_{amb} = 50 °C (note 2)	-	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (note 1)	460	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (note 2)	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.
2. Device mounted on printed circuit board.

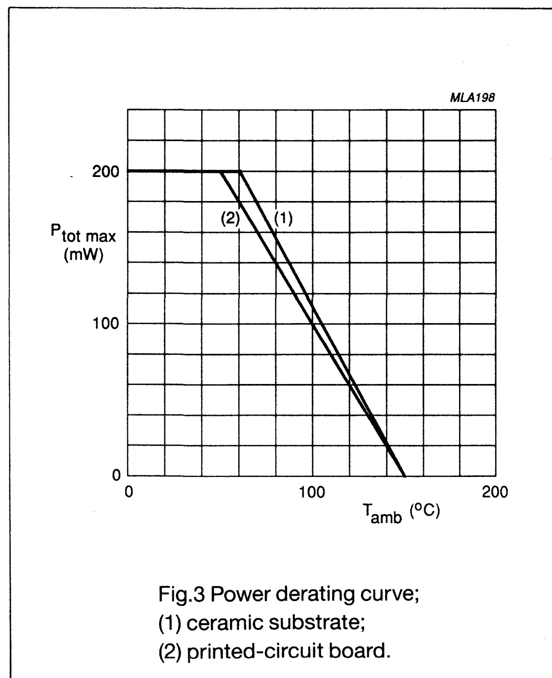


Fig.3 Power derating curve;
(1) ceramic substrate;
(2) printed-circuit board.

Silicon n-channel dual gate MOS-FET BF998

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$\pm V_{G1\text{-}S}$ = 5 V $V_{G2S} = V_{DS}$ = 0	-	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$\pm V_{G2\text{-}S}$ = 5 V $V_{G1S} = V_{DS}$ = 0	-	50	nA
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$\pm I_{G1\text{-}SS}$ = 10 mA $V_{G2\text{-}S} = V_{DS}$ = 0	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$\pm I_{G2\text{-}SS}$ = 10 mA $V_{G1\text{-}S} = V_{DS}$ = 0	6	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $+V_{G2\text{-}S}$ = 4 V	-	2.5	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $V_{G1\text{-}S}$ = 0	-	2.0	V
I_{DSS}	drain current (measured under pulse condition)	V_{DS} = 8 V $V_{G1\text{-}S}$ = 0 $+V_{G2\text{-}S}$ = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_s = 2 mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_s = 3.3 mS $B_s = B_{sopt}$	-	1	-	dB

Silicon n-channel dual gate MOS-FET BF998

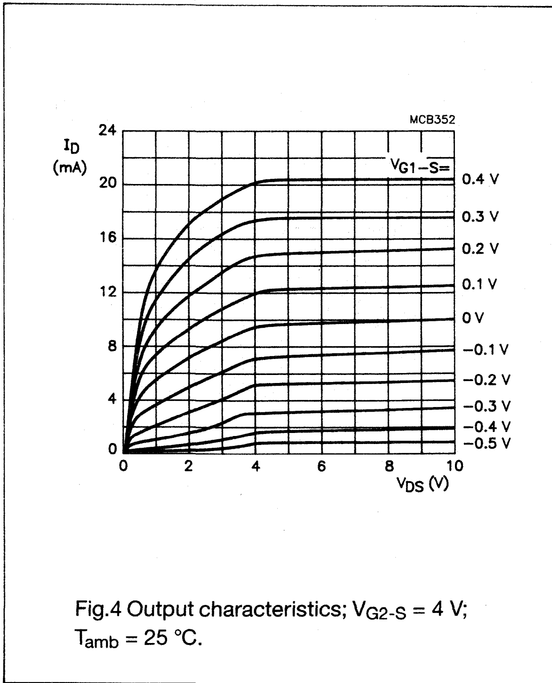


Fig.4 Output characteristics; V_{G2-S} = 4 V; T_{amb} = 25 °C.

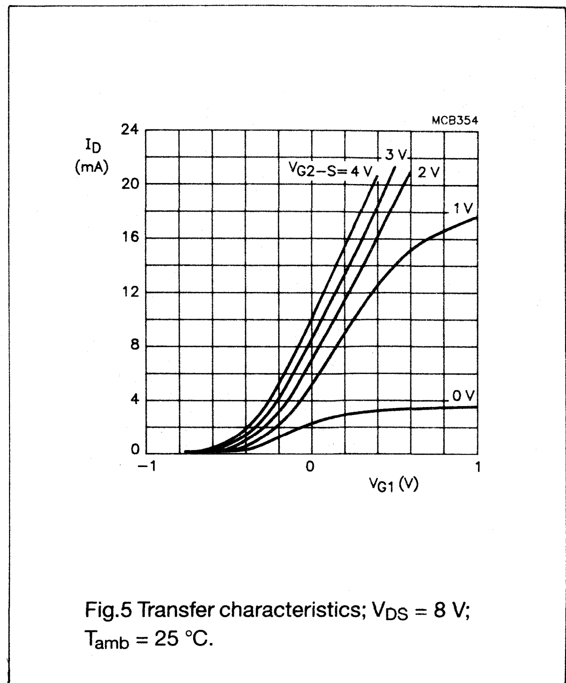


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

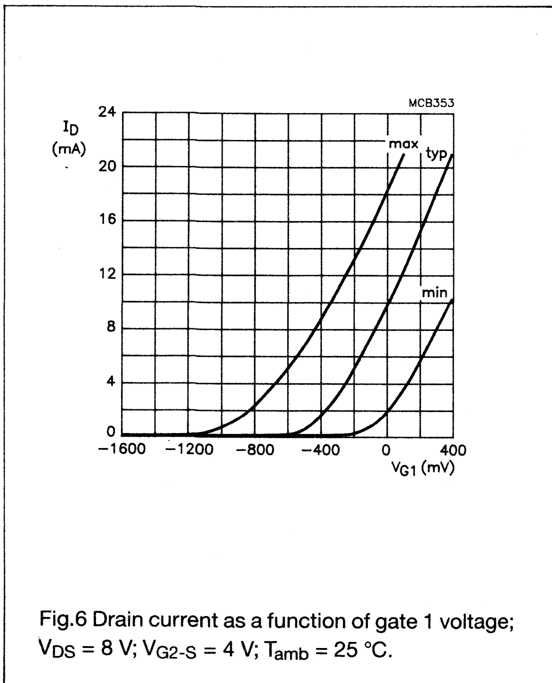


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

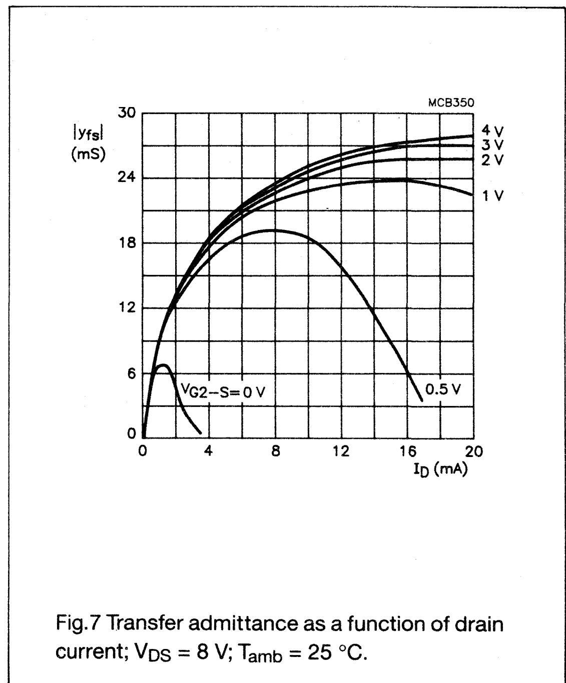


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

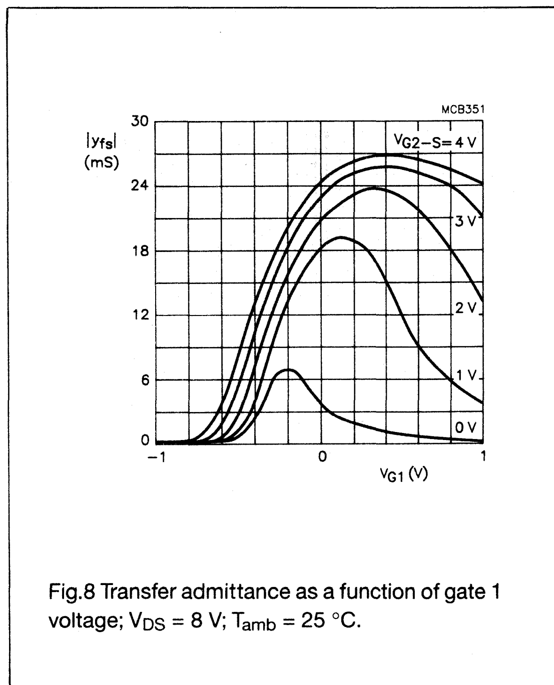


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

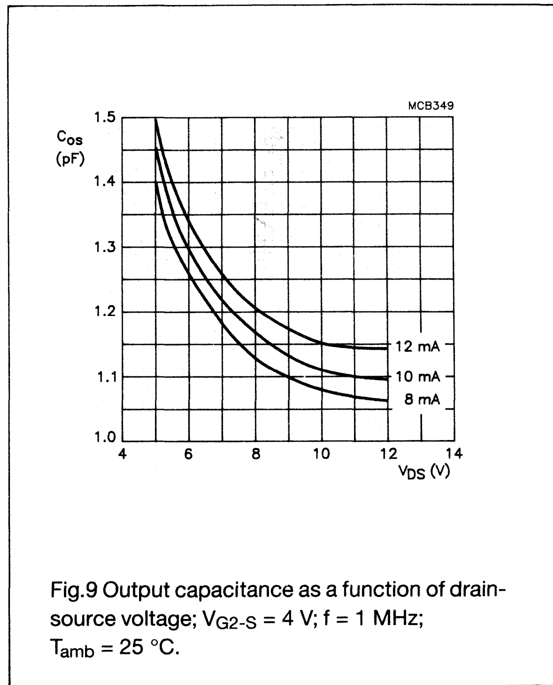


Fig.9 Output capacitance as a function of drain-source voltage; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

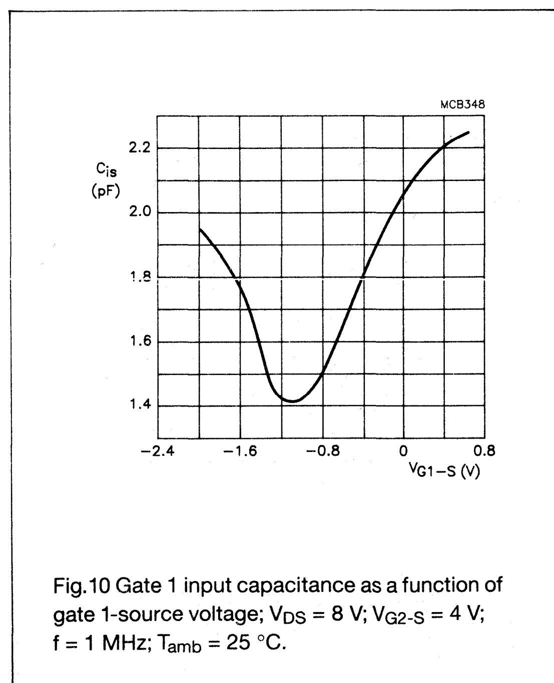


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

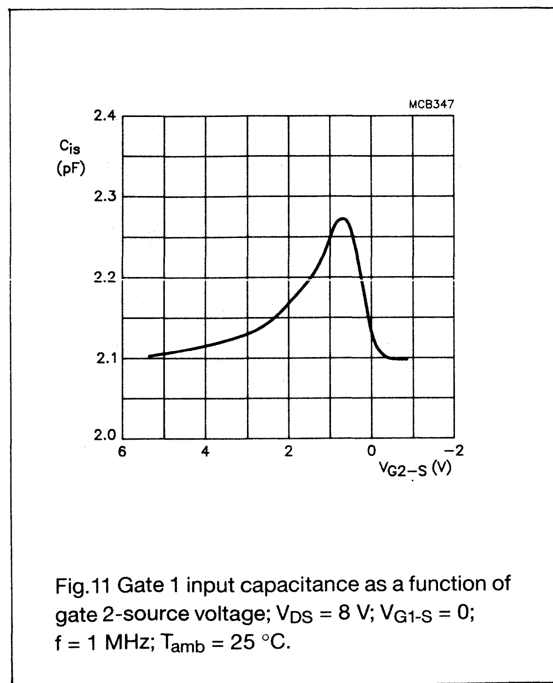


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

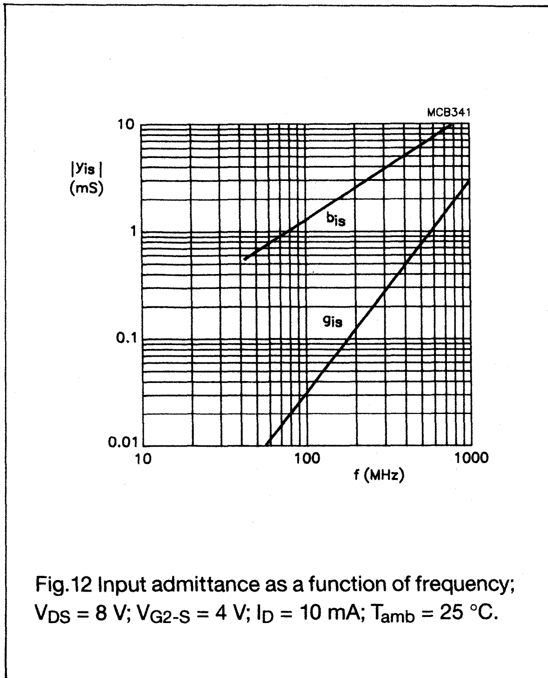


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

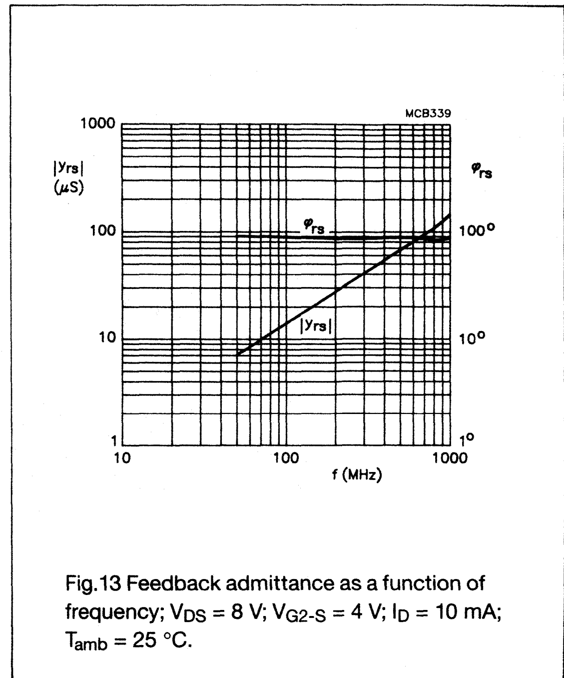


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

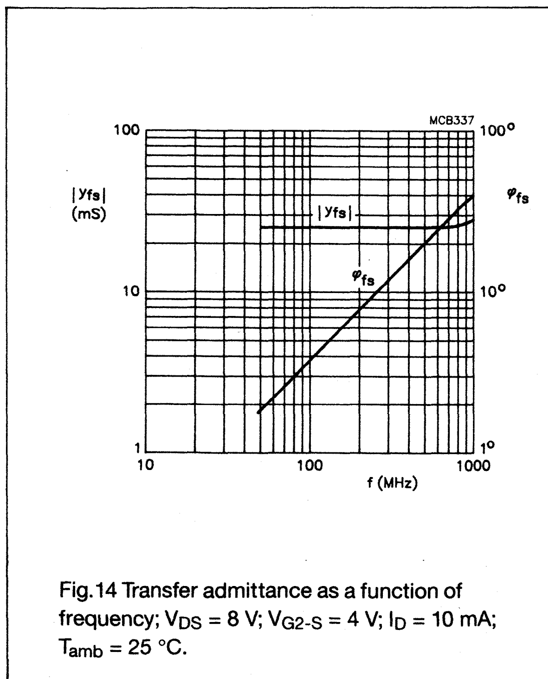


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

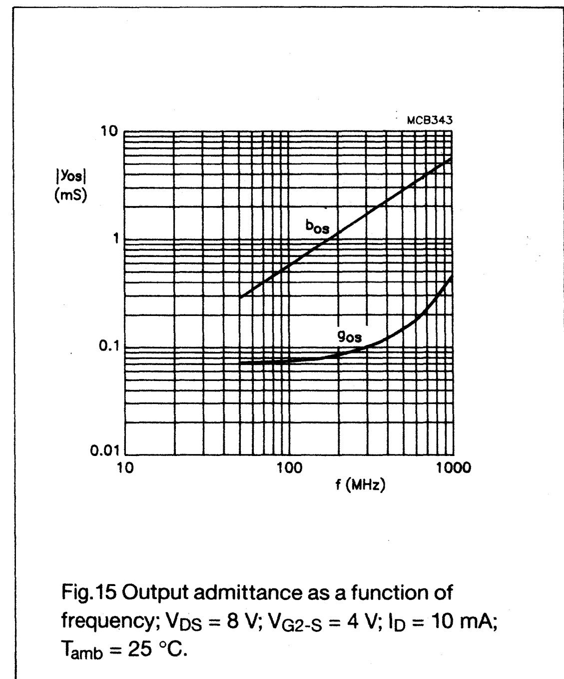
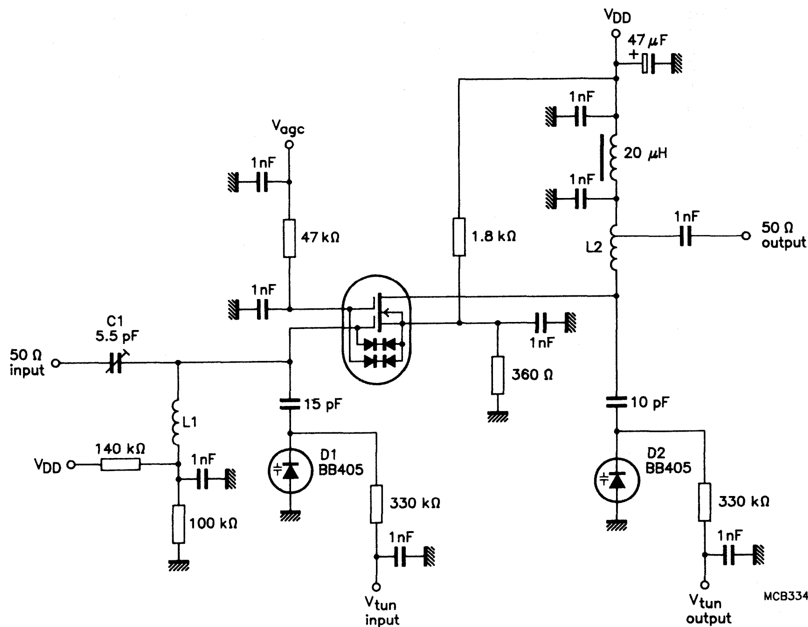
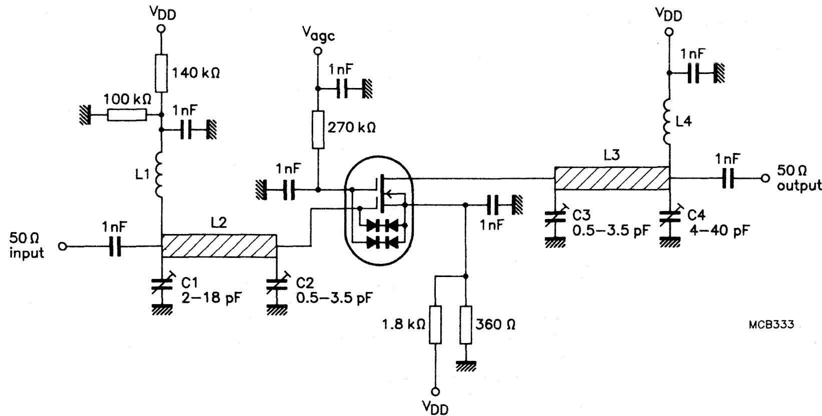


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.



L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.
L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.16 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.17 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

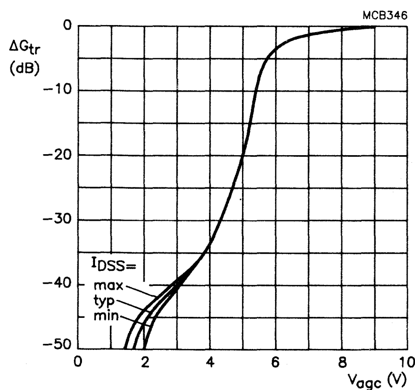


Fig.18 Automatic gain control characteristics measured in circuit of Fig.16; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

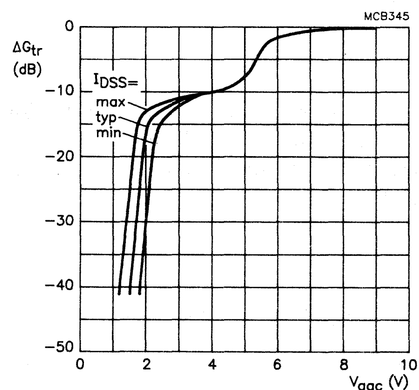


Fig.19 Automatic gain control characteristics measured in circuit of Fig.17; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October 1990

BF998R

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as UHF television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	pF
F	noise figure at 800 MHz	1	-	dB

Silicon n-channel dual gate MOS-FET BF998R

MECHANICAL DATA

Dimensions in mm

Marking code

BF998R = MO$\overline{p}$

See also soldering recommendations.

Fig.1 SOT143R.

PIN CONFIGURATION

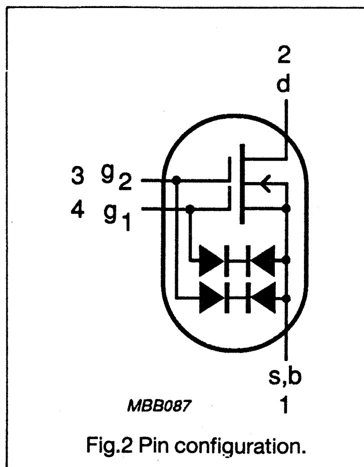


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1-S}$	gate 1-source current		-	10	mA
$\pm I_{G2-S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 50 °C (note 1)	-	200	mW
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient in free air (note 1)	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.

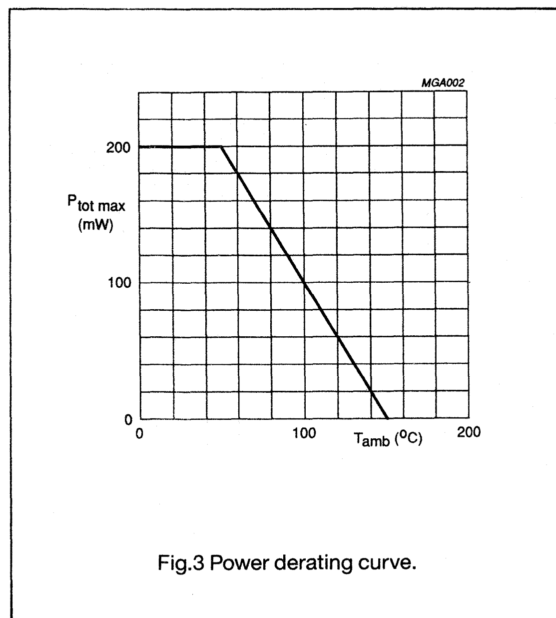


Fig.3 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$\pm V_{G1\text{-}S} = 5$ V $V_{G2S} = V_{DS} = 0$	-	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$\pm V_{G2\text{-}S} = 5$ V $V_{G1S} = V_{DS} = 0$	-	50	nA
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$\pm I_{G1\text{-}SS} = 10$ mA $V_{G2\text{-}S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$\pm I_{G2\text{-}SS} = 10$ mA $V_{G1\text{-}S} = V_{DS} = 0$	6	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$I_D = 20$ μA $V_{DS} = 8$ V $+V_{G2\text{-}S} = 4$ V	-	2.5	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$I_D = 20$ μA $V_{DS} = 8$ V $V_{G1\text{-}S} = 0$	-	2.0	V
I_{DSS}	drain current	$V_{DS} = 8$ V $V_{G1\text{-}S} = 0$ $+V_{G2\text{-}S} = 4$ V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) $I_D = 10$ mA; $V_{DS} = 8$ V; $V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz $G_s = 2$ mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz $G_s = 3.3$ mS $B_s = B_{sopt}$	-	1	-	dB

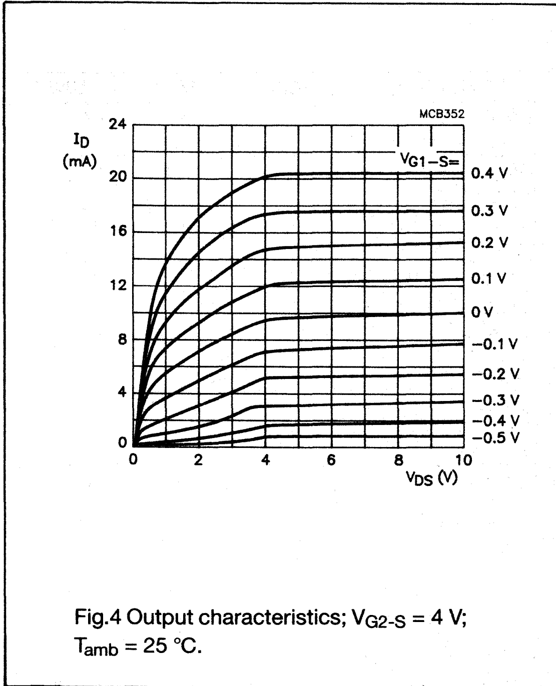


Fig.4 Output characteristics; V_{G2-S} = 4 V; T_{amb} = 25 °C.

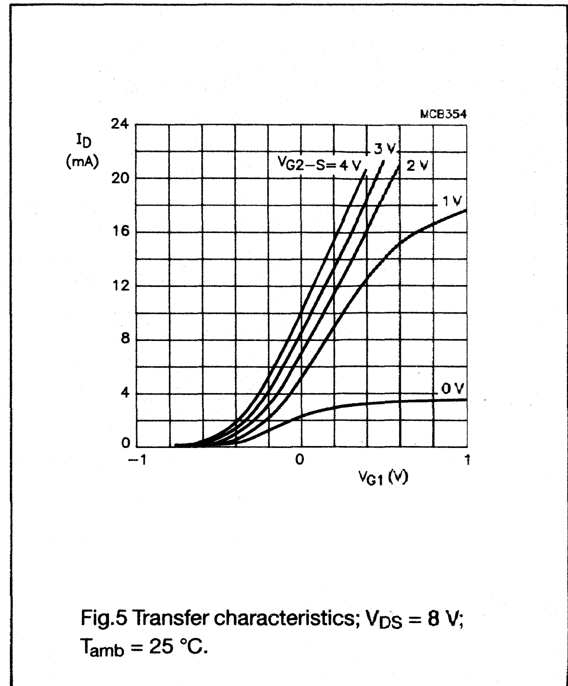


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

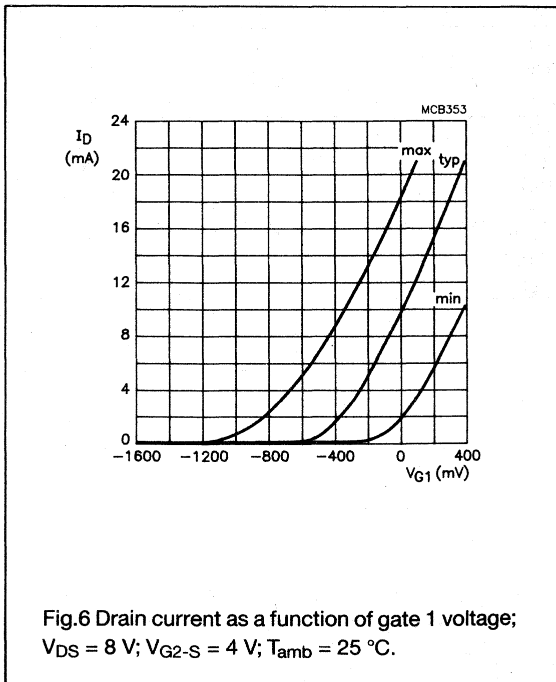


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

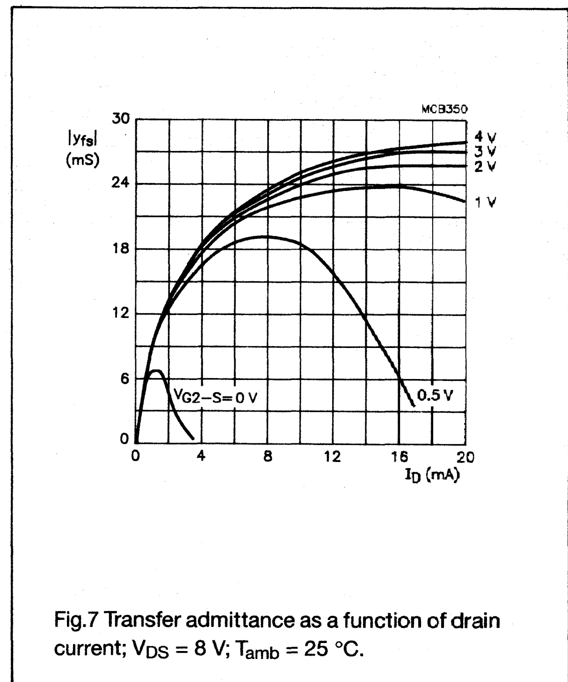


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

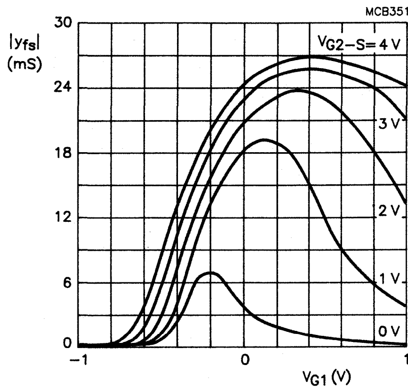


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

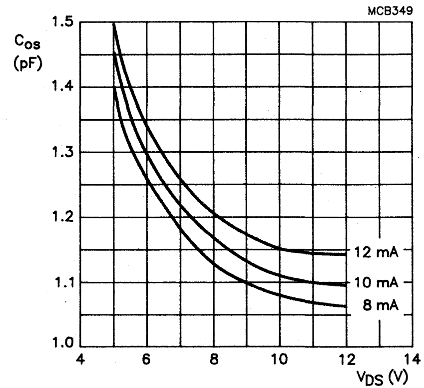


Fig.9 Output capacitance as a function of drain-source voltage; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

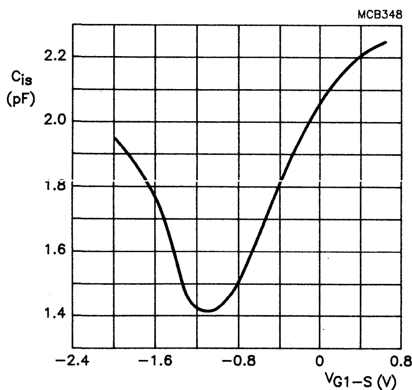


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

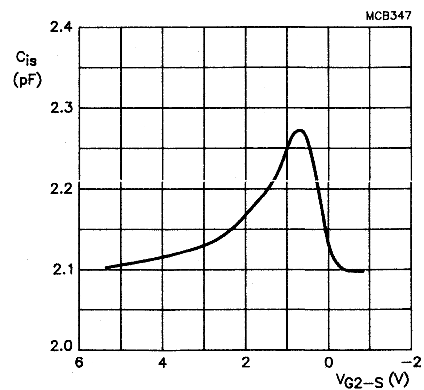


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; V_{G1-S} = 0; f = 1 MHz; T_{amb} = 25 °C.

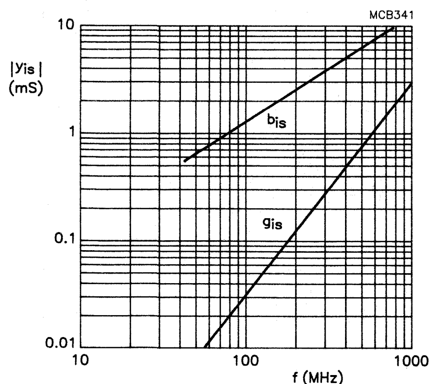


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

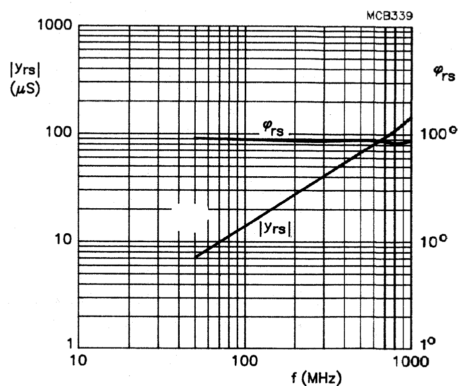


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

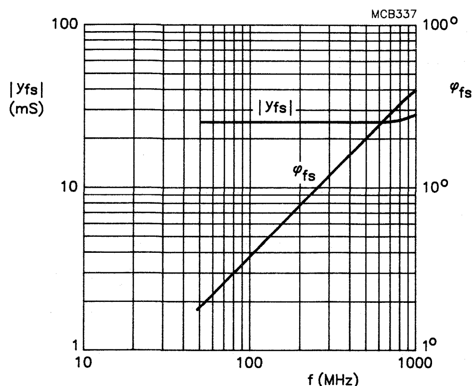


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

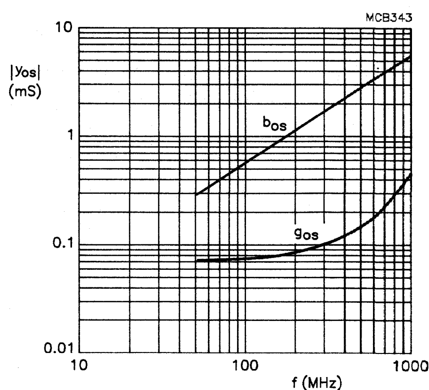
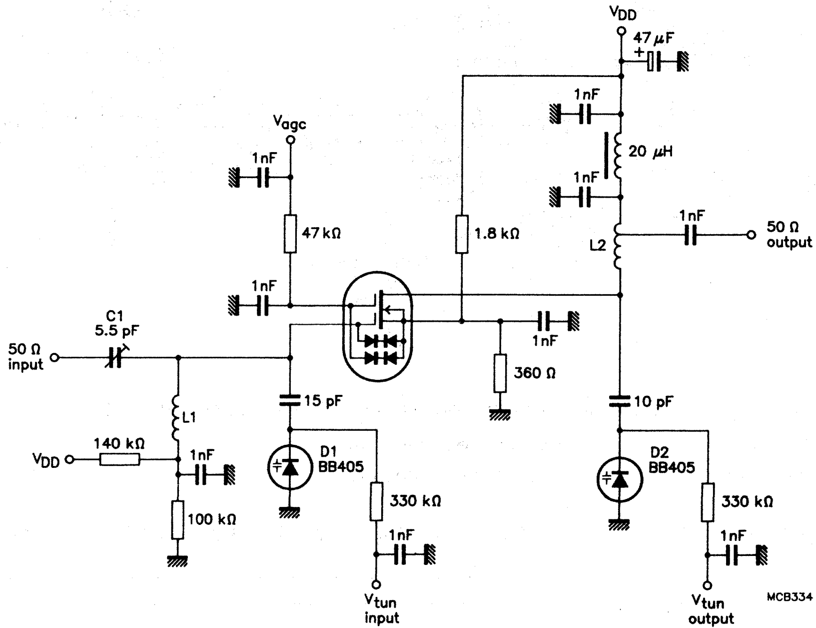


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.



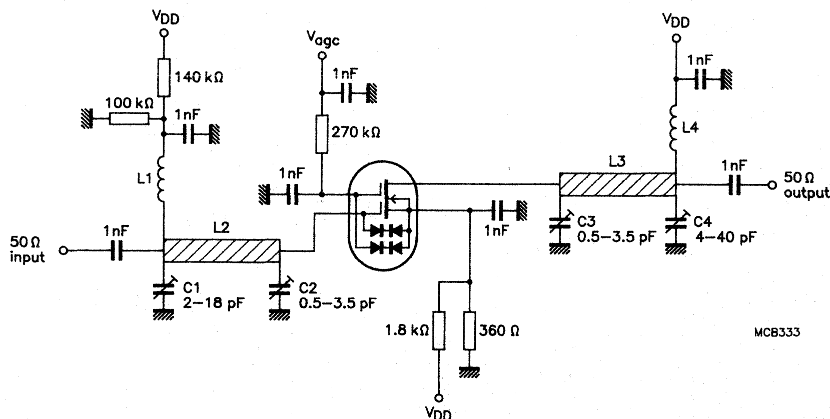
L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.

L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.

Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.

C1 adjusted for G_S = 2 mS.

Fig.16 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.17 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

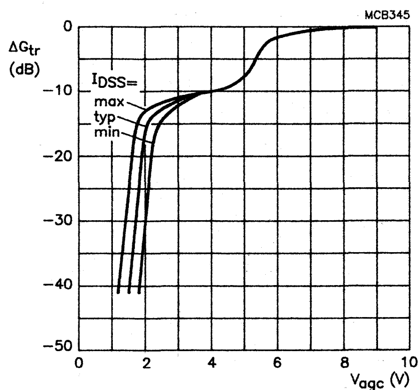


Fig.18 Automatic gain control characteristics measured in circuit of Fig.16; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

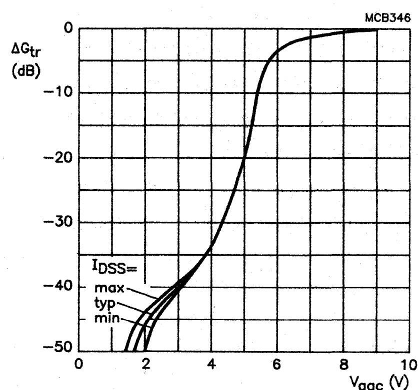


Fig.19 Automatic gain control characteristics measured in circuit of Fig.17; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

QUICK REFERENCE DATA

Drain-substrate voltage	V_{DB}	max.	30	V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10	V
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		10 to 40	mA
Transfer admittance $I_D = 5$ mA; $V_{DS} = 15$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	6	mS
Feedback capacitance $I_D = 5$ mA; $V_{DS} = 15$ V; f = 1 MHz	C_{rs}	<	0,7	pF
Noise figure at f = 200 MHz $I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25$ °C $G_S = 1$ mS; $B_S = B_{Sopt}$	F	<	5	dB
Equivalent noise voltage at f = 1 kHz $I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25$ °C	$V_n/\sqrt{B}$	typ.	100	$nV/\sqrt{Hz}$

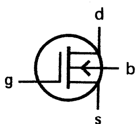
MECHANICAL DATA

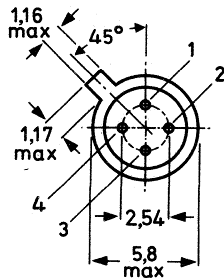
Dimensions in mm

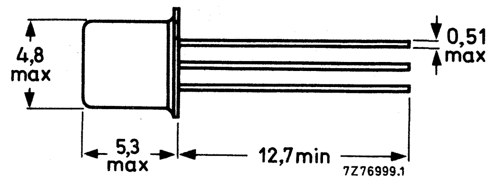
Fig. 1 TO-72.

Pinning

1 = drain
2 = source
3 = gate
4 = substrate (b) connected to case







Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10	V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max.	15	V
		min.	−15	V
Drain current (d.c.)	I_D	max.	20	mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0,1$	I_{DM}	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to + 125		^oC
Junction temperature	T_j	max.	125	^oC

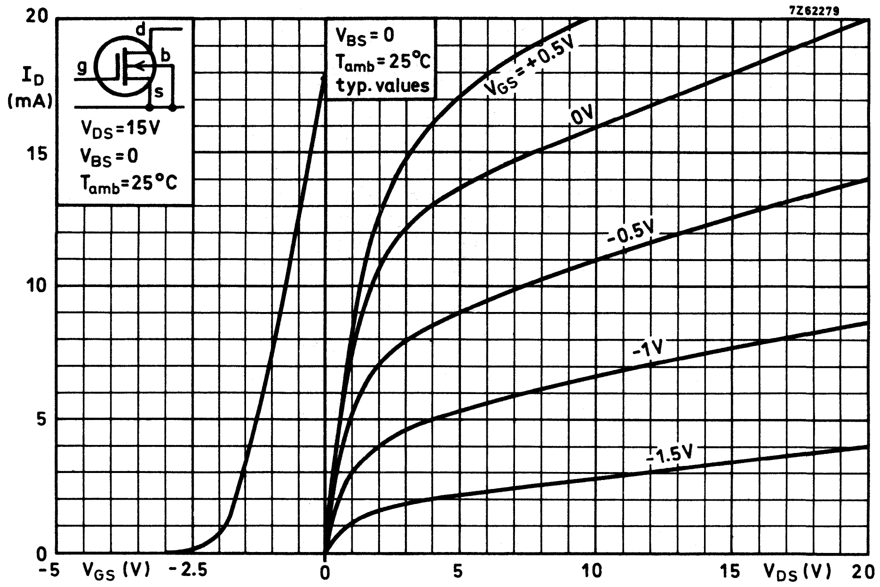
THERMAL RESISTANCE

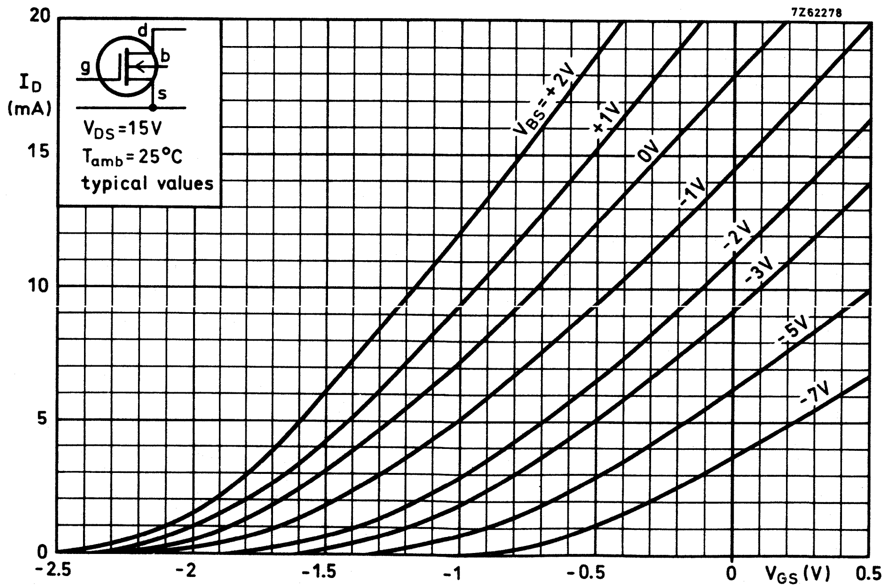
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500	K/W

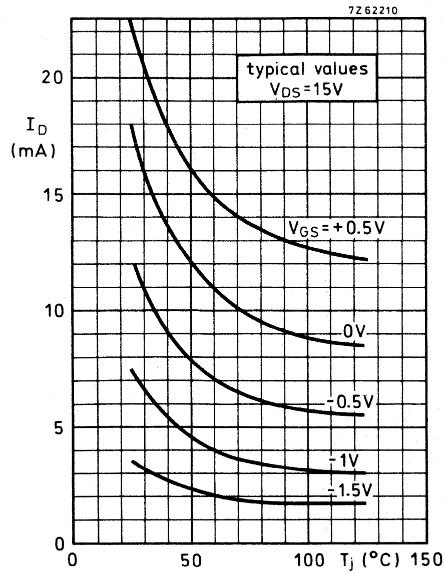
CHARACTERISTICS

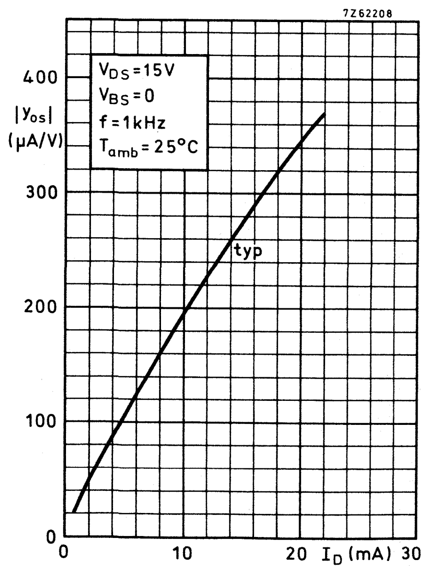
$T_j = 25\,^{o}C$ unless otherwise specified

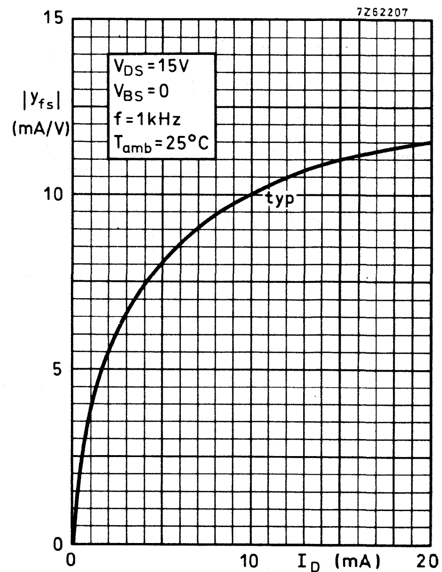
Gate currents; $V_{BS} = 0$				
$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10$ V; $V_{DS} = 0$	I_{GSS}	<	10	pA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\,^{o}C$	$-I_{GSS}$	<	200	pA
$V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\,^{o}C$	I_{GSS}	<	200	pA
Bulk currents; $V_{GB} = 0$				
$-V_{BD} = 30$ V; $I_S = 0$	$-I_{BDO}$	<	10	μA
$-V_{BS} = 30$ V; $I_D = 0$	$-I_{BSO}$	<	10	μA
Drain current				
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		10 to 40	mA
Gate-source voltage				
$I_D = 100$ nA; $V_{DS} = 15$ V	$-V_{GS}$		0.5 to 3.5	V
Gate-source cut-off voltage				
$I_D = 100$ nA ; $V_{DS} = 15$ V	$-V_{(P)GS}$	<	4	V
y parameters				
$I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25\,^{o}C$				
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	6	mS
Output admittance at f = 1 kHz	$\lvert y_{os} \rvert$	<	0.4	mS
Input capacitance at f = 1 MHz	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	0.7	pF
Output capacitance at f = 1 MHz	C_{os}	<	3	pF
Noise figure at f = 200 MHz				
$I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25\,^{o}C$				
$G_S = 1$ mS; $B_S = B_{Sopt}$	F	<	5	dB
Equivalent noise voltage $T_{amb} = 25\,^{o}C$				
$I_D = 5$ mA; $V_{DS} = 15$ V; f = 120 Hz	$V_n/\sqrt{B}$	typ.	300	$nV/\sqrt{Hz}$
$T_{amb} = 25\,^{o}C$ f = 1 kHz	$V_n/\sqrt{B}$	typ.	100	$nV/\sqrt{Hz}$
f = 10 kHz	$V_n/\sqrt{B}$	typ.	35	$nV/\sqrt{Hz}$

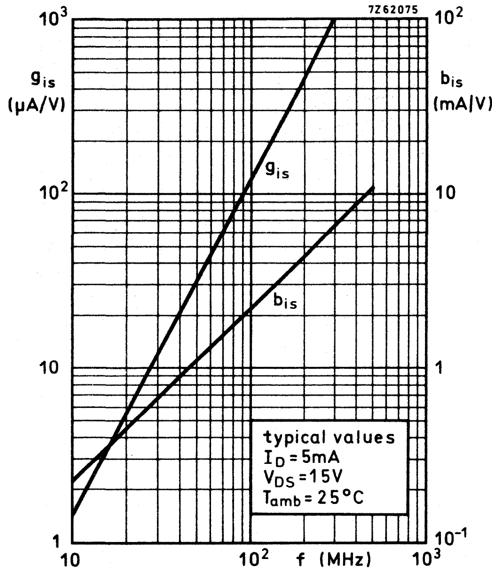

7Z62279
$V_{BS} = 0$
$T_{amb} = 25°C$
typ. values
I_D (mA)
$V_{DS} = 15V$
$V_{BS} = 0$
$T_{amb} = 25°C$
$V_{GS} = +0.5V$
0V
-0.5V
-1V
-1.5V
d
g
b
s
20
15
10
5
0
-5
V_{GS} (V)
-2.5
0
5
10
15
V_{DS} (V)
20

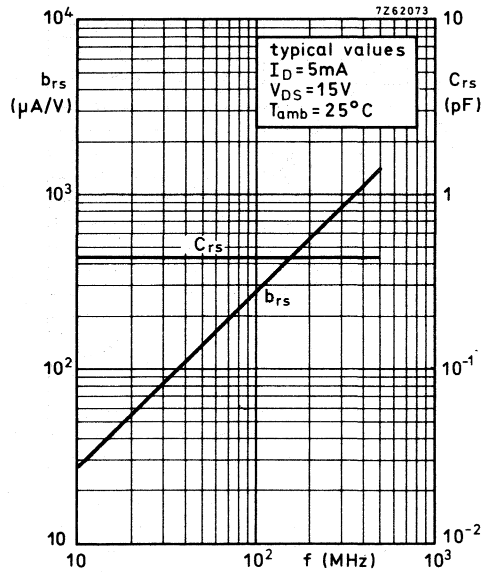

7Z62278
I_D (mA)
$V_{DS} = 15V$
$T_{amb} = 25°C$
typical values
$V_{BS} = +2V$
+1V
0V
-1V
-2V
-3V
-5V
-7V
d
g
b
s
20
15
10
5
0
-2.5
-2
-1.5
-1
-0.5
0
V_{GS} (V)
0.5

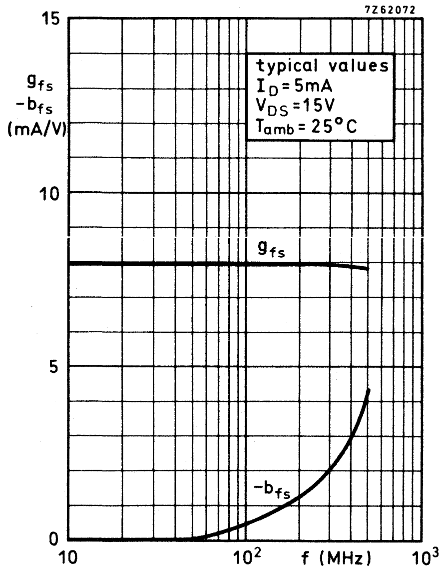

7Z62210
typical values
V_{DS} = 15V
I_D (mA)
V_{GS} = +0.5V
0V
−0.5V
−1V
−1.5V
T_j (°C)
0
5
10
15
20
50
100
150

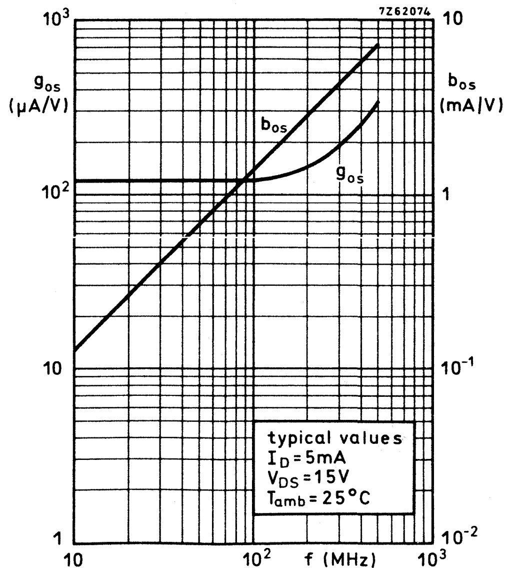

7Z62208
V_{DS} = 15V
V_{BS} = 0
f = 1kHz
T_{amb} = 25°C
$|y_{os}|$ (μA/V)
typ
I_D (mA)
0
100
200
300
400
10
20
30

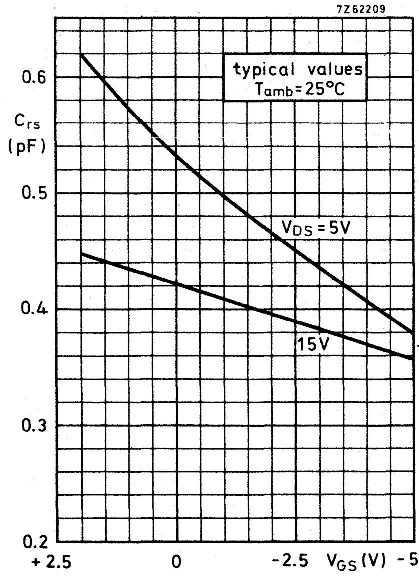

7Z62207
V_{DS} = 15V
V_{BS} = 0
f = 1kHz
T_{amb} = 25°C
$|y_{fs}|$ (mA/V)
typ
I_D (mA)
0
5
10
15
10
20

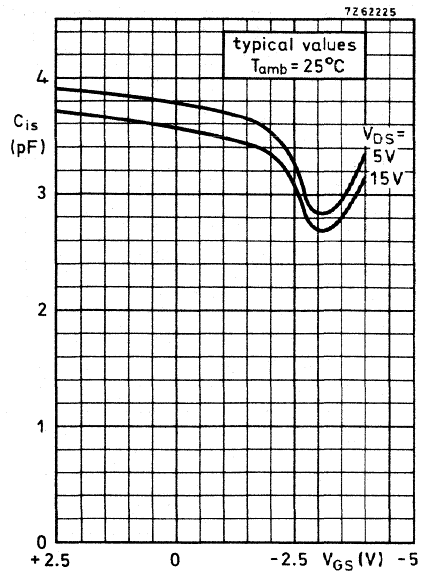

7Z62075
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)
1
10
10^2
10^3
10^{-1}


7Z62073
b_{rs} (μA/V)
C_{rs} (pF)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
C_{rs}
b_{rs}
f (MHz)
10
10^2
10^3
10^4
1
10^{-1}
10^{-2}


7Z62072
g_{fs}
$-b_{fs}$
(mA/V)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
f (MHz)
0
5
10
15
10^2
10^3


7Z62074
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)
1
10
10^2
10^3
10^{-1}
10^{-2}


7Z62209
typical values
T_{amb} = 25°C
C_{rs}
(pF)
0.6
0.5
0.4
0.3
0.2
V_{DS} = 5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5


7Z62225
typical values
T_{amb} = 25°C
C_{is}
(pF)
4
3
2
1
0
V_{DS} =
5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Planar epitaxial symmetrical junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

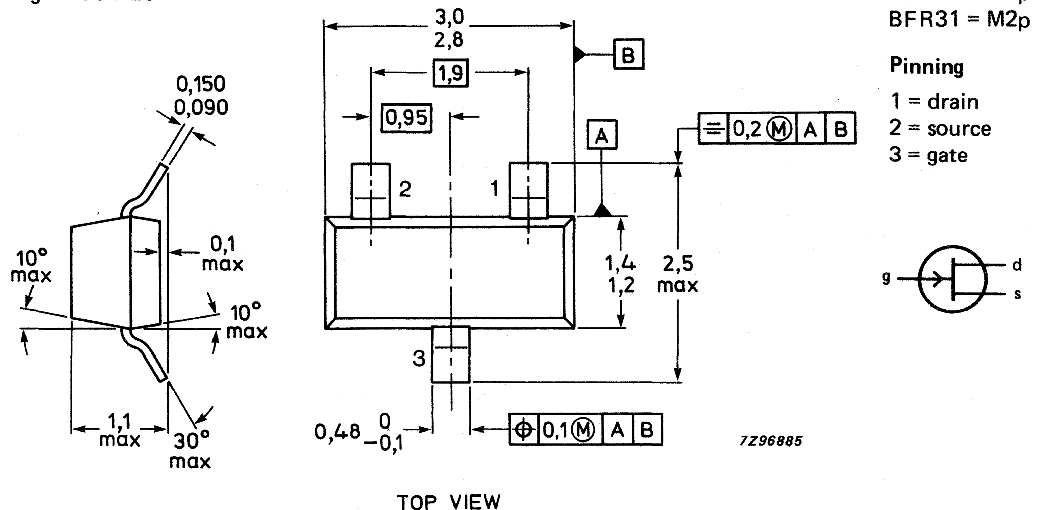
QUICK REFERENCE DATA

			BFR30	BFR31	
Drain-source voltage	$\pm V_{DS}$	max.	25		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25		V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250		mW
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	4	1	mA
		max.	10	5	mA
Transfer admittance (common source) I_D = 1 mA; V_{DS} = 10 V; f = 1 kHz	$\lvert y_{fs}\rvert$	min.	1.0	1.5	mS
		max.	4.0	4.5	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.



Marking code

BFR30 = M1p
BFR31 = M2p

Pinning

1 = drain
2 = source
3 = gate

Note: Drain and source are interchangeable.

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 40 °C*	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		–65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BFR30	BFR31	
Gate cut-off current $-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	max.	0.2	0.2	nA
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	4	1	mA
		max.	10	5	mA
Gate-source voltage I_D = 1 mA; V_{DS} = 10 V	$-V_{GS}$	min.	0.7	0	V
		max.	3.0	1.3	V
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	max.	4.0	2.0	V
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	max.	5	2.5	V
y parameters					
Transfer admittance at f = 1 kHz; T_{amb} = 25 °C I_D = 1 mA; V_{DS} = 10 V	$\|y_{fs}\|$	min.	1.0	1.5	mS
		max.	4.0	4.5	mS
I_D = 200 μA; V_{DS} = 10 V	$\|y_{fs}\|$	min.	0.5	0.75	mS
Output admittance at f = 1 kHz I_D = 1 mA; V_{DS} = 10 V	$\|y_{os}\|$	max.	40	25	μS
I_D = 200 μA; V_{DS} = 10 V	$\|y_{os}\|$	max.	20	15	μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

y parameters (continued)

			BFR30	BFR31	
Input capacitance at f = 1 MHz					
I_D = 1 mA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
I_D = 200 μA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
Feedback capacitance at f = 1 MHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
I_D = 200 μA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
Equivalent noise voltage					
I_D = 200 μA; V_{DS} = 10 V B = 0.6 to 100 Hz	V_n	max.	0.5	0.5	μV

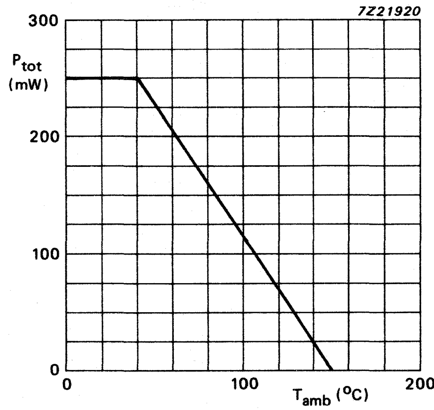


Fig.2 Power derating curve.

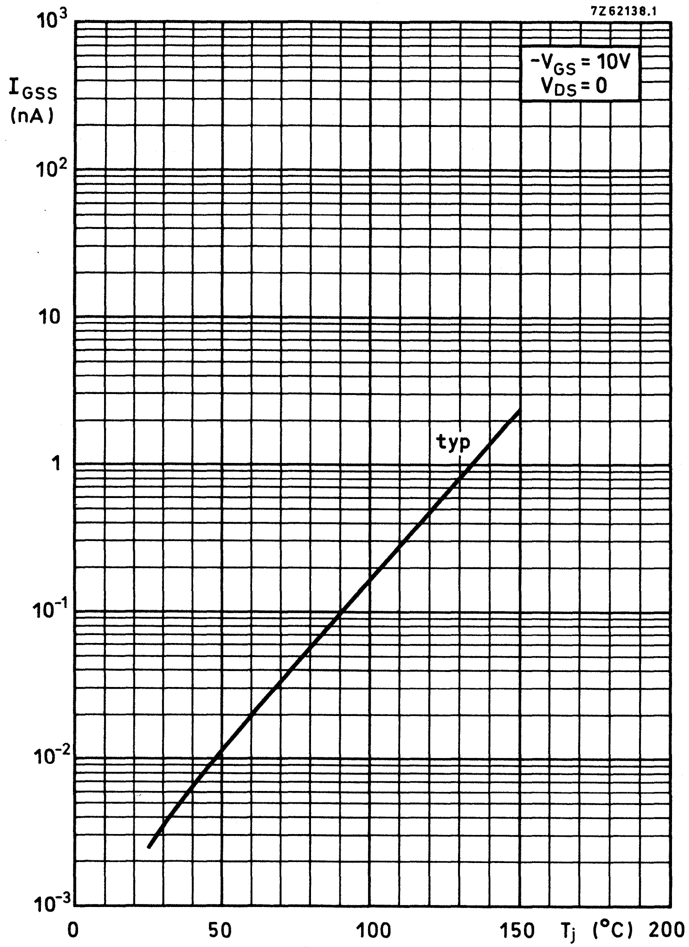


Fig.3.

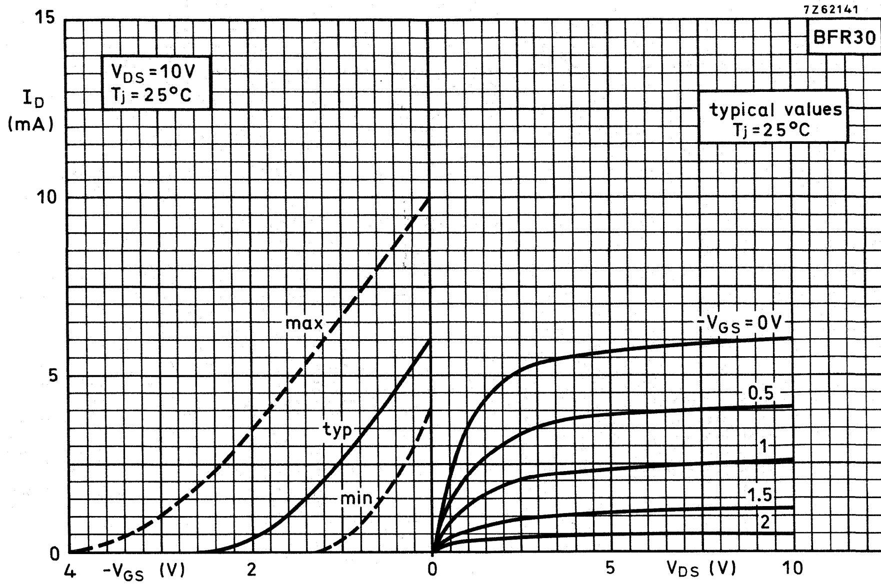


Fig.4.

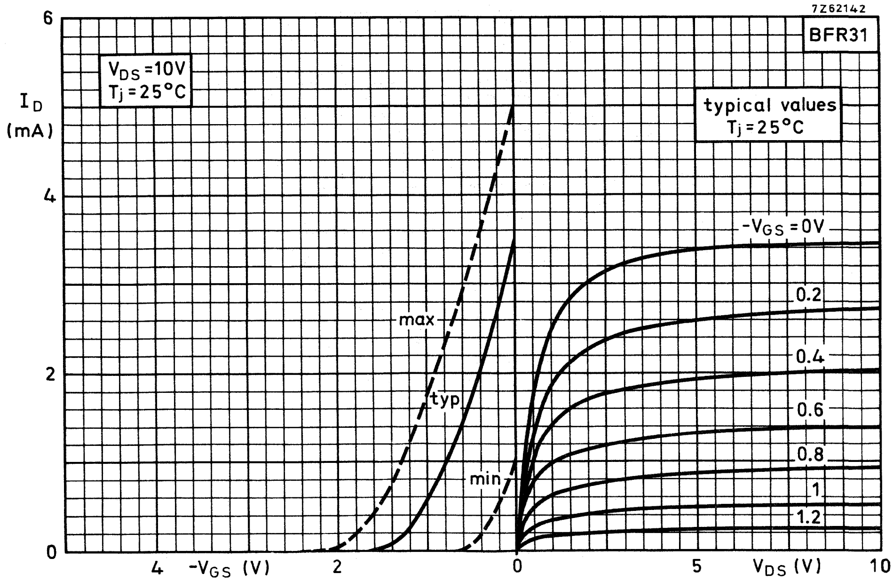


Fig.5.

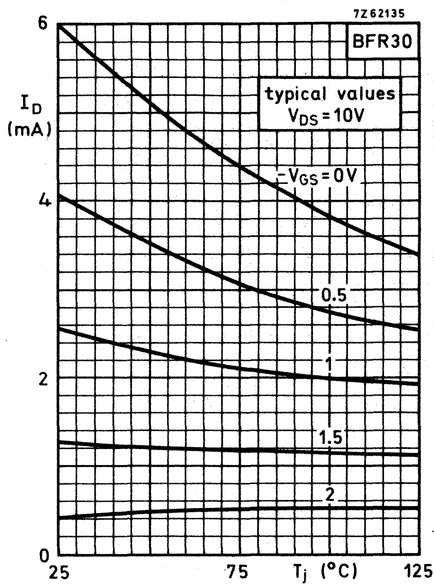


Fig.6.

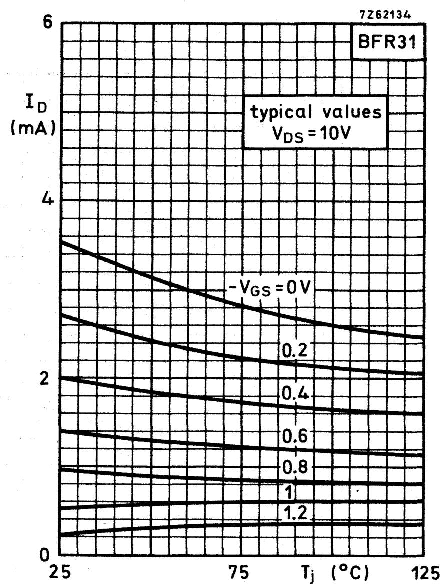


Fig.7.

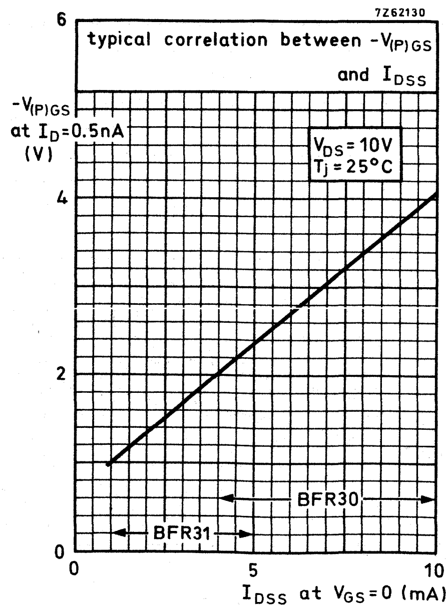


Fig.8.

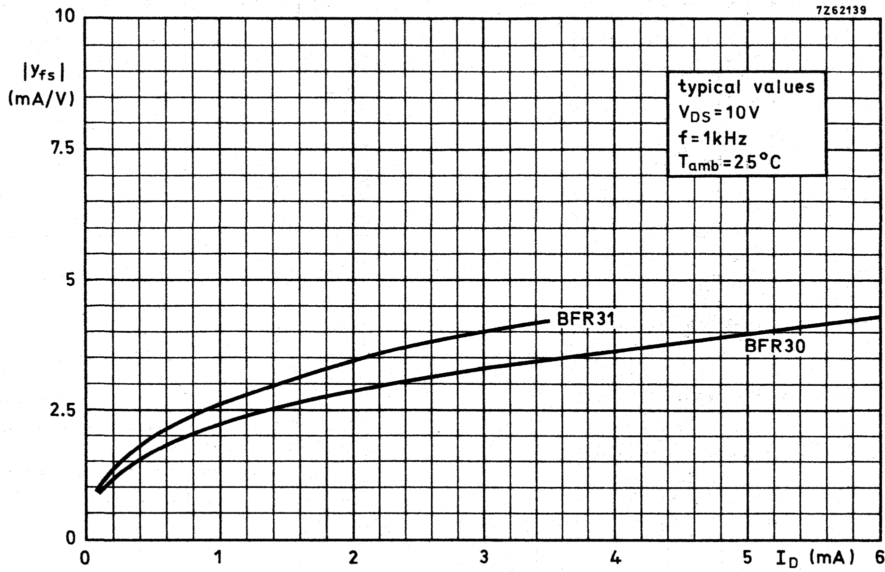


Fig.9.

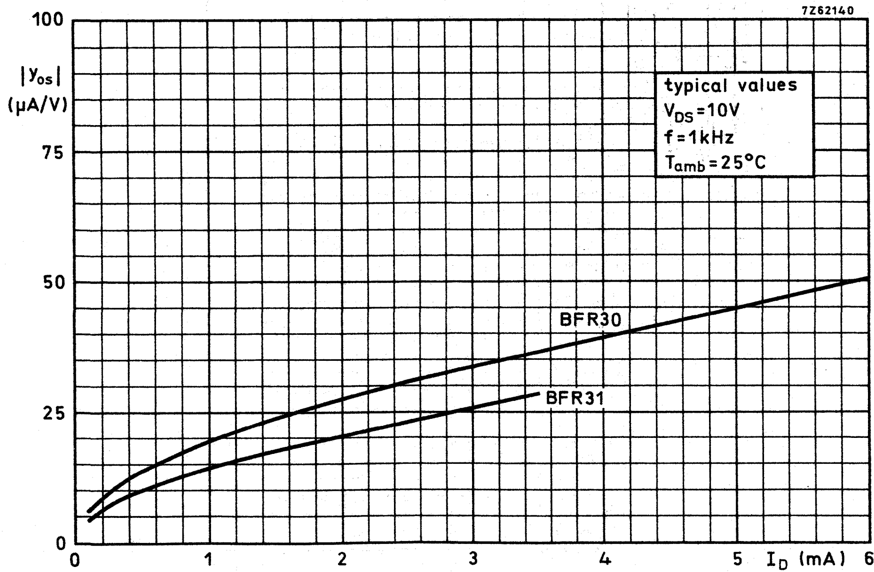


Fig.10.

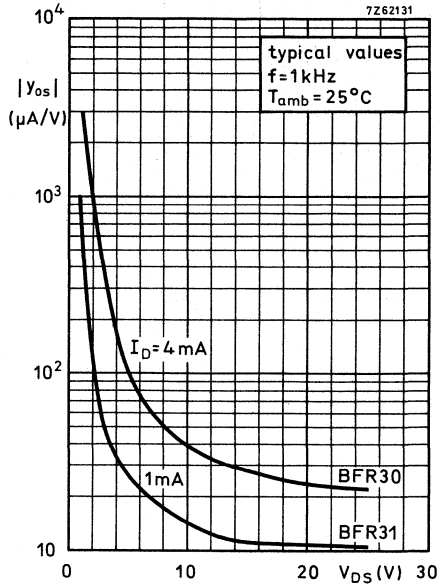


Fig.11.

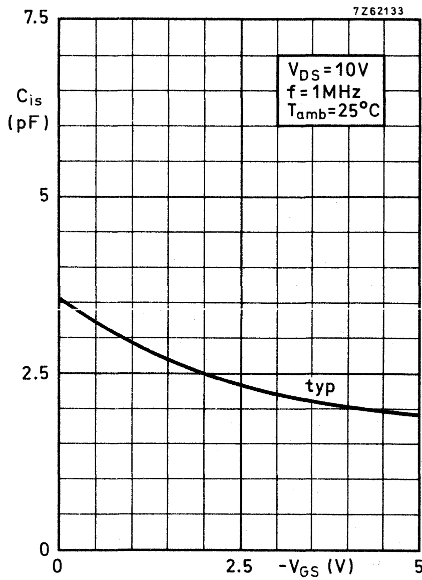


Fig.12.

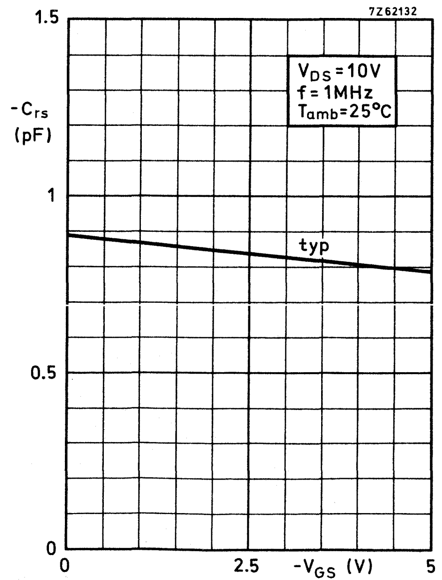


Fig.13.

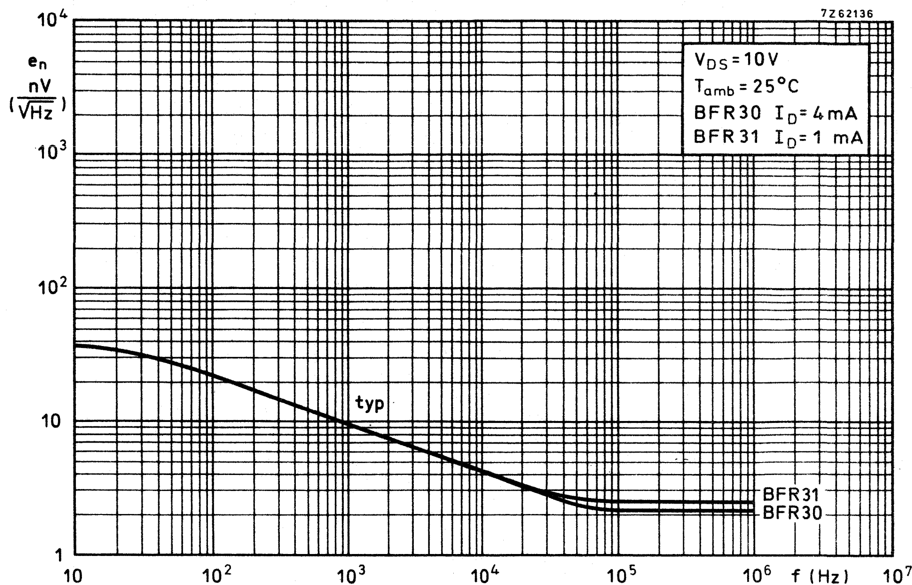


Fig.14.

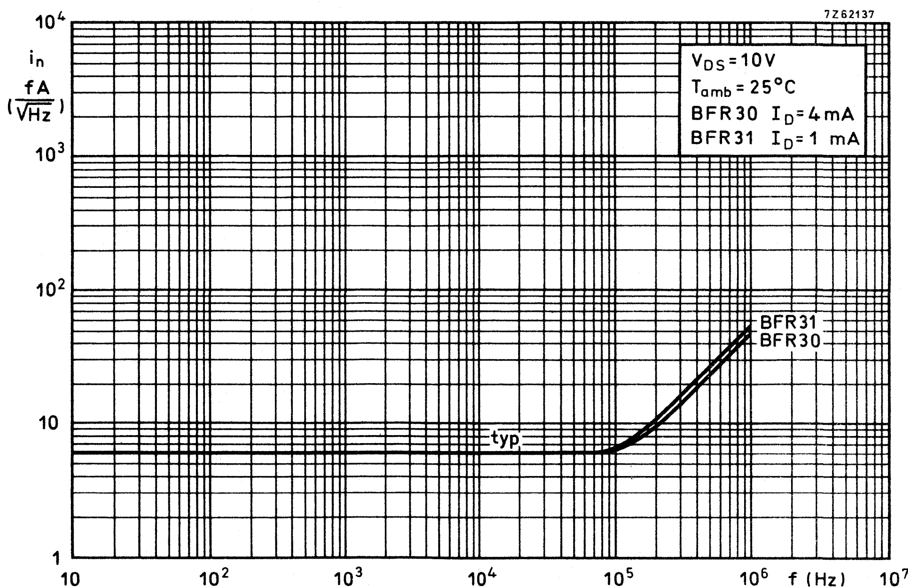


Fig.15.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a metal TO-72 envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

The tetrode configuration, a series arrangement of two gate controlled channels, offers:

a) very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.
b) excellent signal handling capability over the entire gain control range.
c) low noise figure combined with high gain.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	175	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\|y_{fs}\|$	typ.	15	mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	5.5	pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V G_S = 1.2 mA; $-B_S$ = 5.7 mS; f = 200 MHz	F	typ.	2.3	dB

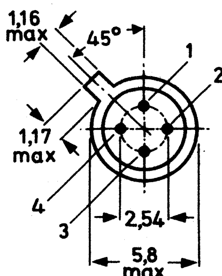
MECHANICAL DATA

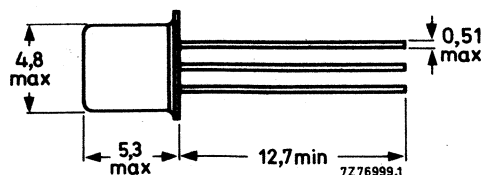
Dimensions in mm

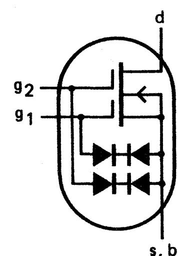
Fig.1 TO-72.

Source and substrate connected to the case.

Pinning:
1 = drain
2 = gate 2
3 = gate 1
4 = source







Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	50	mA
Drain current (peak value)	I_{DM}	max.	100	mA
Gate 1-source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to + 175		°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500	K/W

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$

Parameter	Symbol		Value
Gate cut-off currents			
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	10 nA
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$; $T_j = 150\ ^oC$	$\pm I_{G1-SS}$	max.	10 μA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	10 nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$; $T_j = 150\ ^oC$	$\pm I_{G2-SS}$	max.	10 μA
Gate-source breakdown voltages			
$\pm I_{G1-SS} = 0.1$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS} = 0.1$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20 V
Drain current			
$V_{DS} = 10$ V; $V_{G1-S} = 0$; $+V_{G2-S} = 4$ V	I_{DSS}		20 to 55 mA
Gate 1-source voltage			
$I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$-V_{G1-SS}$		0.6 to 2.1 V
Gate-source cut-off voltages			
$I_D = 10$ μA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$-V_{(P)G1-S}$		1.5 to 3.8 V
$I_D = 10$ μA; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$		1.5 to 3.4 V

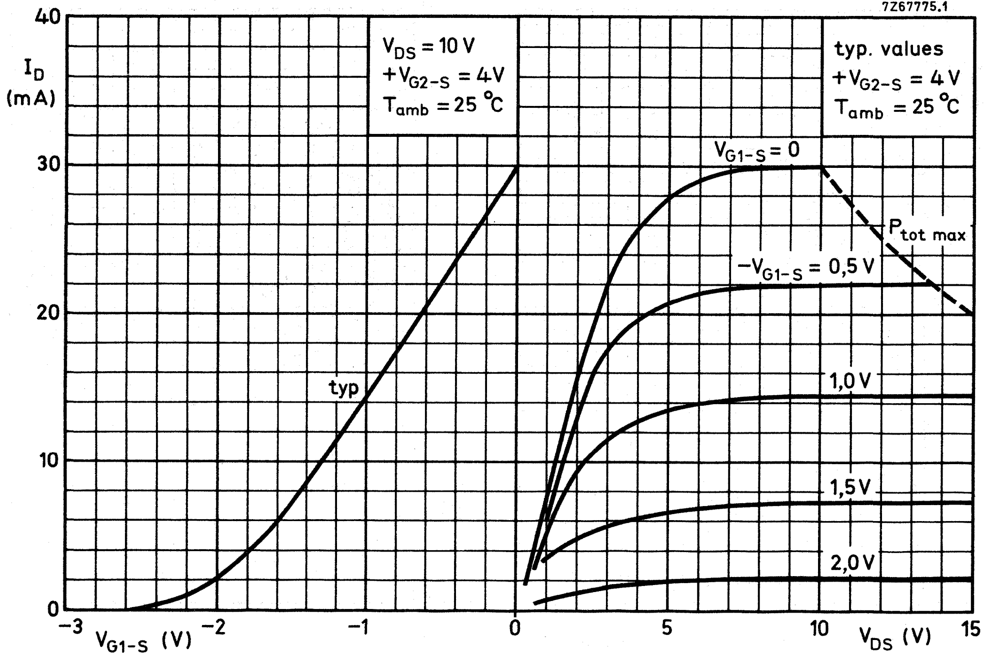
DYNAMIC CHARACTERISTICS

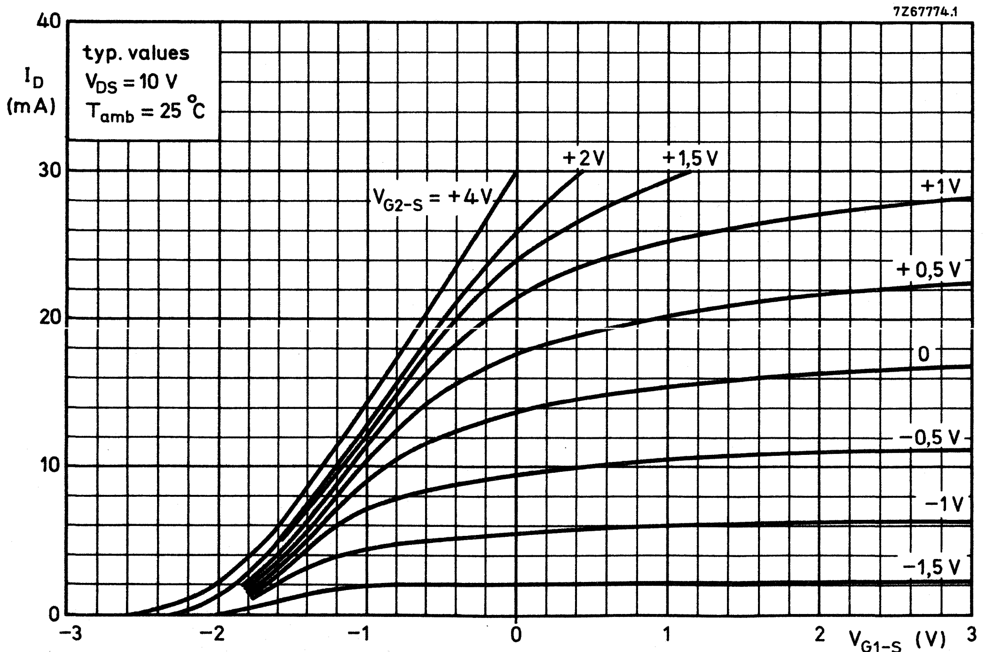
Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V; $T_{amb} = 25\ ^oC$

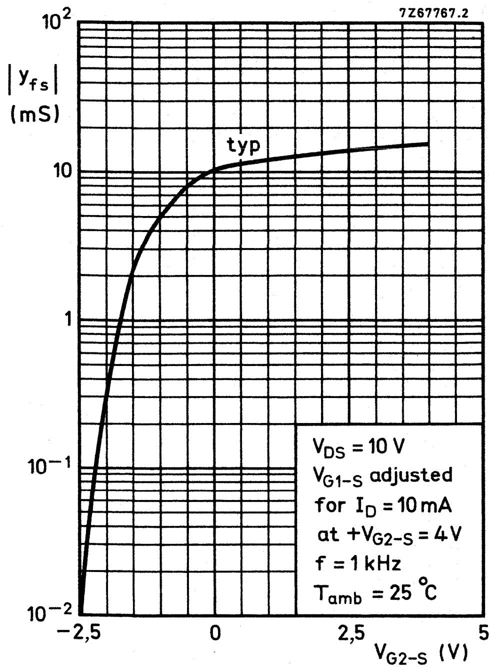
Parameter	Symbol		Value
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	12 mS
		typ.	15 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	5.5 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	3.5 pF
Noise figure at optimum source admittance			
$G_S = 0.95$ mS; $-B_S = 5.0$ mS; f = 100 MHz	F	typ.	1.9 dB
$G_S = 1.20$ mS; $-B_S = 5.7$ mS; f = 200 MHz	F	typ.	2.3 dB
		max.	3.0 dB
Cross modulation at f = 200 MHz			
Wanted signal at f_o = 197.5 MHz			
Unwanted signal at f_{int} = 202.5 MHz			
Interference voltage at g_1 for K = 1%	V_{int}	typ.	100 mV (note 1)

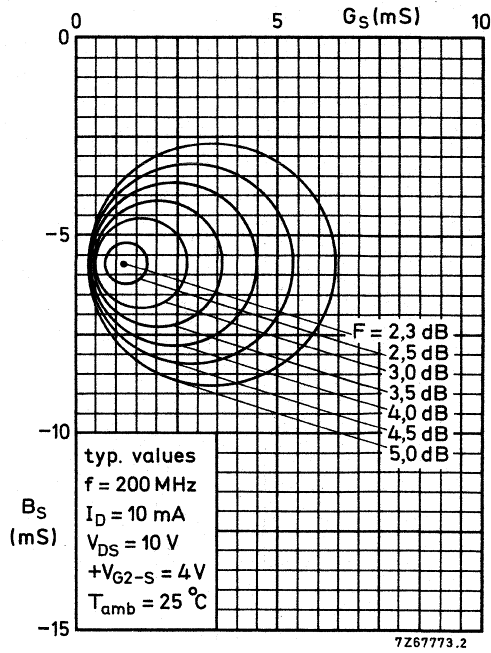
Note

1. Cross modulation is defined here as the voltage at g_1 of an unwanted signal with 80% modulation depth, giving 0.8% modulation depth on the wanted signal (a.m. definition).


7Z67775.1
I_D (mA)
V_{DS} = 10 V
$+V_{G2-S}$ = 4 V
T_{amb} = 25 °C
typ. values
$+V_{G2-S}$ = 4 V
T_{amb} = 25 °C
typ
V_{G1-S} = 0
$P_{tot\ max}$
$-V_{G1-S}$ = 0,5 V
1,0 V
1,5 V
2,0 V
V_{G1-S} (V)
V_{DS} (V)


7Z67774.1
I_D (mA)
typ. values
V_{DS} = 10 V
T_{amb} = 25 °C
V_{G2-S} = +4 V
+2 V
+1,5 V
+1 V
+0,5 V
0
−0,5 V
−1 V
−1,5 V
V_{G1-S} (V)





circles of constant noise figure

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October 1990

BFR200

N-channel junction field-effect transistor

FEATURES

- Ultra-low leakage performance ($-I_{GSS}$ max. 3 pA); important for use in highly sensitive equipment, such as burglar alarms, infrared sensors, etc.
- Insensitive to radio frequency interference (RFI), owing to an integrated low pass filter.
- Input protected against successive voltage surges by a forward and reverse integrated diode.
- Low LF noise performance (20 nV/√Hz).

DESCRIPTION

Silicon asymmetrical n-channel junction FET in a surface mount SOT143 envelope, with an integrated RC low pass filter and two anti-parallel diodes connected to the gate. It is designed primarily for use as a source follower in infrared detectors, burglar alarms, electret microphones, smoke alarms and radiation detectors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	-	30	V
I_{DSS}	drain current	0.2	3.5	mA
$-V_{GS(off)}$	gate-source cut-off voltage	0.5	2	V

MECHANICAL DATA

Dimensions in mm

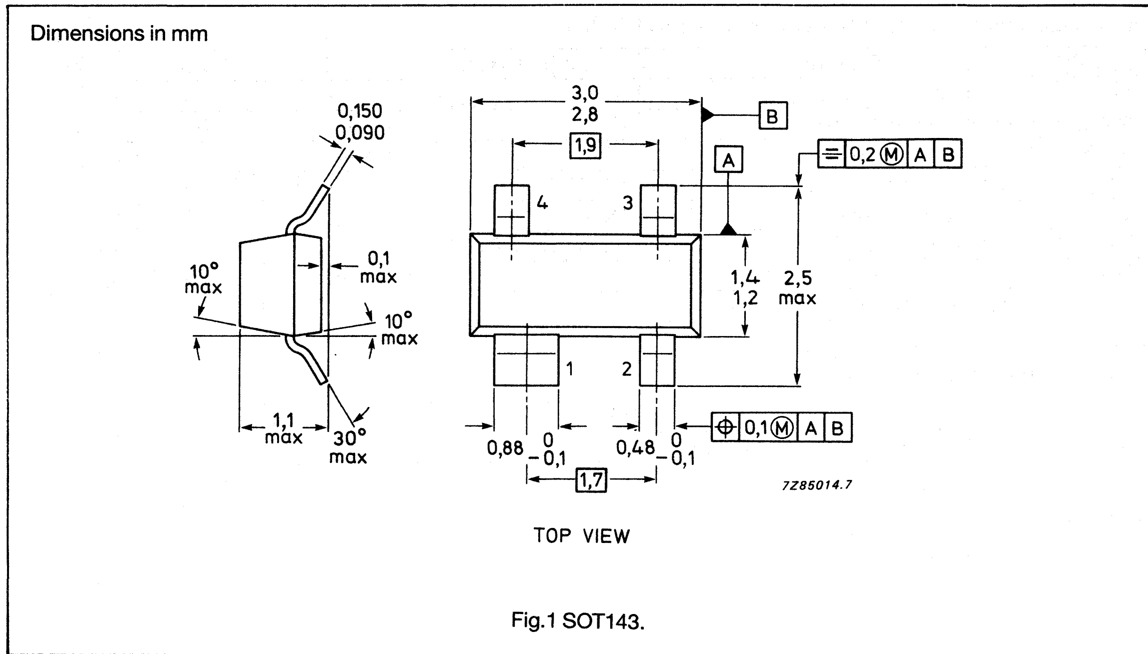


Fig.1 SOT143.

PIN CONFIGURATION

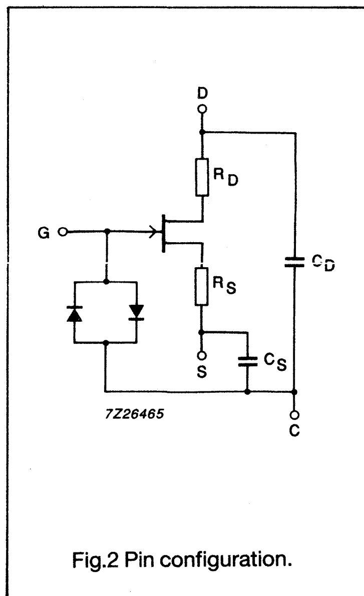


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	gate
2	common
3	source
4	drain

Marking: BFR200 = M20

N-channel junction field-effect transistor BFR200

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	30	V
$-V_{GSO}$	gate-source voltage		-	30	V
$-V_{GDO}$	gate-drain voltage		-	30	V
I_D	drain current	DC	-	20	mA
I_G	forward gate current	DC	-	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	250	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Notes

1. Mounted on FR4 printboard.

N-channel junction field-effect transistor — BFR200

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$V_{DS} = 0$ $-I_G = 1\ \mu A$	30	-	-	V
I_{DSS}	drain current	$V_{DS} = 6$ V $V_{GS} = 0$	0.2	-	3.5	mA
$-I_{GSS}$	gate-source leakage current (note 1)	$-V_{GS} = 6$ V $V_{DS} = 0$ $V_{GC} = 0$	-	-	3	pA
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 0.1\ \mu A$ $V_{DS} = 6$ V	0.5	-	2	V
V_F	diode forward voltage	$\pm I_F = 10$ mA	0.7	-	1.2	V
R_D	drain resistance		-	800	-	Ω
R_S	source resistance		-	180	-	Ω

Notes

1. Based on level I, AQL 1.5%.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	$V_{DS} = 6$ V $V_{GS} = 0$	1.3	-	-	mS
$\lvert Y_{os} \rvert$	output admittance	$V_{DS} = 6$ V $V_{GS} = 0$	-	40	-	μS
C_{iss}	input capacitance (note 1)	$V_{DS} = 6$ V $V_{GS} = 0$ $V_{GC} = 0$ f = 1 MHz	-	-	6	pF
C_{GC}	diode capacitance	$V_{GC} = 0$ drain and source grounded	-	3	-	pF
C_D	drain decoupling capacitance	$V_{DC} = 0$ gate and source grounded	-	8	-	pF
C_S	source decoupling capacitance	$V_{SC} = 0$ gate and drain grounded	-	8	-	pF

Notes

1. Value is inclusive of the capacitance of the diodes.

N-CHANNEL SILICON FET

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

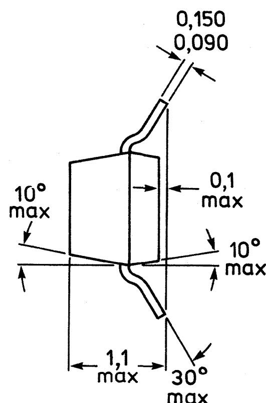
QUICK REFERENCE DATA

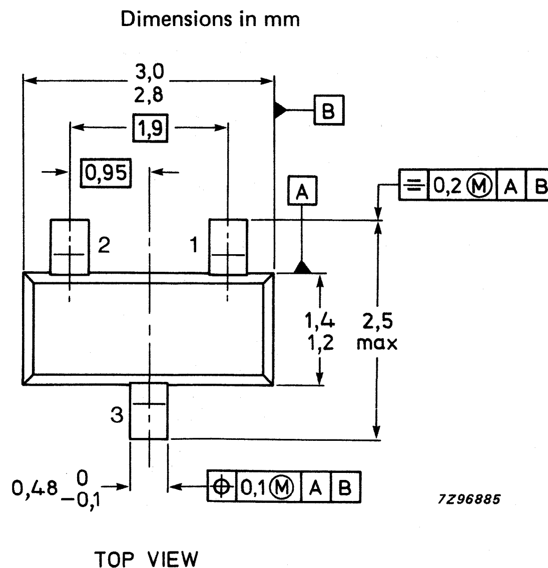
Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	mW
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	> <	0,2 1,5	mA mA
Transfer admittance (common source) I_D = 0,2 mA; V_{DS} = 10 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	mS
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; B = 0,6 to 100 Hz	V_n	<	0,5	μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.





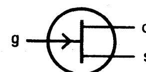
TOP VIEW

Marking code

BFT46 = M3

Pinning

1 = drain
2 = source
3 = gate



Note : Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	10 mA
Gate current	I_G	max.	5 mA
Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off current $-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	$<$	0,2 nA
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	$>$ $<$	0,2 mA 1,5 mA
Gate-source voltage I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	$>$ $<$	0,1 V 1,0 V
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	$<$	1,2 V
y-parameters at f = 1 kHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs}\rvert$	$>$	1,0 mS
Output admittance	$\lvert y_{os}\rvert$	$<$	10 μS
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs}\rvert$	$>$	0,5 mS
Output admittance	$\lvert y_{os}\rvert$	$<$	5 μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{rs}	<	1,5 pF
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C B = 0,6 to 100 Hz	V_n	<	0,5 μV

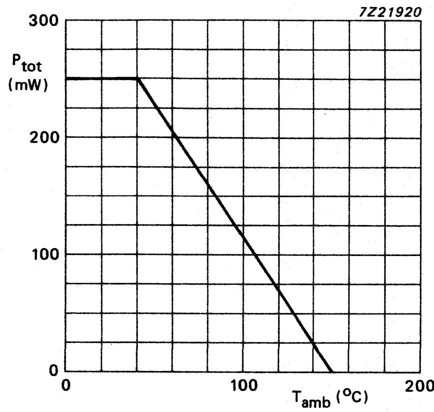


Fig.2 Power derating curve.

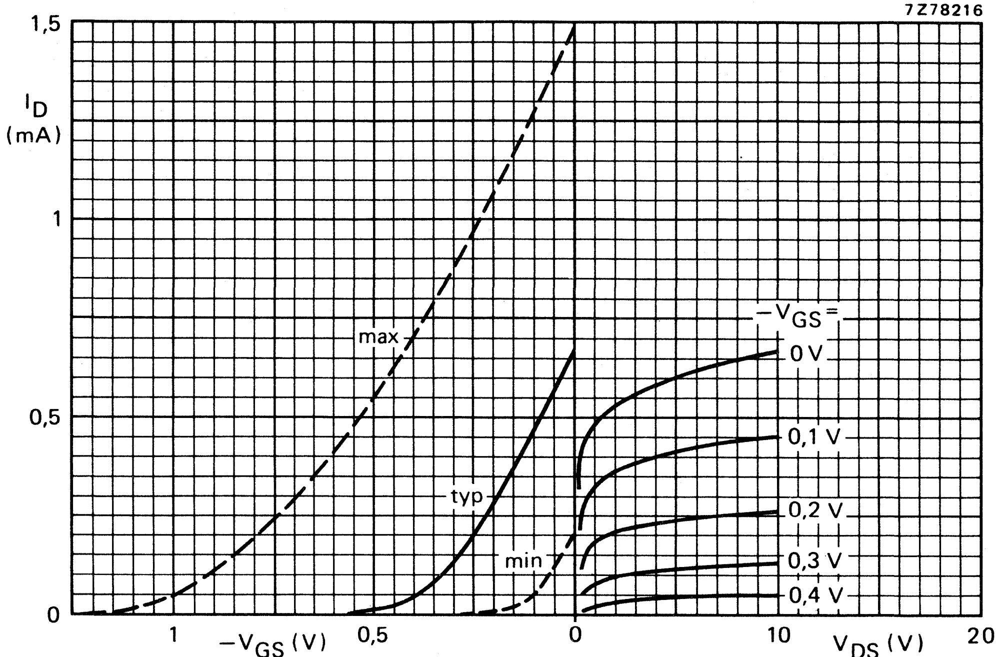


Fig. 3 Typical values. V_{DS} = 10 V; T_j = 25 °C.

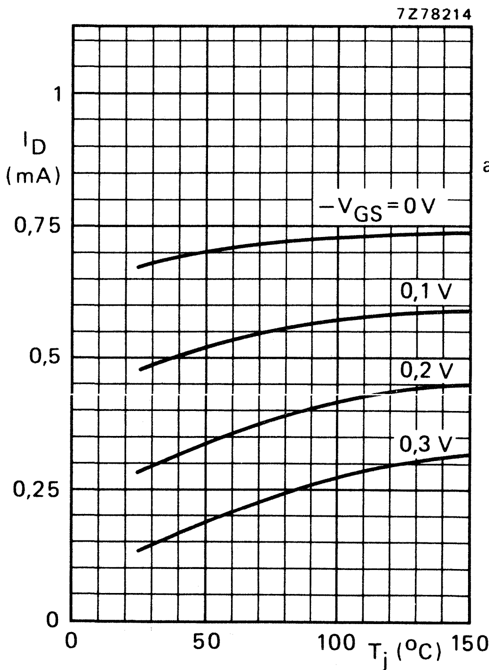


Fig. 4 Typical values. V_{DS} = 10 V.

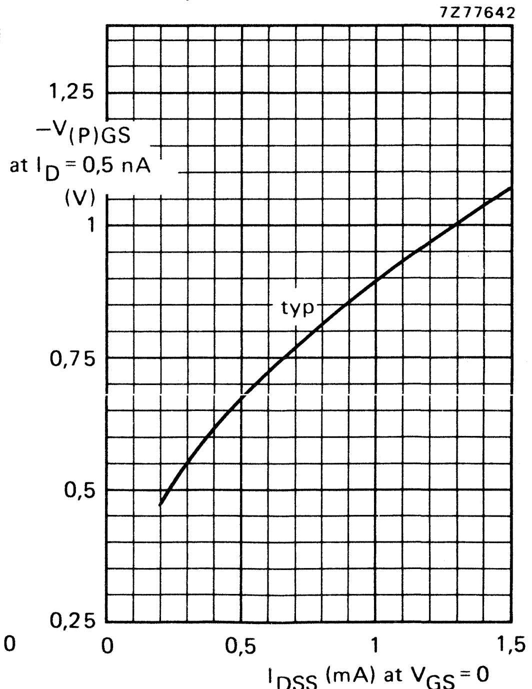


Fig. 5 Correlation between $-V_{(P)GS}$ and I_{DSS}. V_{DS} = 10 V; T_j = 25 °C.

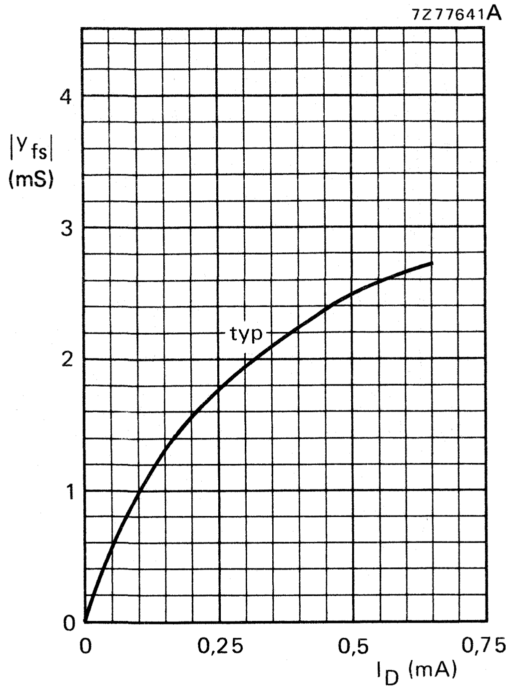


Fig. 6

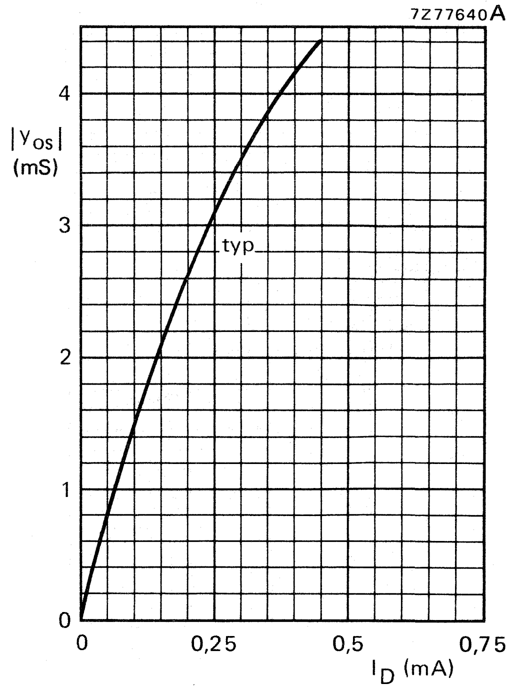


Fig. 7

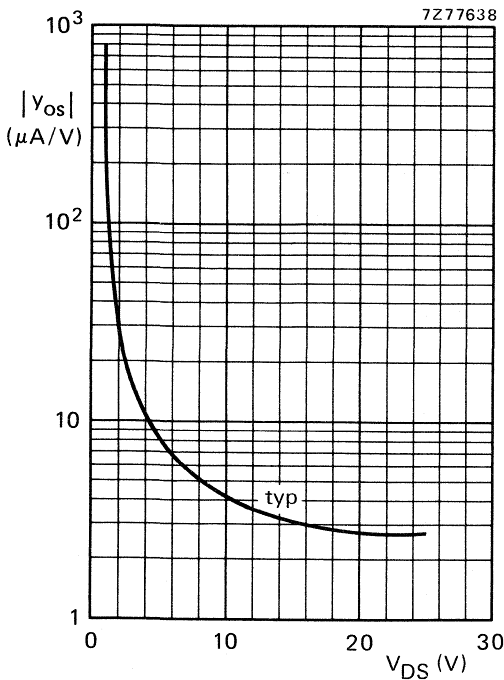


Fig. 8

Fig. 6 $|y_{fs}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 7 $|y_{os}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 8 $|y_{os}|$ versus V_{DS}.
I_D = 0,4 mA; f = 1 kHz; T_{amb} = 25 °C.

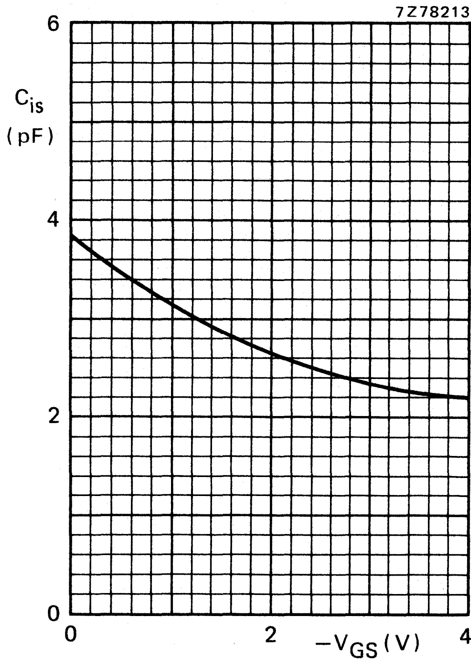


Fig. 9

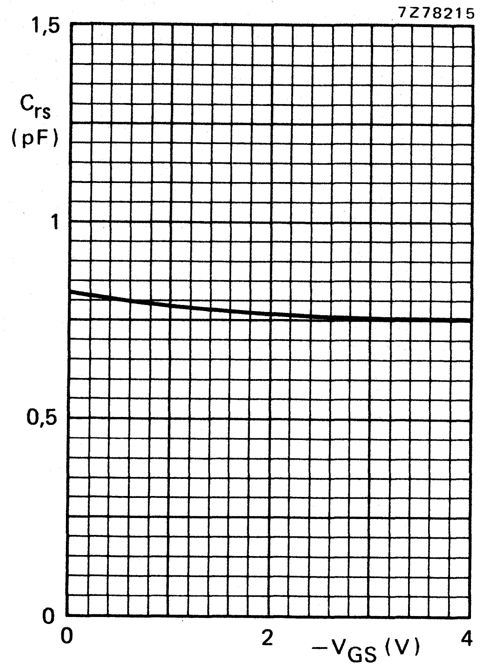


Fig. 10

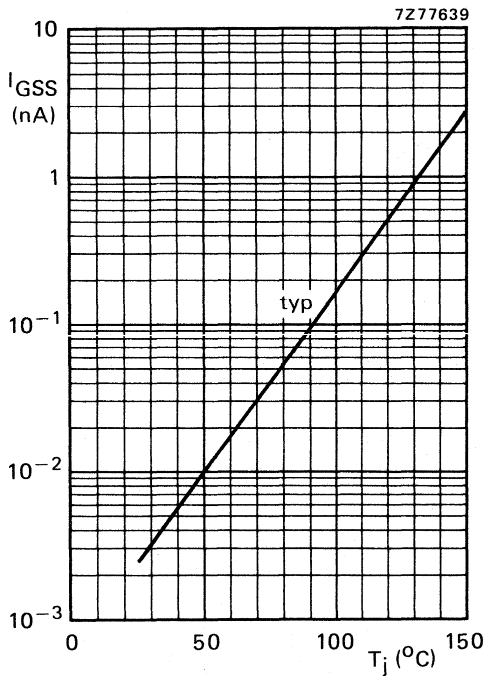


Fig. 11

Fig. 9 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 10 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 11 I_{GSS} versus T_j.
$-V_{GSS}$ = 10V; V_{DS} = 0.

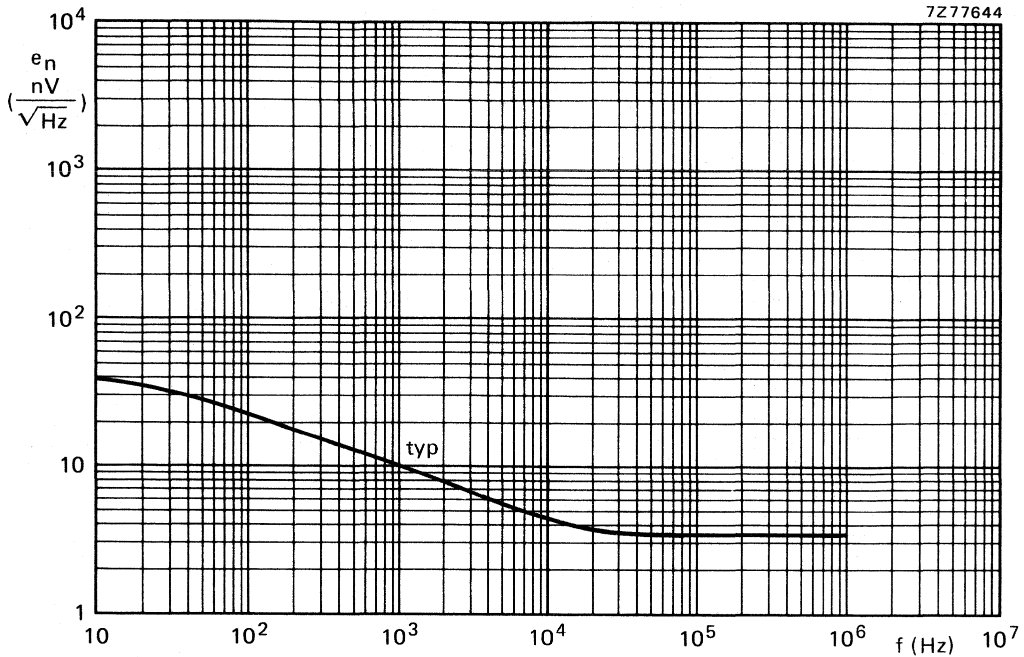


Fig. 12 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

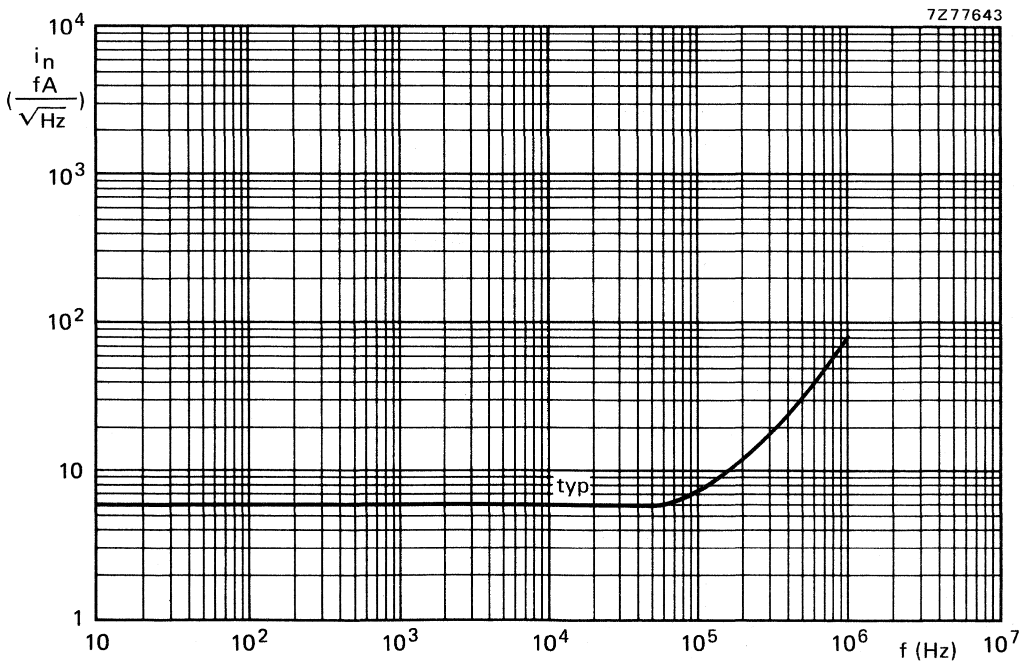


Fig. 13 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

N-channel silicon field-effect transistors

BFU308/309/310

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-18 envelope. They are intended for use in UHF/VHF amplifiers, oscillators and mixers.

PIN CONFIGURATION

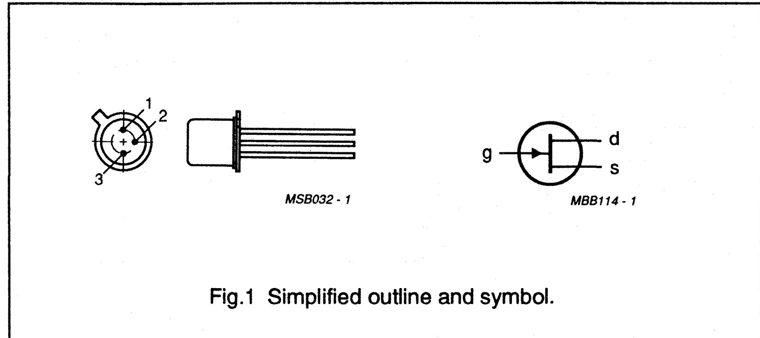


Fig.1 Simplified outline and symbol.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	BFU308		12	60	mA
	BFU309		12	30	mA
	BFU310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	275	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA			
	BFU308		1	6.5	V
	BFU309		1	4	V
	BFU310		2	6.5	V
Y_{fs}	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	275	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	360	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead minimum 10 x 10 mm.

STATIC CHARACTERISTICS

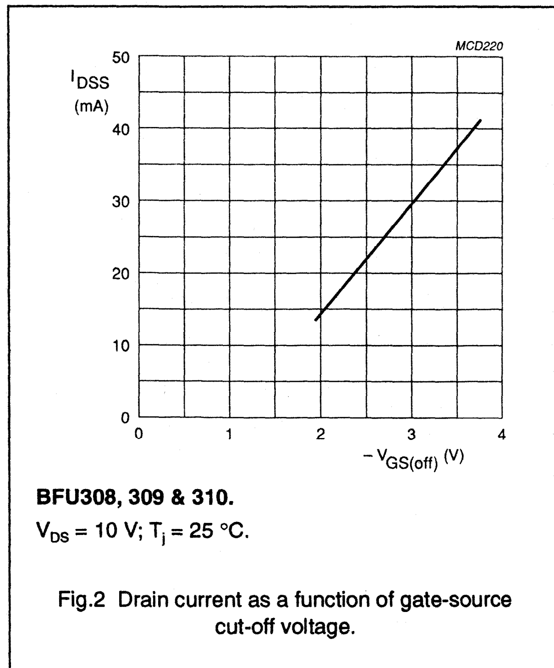
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	–	–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	BFU308		12	–	60	mA
	BFU309		12	–	30	mA
	BFU310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	BFU308		1	–	6.5	V
	BFU309		1	–	4	V
	BFU310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\|Y_{os}\|$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

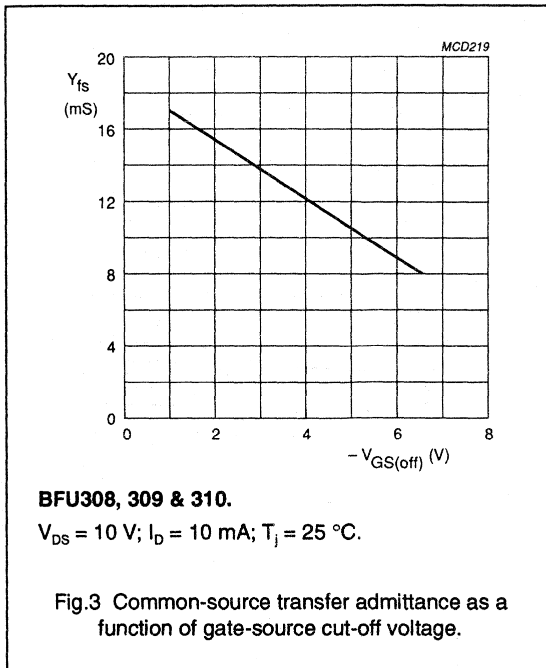
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\overline{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



BFU308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

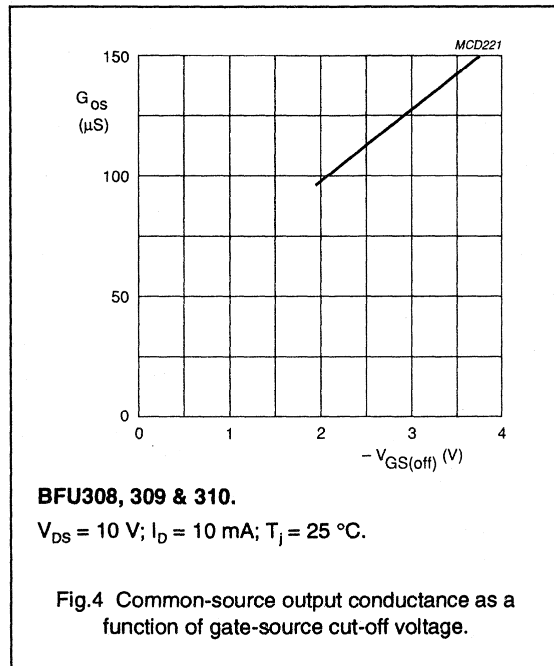
Fig.2 Drain current as a function of gate-source cut-off voltage.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

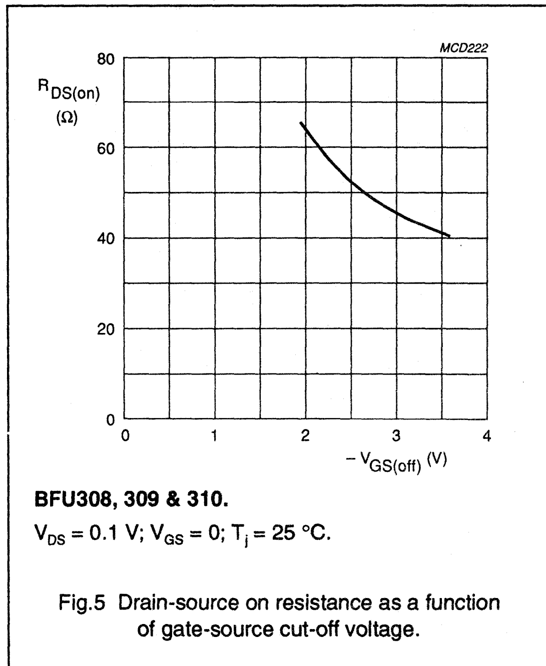
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

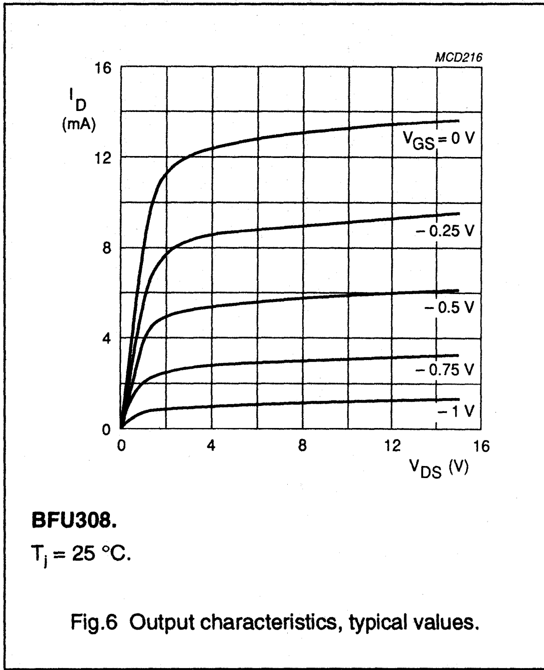
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



BFU308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

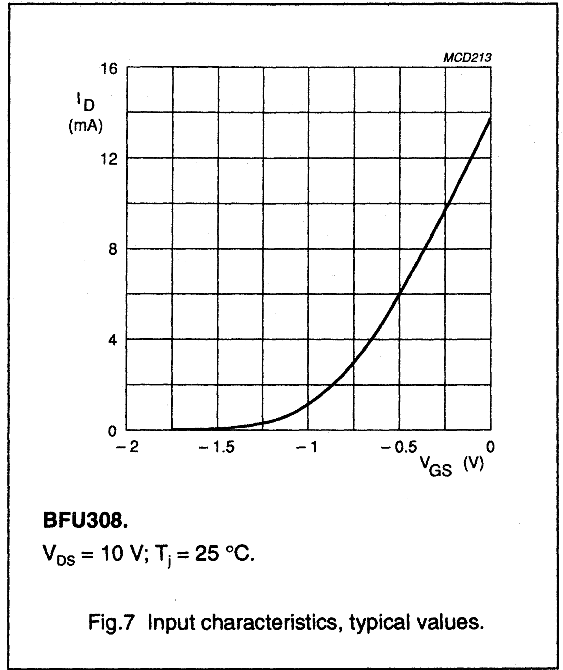
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



BFU308.

$T_j = 25$ °C.

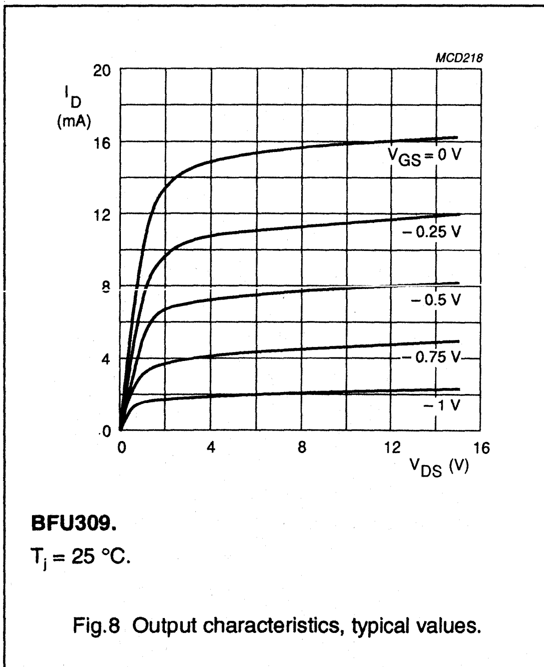
Fig.6 Output characteristics, typical values.



BFU308.

$V_{DS} = 10$ V; $T_j = 25$ °C.

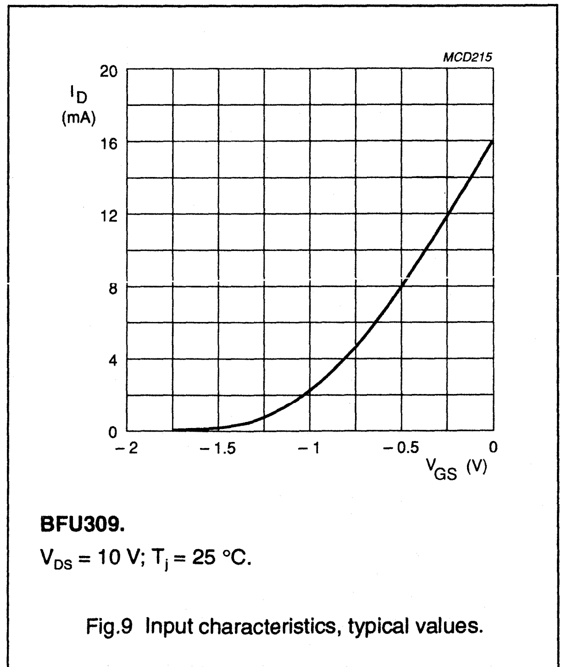
Fig.7 Input characteristics, typical values.



BFU309.

$T_j = 25$ °C.

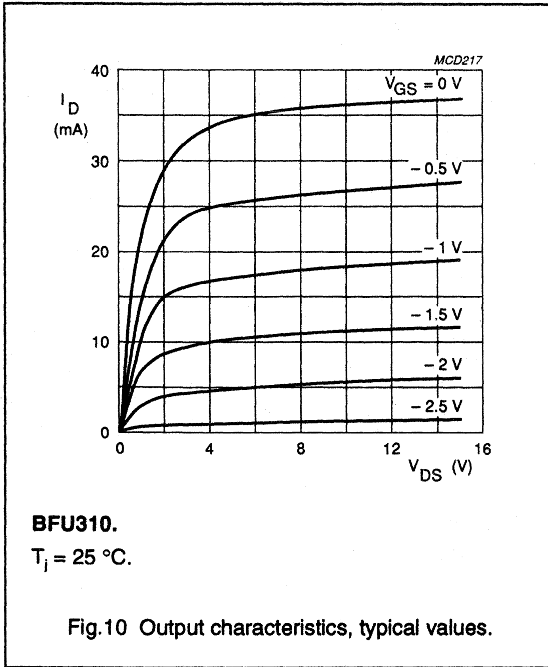
Fig.8 Output characteristics, typical values.



BFU309.

$V_{DS} = 10$ V; $T_j = 25$ °C.

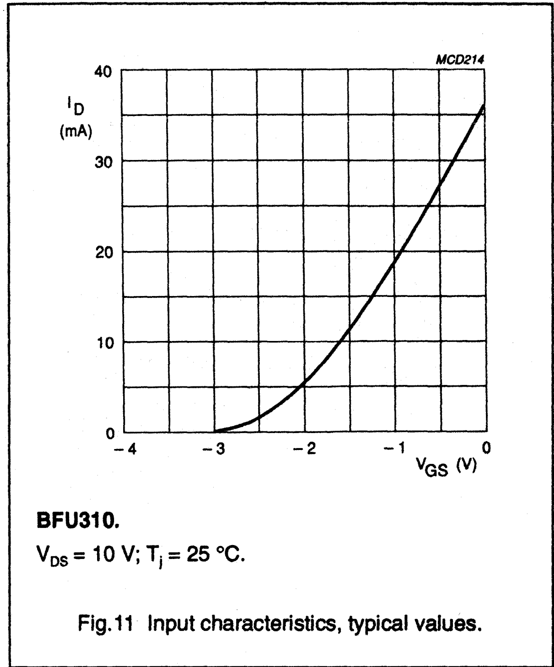
Fig.9 Input characteristics, typical values.



BFU310.

T_j = 25 °C.

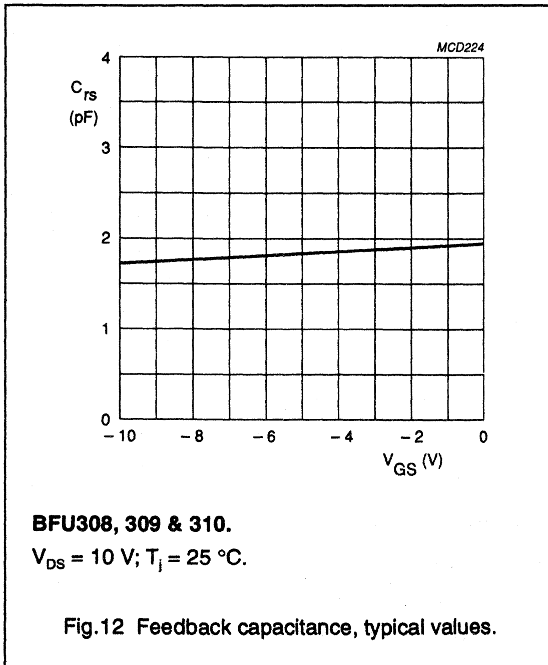
Fig.10 Output characteristics, typical values.



BFU310.

V_{DS} = 10 V; T_j = 25 °C.

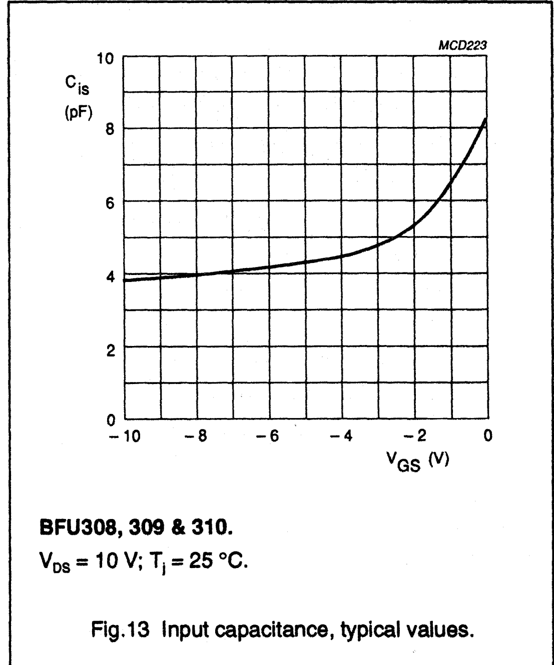
Fig.11 Input characteristics, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

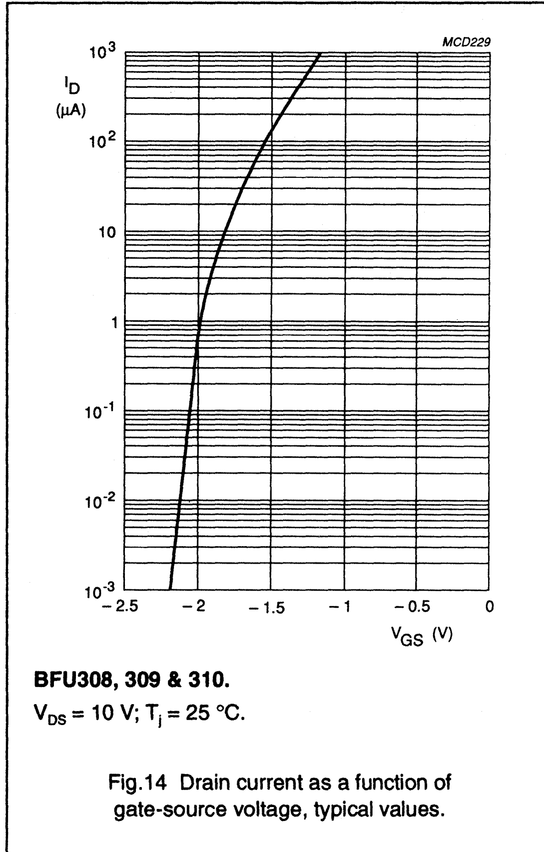
Fig.12 Feedback capacitance, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

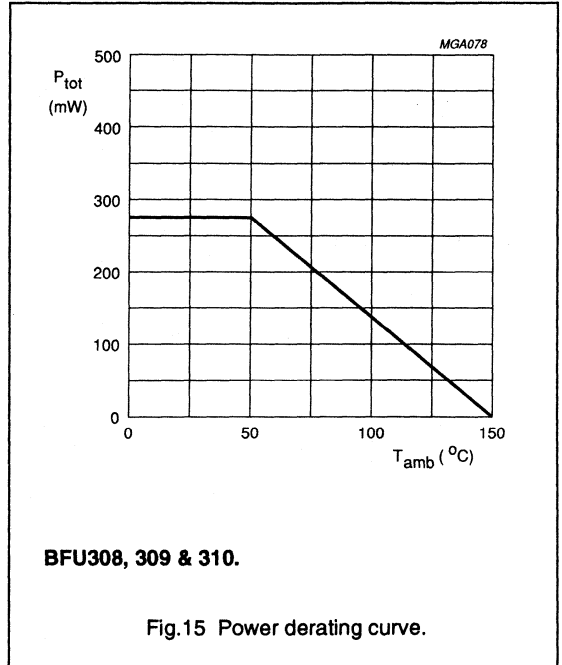
Fig.13 Input capacitance, typical values.



BFU308, 309 & 310.

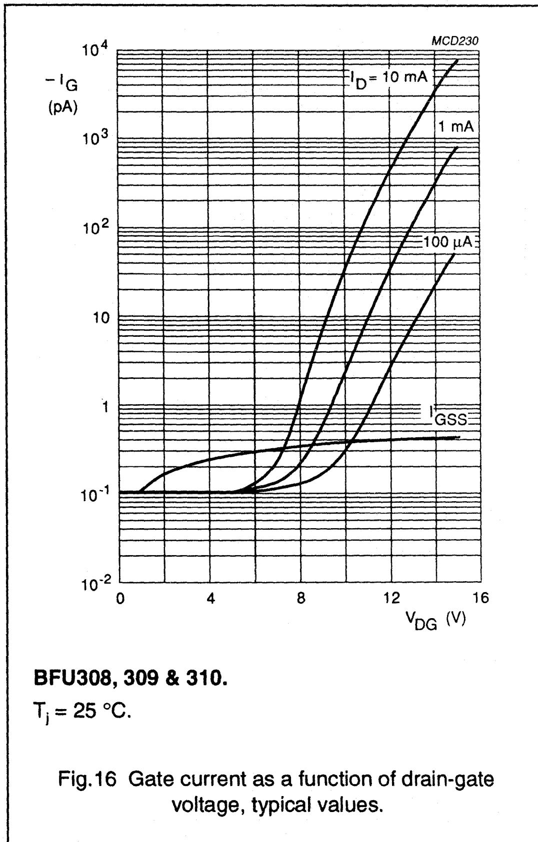
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



BFU308, 309 & 310.

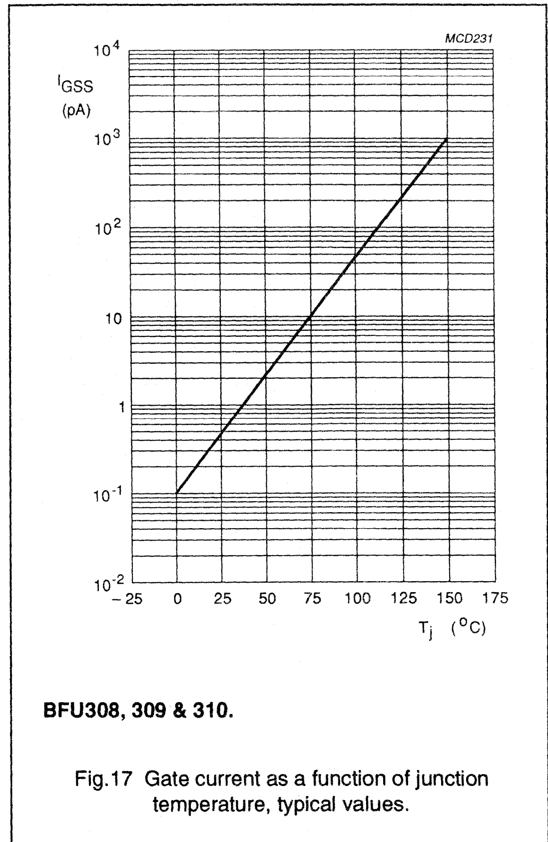
Fig.15 Power derating curve.



BFU308, 309 & 310.

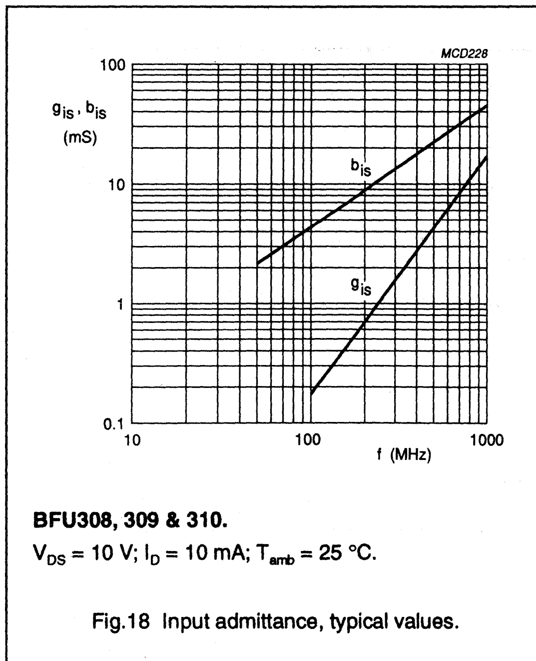
$T_j = 25$ °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



BFU308, 309 & 310.

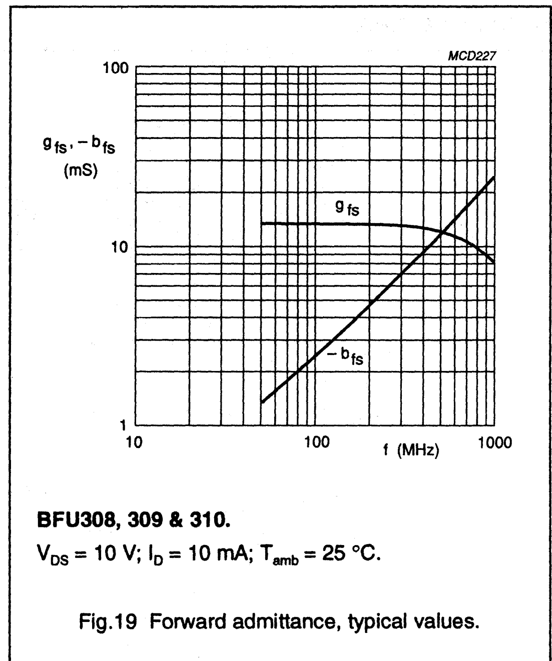
Fig.17 Gate current as a function of junction temperature, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

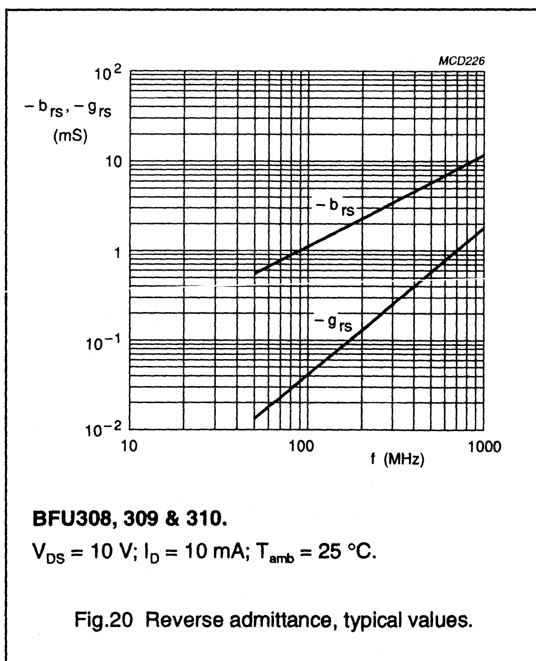
Fig.18 Input admittance, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

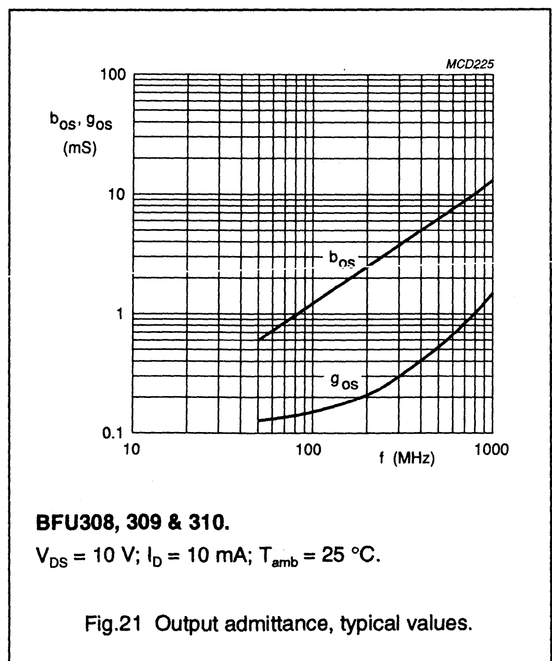
Fig.19 Forward admittance, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.

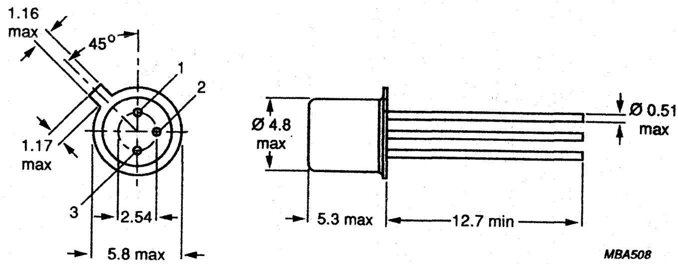


BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

PACKAGE OUTLINE



Dimensions in mm.

Gate connected to case.

Drain and source are interchangeable.

Fig.22 TO-18.

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250		mW
			BFW10	**BFW11**	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> <	8 20	4 10	mA mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\|y_{fs}\|$	>	3,2	3,2	mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0 f = 100 MHz; R_G = 1 kΩ	F	<	2,5	2,5	dB
Equivalent noise voltage f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

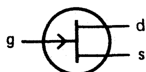
MECHANICAL DATA

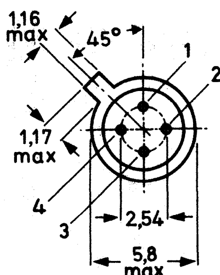
Dimensions in mm

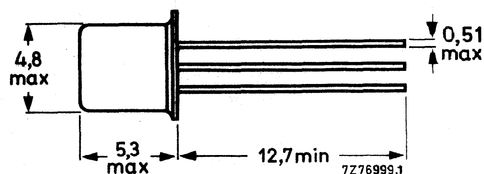
Fig.1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

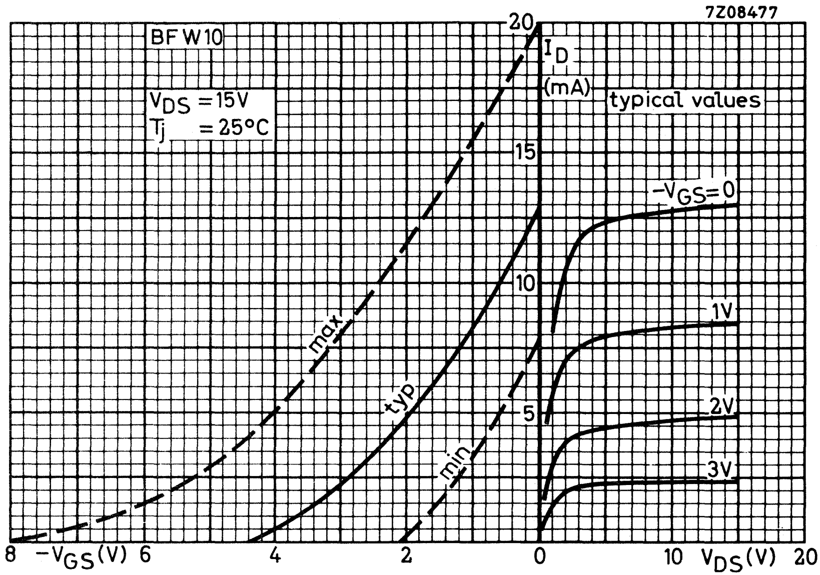
From junction to ambient	$R_{th\ j\text{-}a}$	=	590	K/W

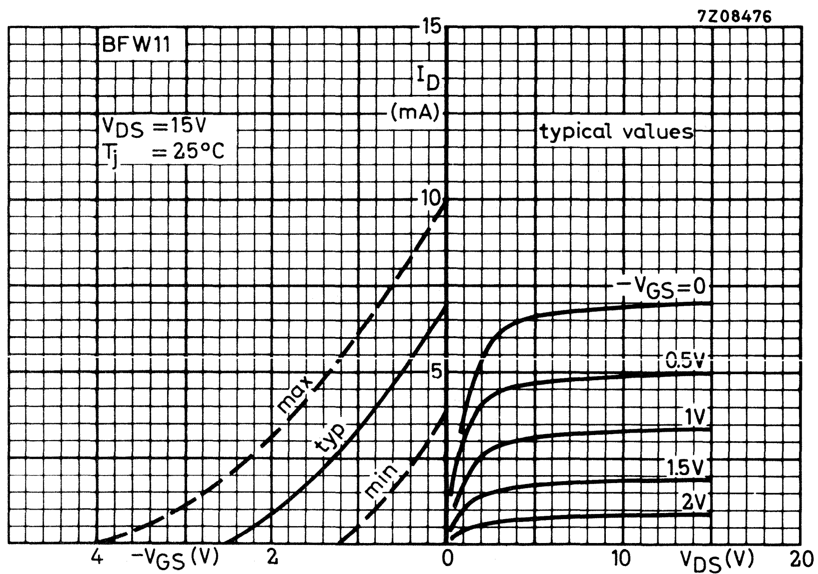
CHARACTERISTICS

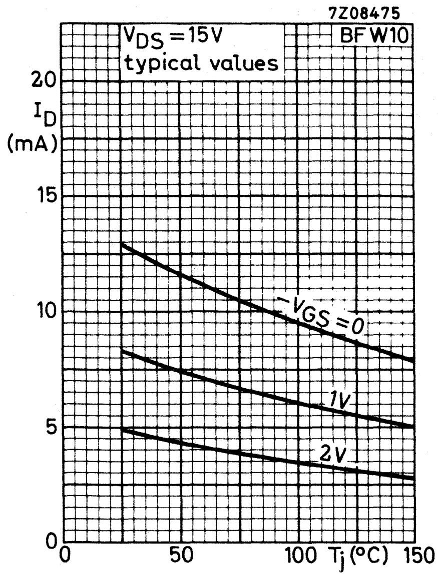
T_j = 25 °C unless otherwise specified

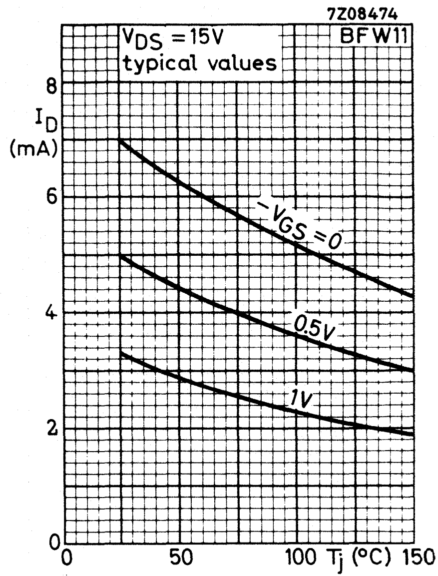
			BFW10	BFW11	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.5	0.5	μA
Drain current*					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source voltage					
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$	>	2.0		V
		<	7.5		V
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>		1.25	V
		<		4.0	V
Gate source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
y parameters					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 1 kHz					
Transfer admittance	$\|y_{fs}\|$	>	3.5	3.0	mS
		<	6.5	6.5	mS
Output admittance	$\|y_{os}\|$	<	85	50	μS
f = 1 MHz; input capacitance	C_{is}	typ.	4	4	pF
		<	5	5	pF
Feedback capacitance	C_{rs}	typ.	0.6	0.6	pF
		<	0.80	0.80	pF
f = 200 MHz; transfer admittance	$\|y_{fs}\|$	>	3.2	3.2	mS
Input capacitance	g_{is}	<	800	800	μS
Output capacitance	g_{os}	<	200	100	μS
Noise figure at f = 100 MHz; R_G = 1 kΩ					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
input tuned to minimum noise	F	<	2.5	2.5	dB
Equivalent noise voltage					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	nV/$\sqrt{Hz}$

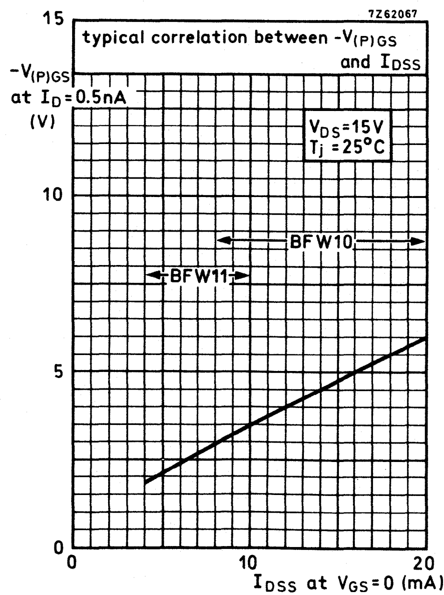
* Measured under pulsed conditions.

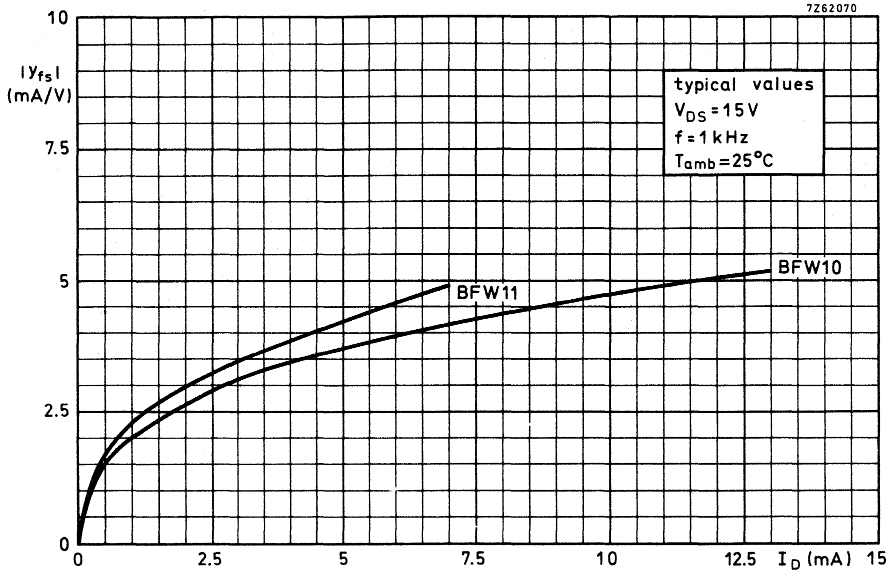

7Z08477
BFW10
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
1V
2V
3V
max
typ
min
20
15
10
5
8
$-V_{GS}$ (V)
6
4
2
0
10
V_{DS} (V)
20

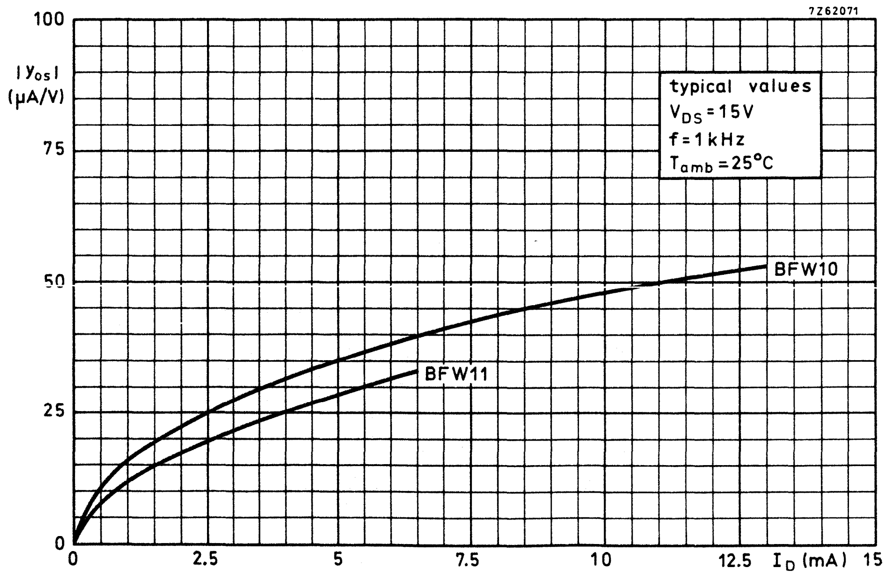

7Z08476
BFW11
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
0.5V
1V
1.5V
2V
max
typ
min
15
10
5
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

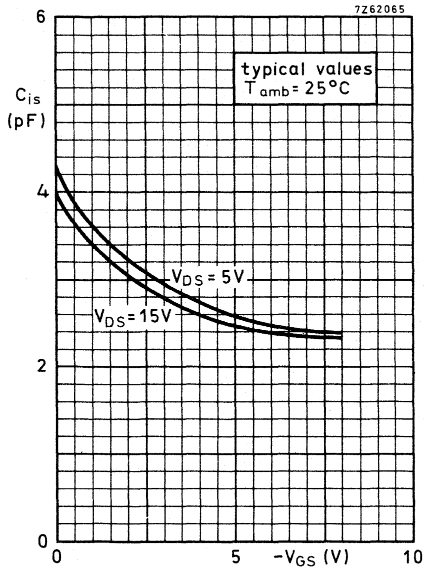

7Z08475
V_{DS} = 15 V
typical values
BFW10
I_D (mA)
$-V_{GS}$ = 0
1V
2V
T_j (°C)
0
5
10
15
20
50
100
150

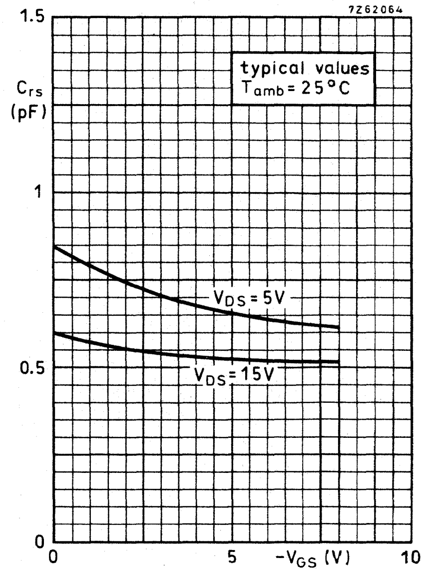

7Z08474
V_{DS} = 15 V
typical values
BFW11
I_D (mA)
$-V_{GS}$ = 0
0.5V
1V
T_j (°C)
0
2
4
6
8
50
100
150

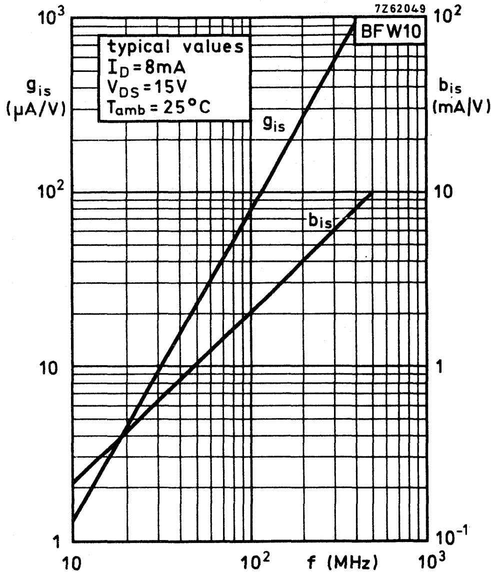

7Z62067
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5nA (V)
V_{DS} = 15 V
T_j = 25°C
BFW10
BFW11
I_{DSS} at V_{GS} = 0 (mA)
0
5
10
15
20

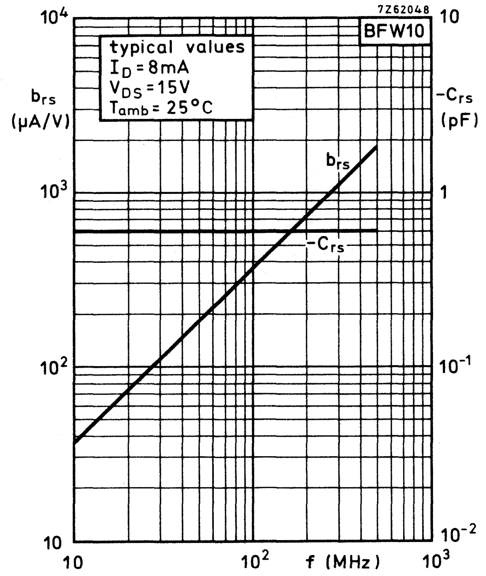

7Z62070
10
|y_fs|
(mA/V)
7.5
5
2.5
0
0
2.5
5
7.5
10
12.5
I_D (mA)
15
typical values
V_DS = 15 V
f = 1 kHz
T_amb = 25°C
BFW11
BFW10

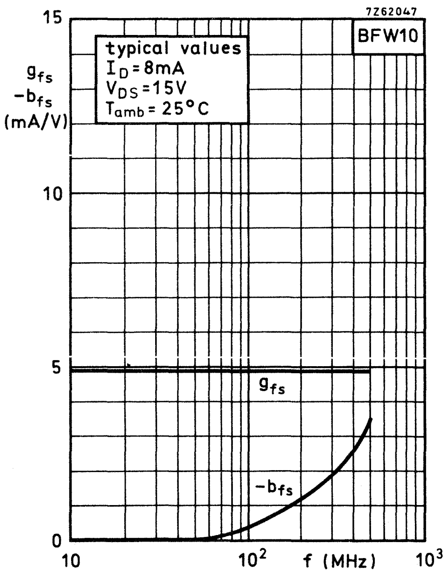

7Z62071
100
|y_os|
(μA/V)
75
50
25
0
0
2.5
5
7.5
10
12.5
I_D (mA)
15
typical values
V_DS = 15 V
f = 1 kHz
T_amb = 25°C
BFW10
BFW11

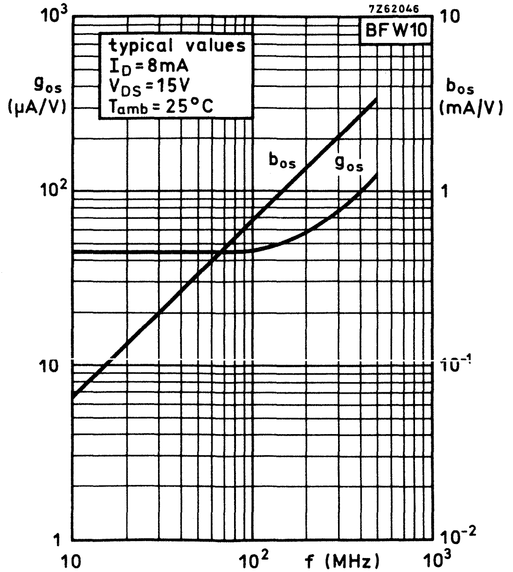

7Z62065
typical values
T_{amb} = 25 °C
C_{is} (pF)
V_{DS} = 5 V
V_{DS} = 15 V
$-V_{GS}$ (V)
0
2
4
6
5
10

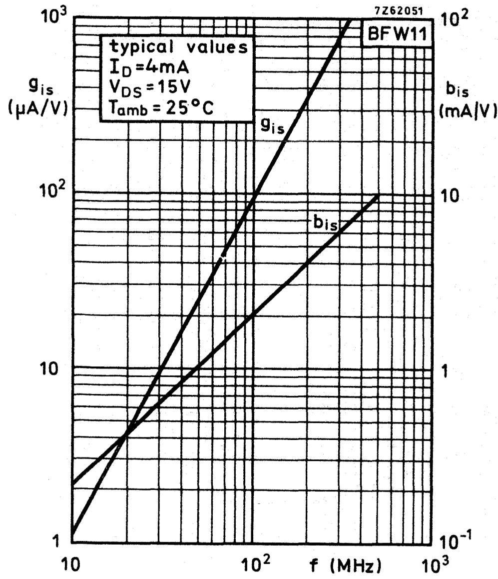

7Z62064
typical values
T_{amb} = 25 °C
C_{rs} (pF)
V_{DS} = 5 V
V_{DS} = 15 V
$-V_{GS}$ (V)
0
0.5
1
1.5
5
10

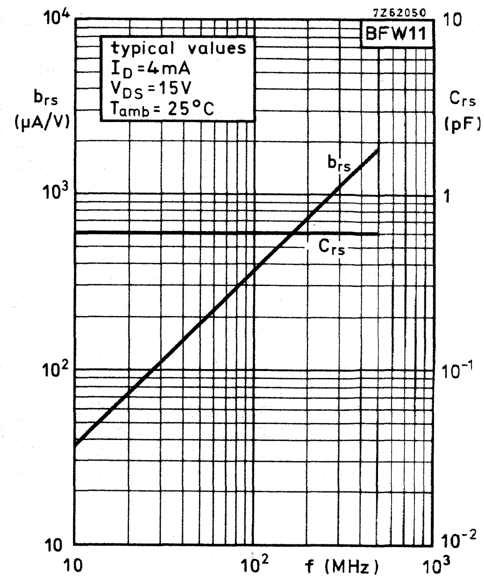

7Z62049
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

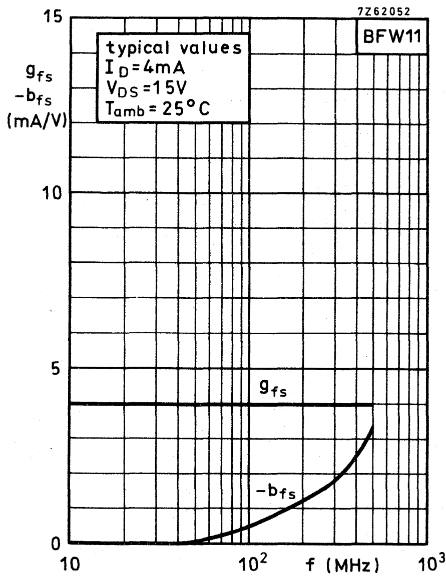

7Z62048
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
$-C_{rs}$ (pF)
b_{rs}
$-C_{rs}$
f (MHz)

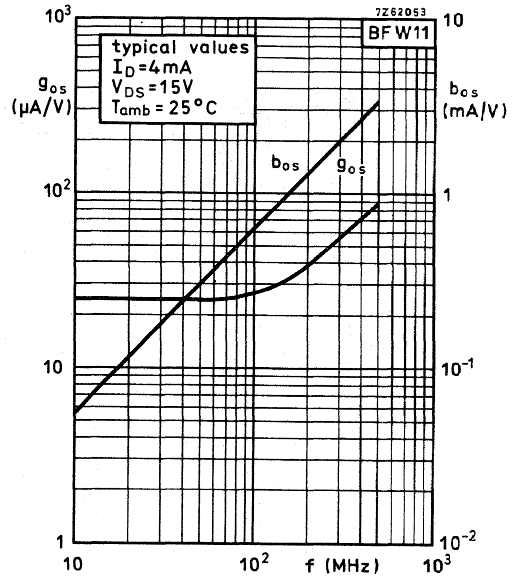

7Z62047
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
(mA/V)
g_{fs}
$-b_{fs}$
f (MHz)

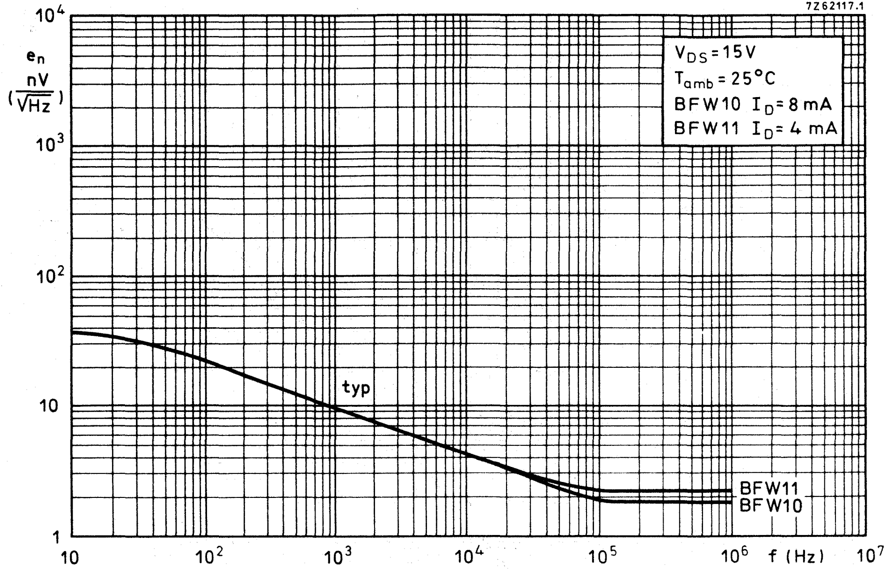

7Z62046
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)

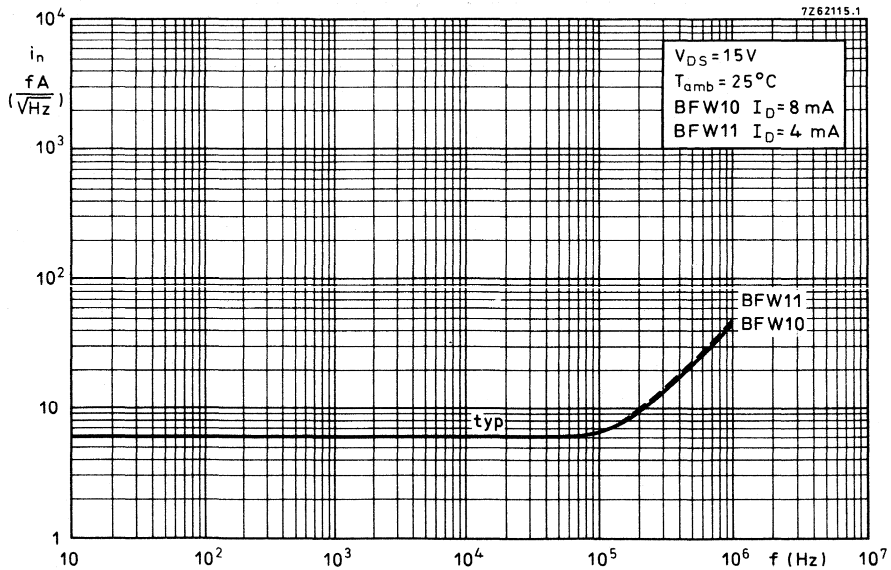

7Z62051
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is}
(μA/V)
b_{is}
(mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

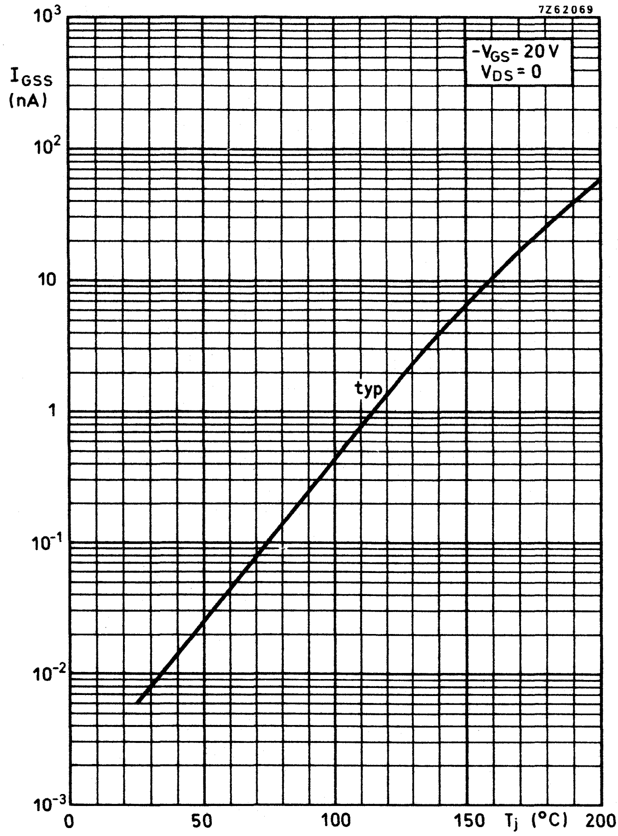

7Z62050
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs}
(μA/V)
C_{rs}
(pF)
b_{rs}
C_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3


7Z62052
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
(mA/V)
g_{fs}
$-b_{fs}$
15
10
5
0
10
10^2
f (MHz)
10^3


7Z62053
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os}
(μA/V)
b_{os}
(mA/V)
b_{os}
g_{os}
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3


7Z62117.1
e_n
nV
(√Hz)
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
f (Hz)


7Z62115.1
i_n
fA
(√Hz)
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
f (Hz)


7Z62069
I_{GSS} (nA)
$-V_{GS}$ = 20 V
V_{DS} = 0
typ
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150	mW

			BFW12	BFW13	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	$>$ $<$	1 5	0,2 1,5	mA mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	$<$	2,5	1,2	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	$<$	0,80	0,80	pF
Transfer admittance (common source) V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\|y_{fs}\|$	$>$	0,5	0,5	mS
Equivalent noise voltage V_{DS} = 15 V; I_D = 200 μA B = 0,6 to 100 Hz	V_n	$<$	0,5	0,5	μV

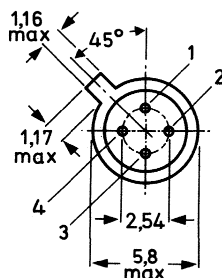
MECHANICAL DATA

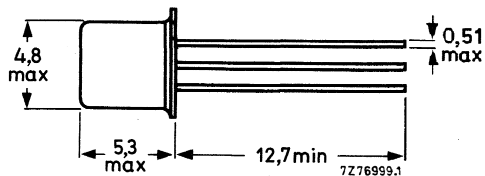
Dimensions in mm

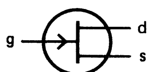
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 85 °C	P_{tot}	max.	150	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

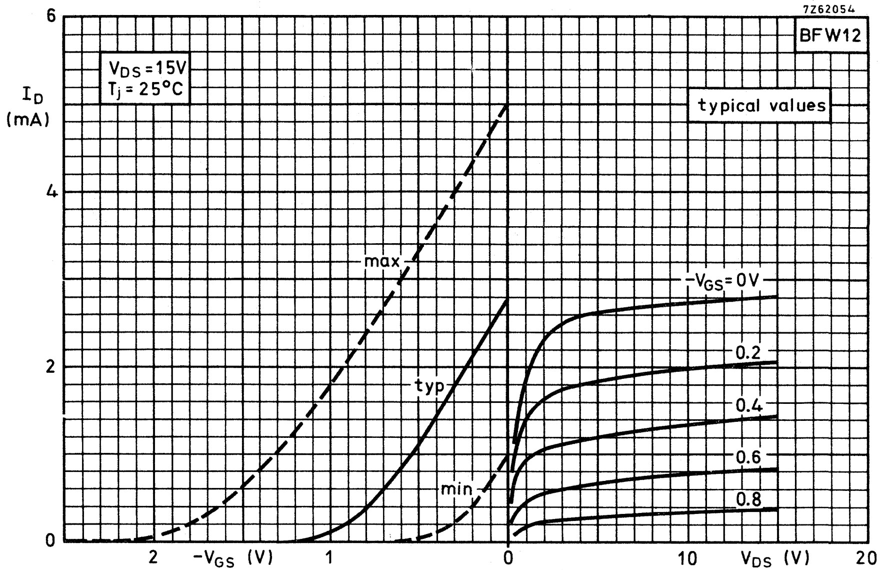
From junction to ambient	$R_{th\ j\text{-}a}$	=	590	K/W

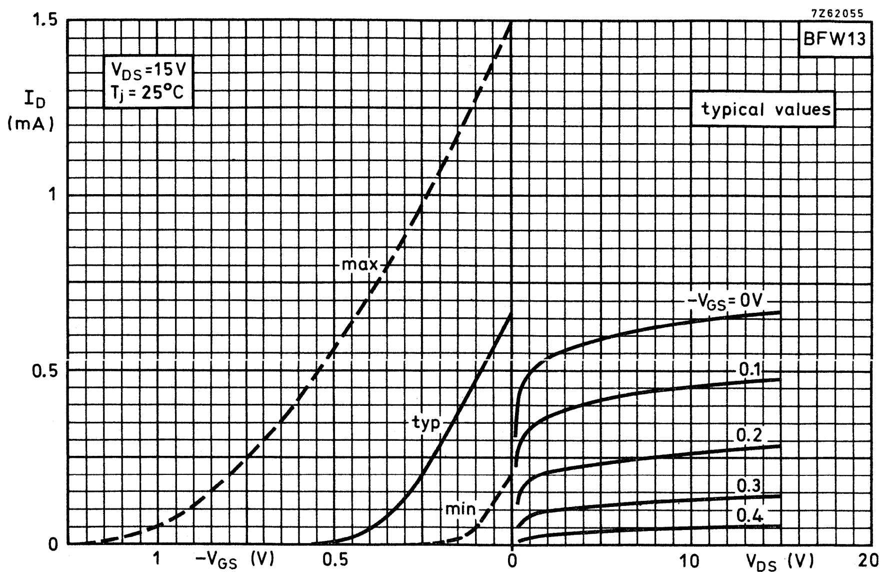
CHARACTERISTICS

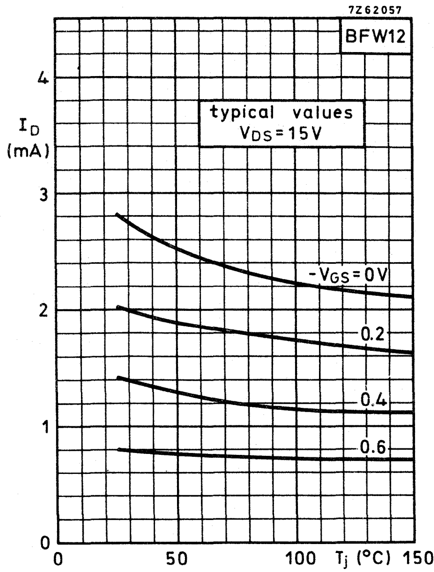
$T_j = 25\ ^oC$ unless otherwise specified

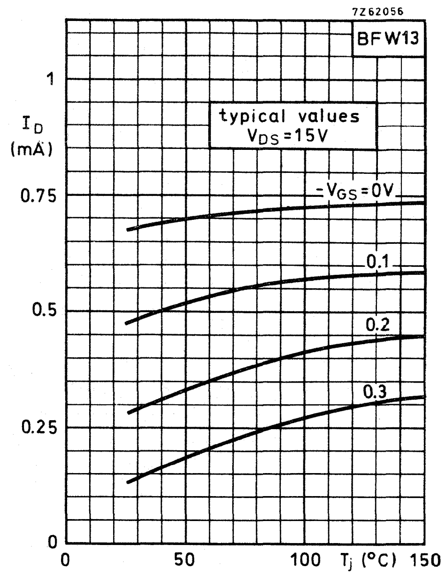
			BFW12	BFW13	
Gate cut-off currents					
$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 150\ ^oC$	$-I_{GSS}$	<	0.1	0.1	μA
Drain current [1]					
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
$I_D = 50$ μA; $V_{DS} = 15$ V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
$I_D = 0.5$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at f = 1 kHz; $T_{amb} = 25\ ^oC$					
$V_{DS} = 15$ V; $V_{GS} = 0$					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mS
Output admittance	$\|y_{os}\|$	<	30	10	μS
$V_{DS} = 15$ V; $I_D = 500$ μA					
Transfer admittance	$\|y_{fs}\|$	>	1.5	–	mS
Output admittance	$\|y_{os}\|$	<	10	–	μS
$V_{DS} = 15$ V; $I_D = 200$ μA					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mS
Output admittance	$\|y_{os}\|$	<	5	5	μS
f = 1 MHz; $T_{amb} = 25\ ^oC$					
$V_{DS} = 15$ V; $V_{GS} = 0$					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	C_{rs}	<	0.80	0.80	pF
Equivalent noise voltage					
$V_{DS} = 15$ V; $I_D = 200$ μA; $T_{amb} = 25\ ^oC$; B = 0.6 to 100 Hz	V_n	<	0.5	0.5	μV

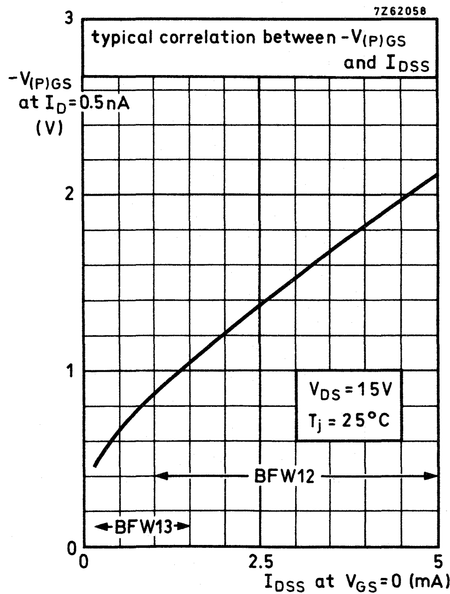
[1]) Measured under pulsed conditions.

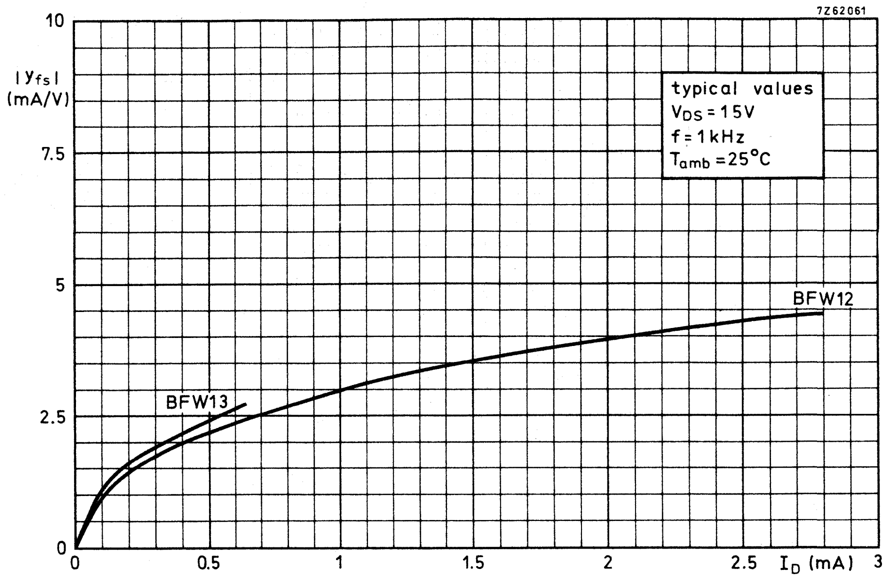

7Z62054
BFW12
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
max
typ
min
$-V_{GS}$ = 0V
0.2
0.4
0.6
0.8
$-V_{GS}$ (V)
V_{DS} (V)
0
2
4
6
1
10
20

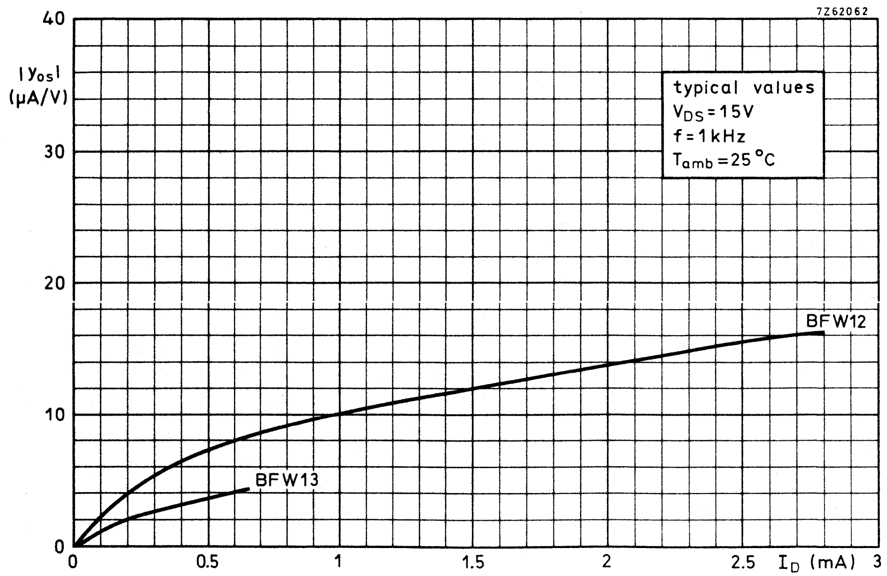

7Z62055
BFW13
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
max
typ
min
$-V_{GS}$ = 0V
0.1
0.2
0.3
0.4
$-V_{GS}$ (V)
V_{DS} (V)
0
0.5
1
1.5
10
20

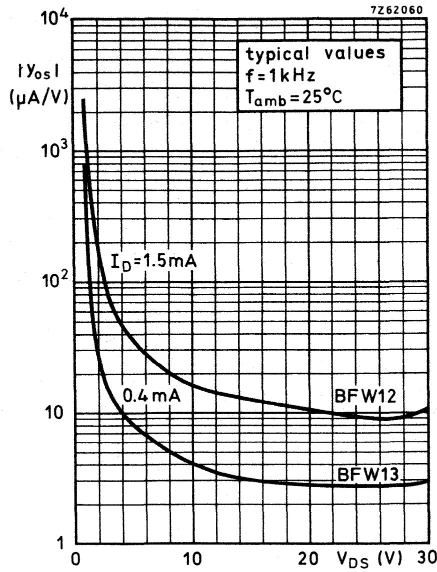

7Z62057
BFW12
typical values
V_{DS} = 15 V
I_D (mA)
$-V_{GS}$ = 0 V
0.2
0.4
0.6
T_j (°C)
0
50
100
150
0
1
2
3
4

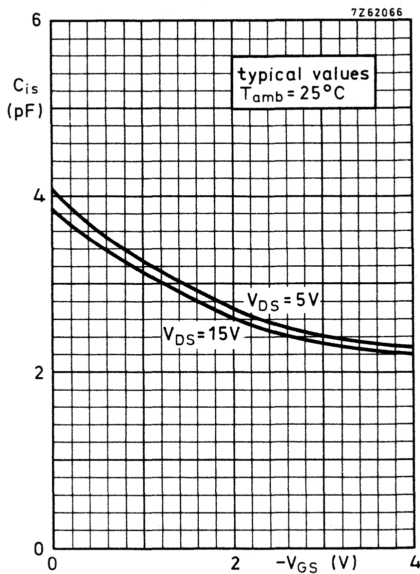

7Z62056
BFW13
typical values
V_{DS} = 15 V
I_D (mA)
$-V_{GS}$ = 0 V
0.1
0.2
0.3
T_j (°C)
0
50
100
150
0
0.25
0.5
0.75
1

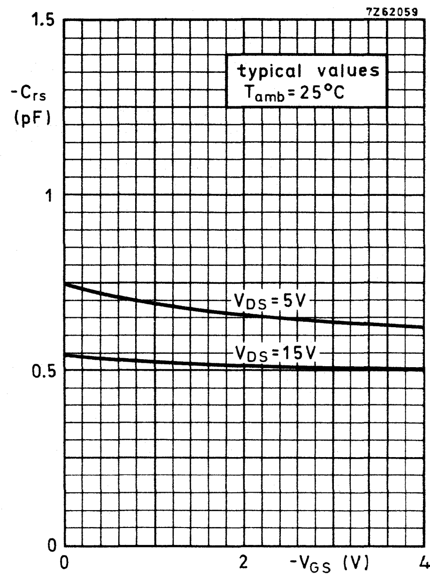

7Z62058
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5 nA (V)
V_{DS} = 15 V
T_j = 25 °C
BFW12
BFW13
I_{DSS} at V_{GS} = 0 (mA)
0
2.5
5
0
1
2
3

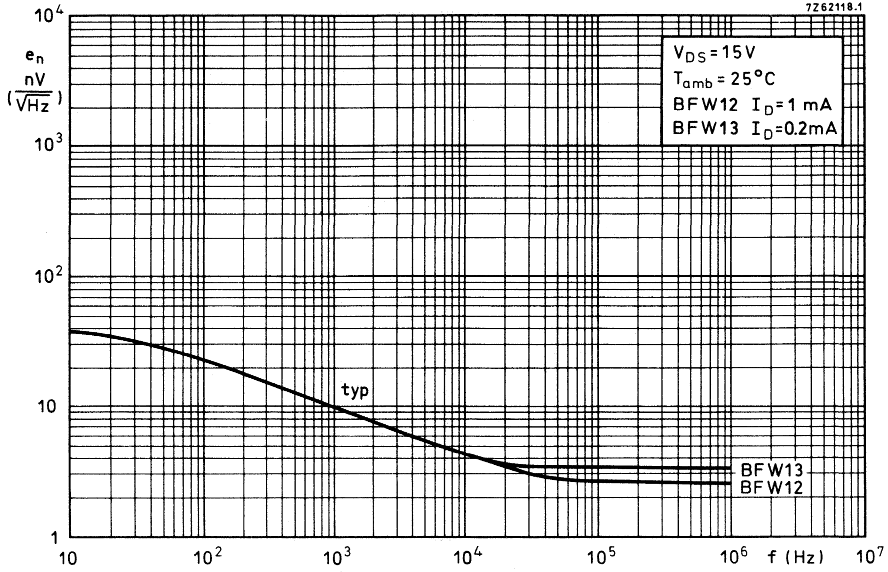

7Z62061
10
|yfs|
(mA/V)
7.5
5
2.5
0
0
0.5
1
1.5
2
2.5
ID (mA)
3
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13

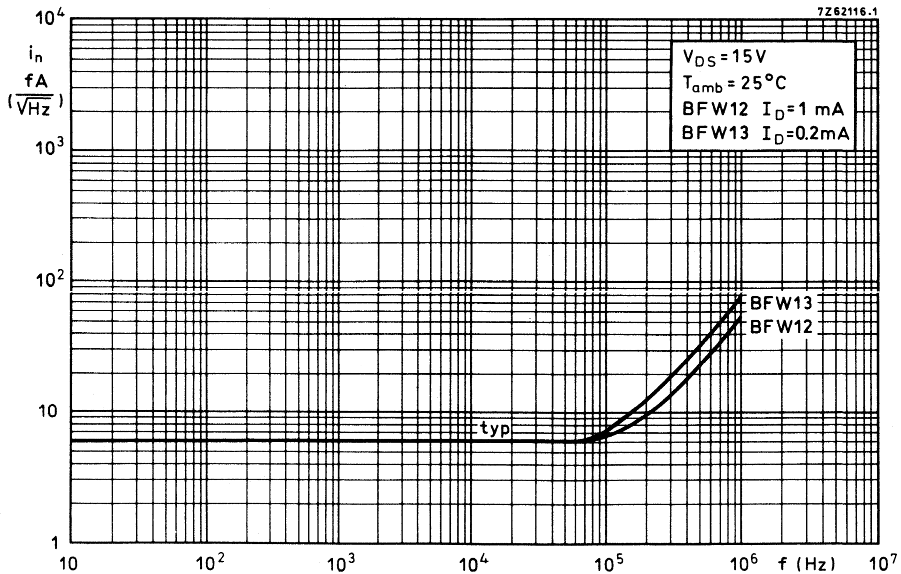

7Z62062
40
|yos|
(μA/V)
30
20
10
0
0
0.5
1
1.5
2
2.5
ID (mA)
3
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13

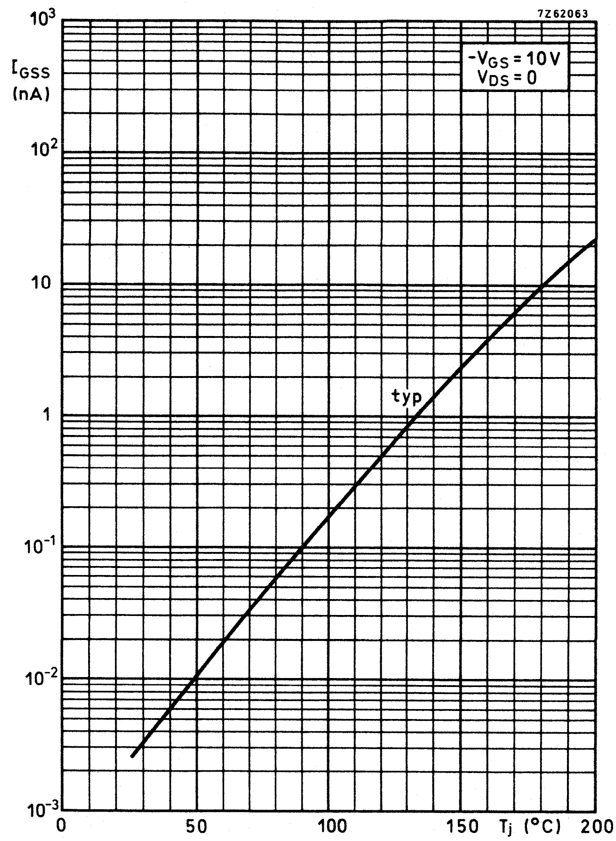

7Z62060
typical values
f = 1 kHz
T_amb = 25°C
|y_os|
(μA/V)
10^4
10^3
10^2
10
1
I_D = 1.5 mA
0.4 mA
BFW12
BFW13
0
10
20
V_DS (V)
30


7Z62066
typical values
T_amb = 25°C
C_is
(pF)
6
4
2
0
V_DS = 5V
V_DS = 15V
0
2
-V_GS (V)
4


7Z62059
typical values
T_amb = 25°C
-C_rs
(pF)
1.5
1
0.5
0
V_DS = 5V
V_DS = 15V
0
2
-V_GS (V)
4


7Z62118.1
e_n
nV
($\sqrt{Hz}$)
10^4
10^3
10^2
10
1
$V_{DS} = 15 V$
$T_{amb} = 25 °C$
BFW12 $I_D = 1$ mA
BFW13 $I_D = 0.2$ mA
typ
BFW13
BFW12
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62116.1
i_n
fA
($\sqrt{Hz}$)
10^4
10^3
10^2
10
1
$V_{DS} = 15 V$
$T_{amb} = 25 °C$
BFW12 $I_D = 1$ mA
BFW13 $I_D = 0.2$ mA
BFW13
BFW12
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62063
10^3
I_{GSS}
(nA)
$-V_{GS} = 10\ V$
$V_{DS} = 0$
10^2
10
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20	mA
Gate-source cut-off voltage I_D = 1.0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	2.0	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 10 MHz	$\|y_{fs}\|$	>	1.6	mS

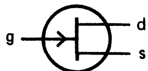
MECHANICAL DATA

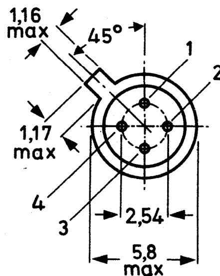
Dimensions in mm

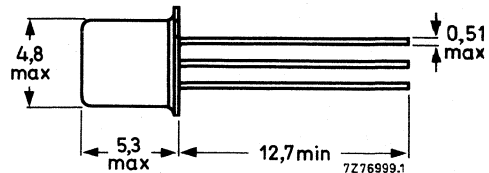
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	20 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}	−65 to + 175 °C	
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590 K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Gate cut-off currents			
$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	$<$	1.0 nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_j = 150\ ^oC$	$-I_{GSS}$	$<$	1.0 μA
Drain current*			
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		2 to 20 mA
Gate-source voltage			
$I_D = 200$ μA; $V_{DS} = 15$ V	$-V_{GS}$		0.5 to 7.5 V
Gate-source cut-off voltage			
$I_D = 1.0$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	$<$	8 V
y-parameters (common source)			
$V_{DS} = 15$ V; $V_{GS} = 0$			
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$		2.0 to 6.5 mS
at f = 10 MHz		$>$	1.6 mS
Output admittance at f = 1 kHz	$\lvert y_{os} \rvert$	$<$	85 μS
Input capacitance at f = 1 MHz	C_{is}	$<$	6 pF
Feedback capacitance at f = 1 MHz	C_{rs}	$<$	2,0 pF

* Measured under pulse conditions.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

BS107

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PIN CONFIGURATION

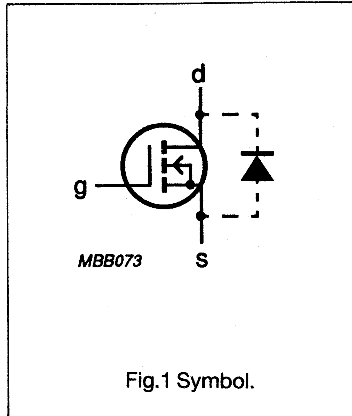


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	drain current	150	mA
$R_{DS(on)}$	drain-source on-resistance	28	Ω
$V_{GS(th)}$	gate threshold voltage	2.4	V

N-channel enhancement mode vertical D-MOS transistor

BS107

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	150	mA
I_{DM}	drain current	peak	-	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	830	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	-	-	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	-	-	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA $V_{DS} = V_{GS}$	0.8	-	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	-	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	-	14	-	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	-	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	4	20	ns

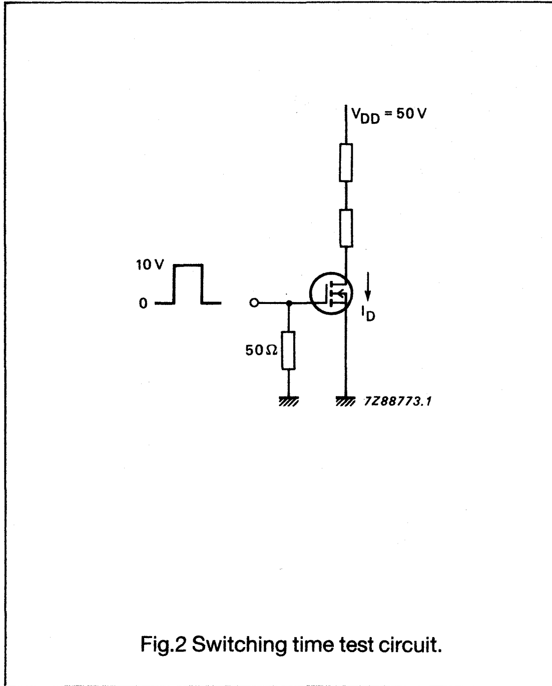


Fig.2 Switching time test circuit.

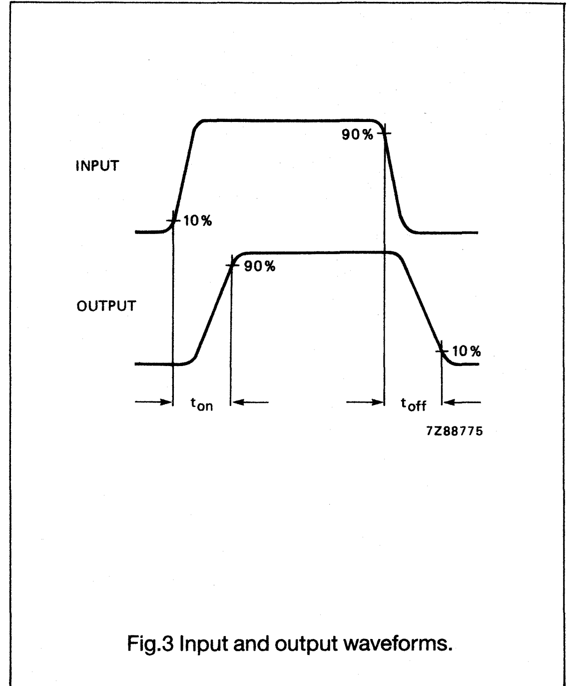


Fig.3 Input and output waveforms.

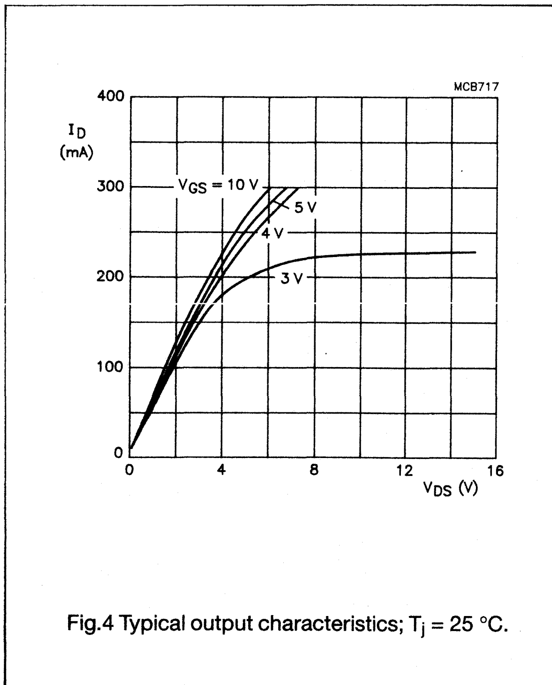


Fig.4 Typical output characteristics; T_j = 25 °C.

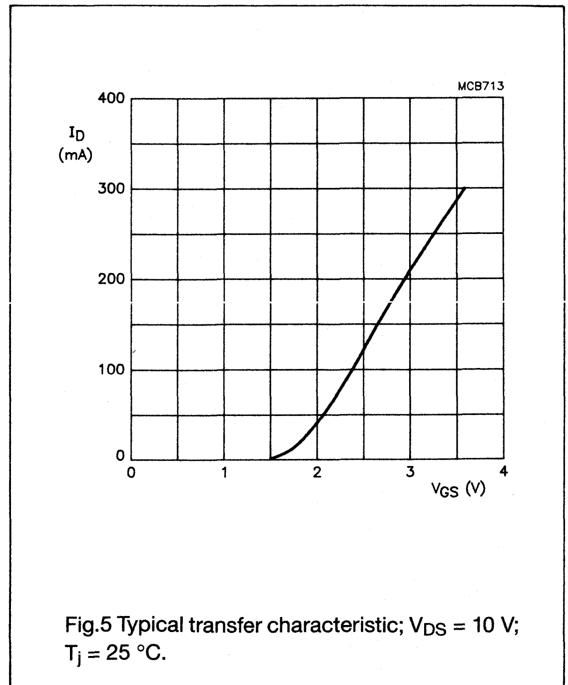


Fig.5 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

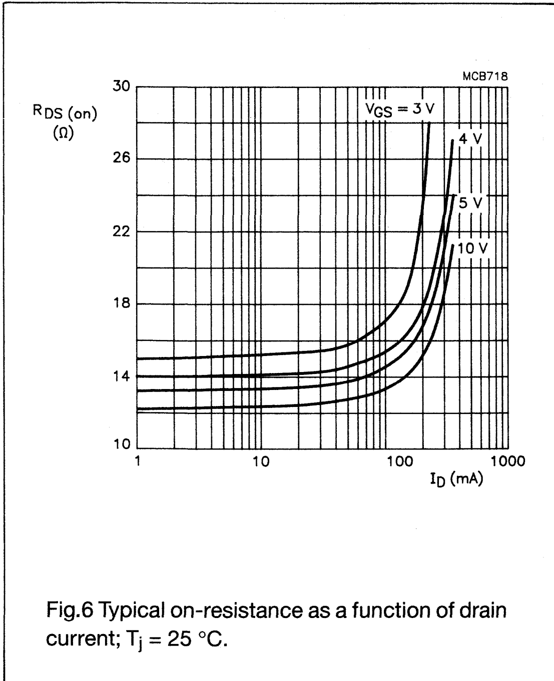


Fig.6 Typical on-resistance as a function of drain current; T_j = 25 °C.

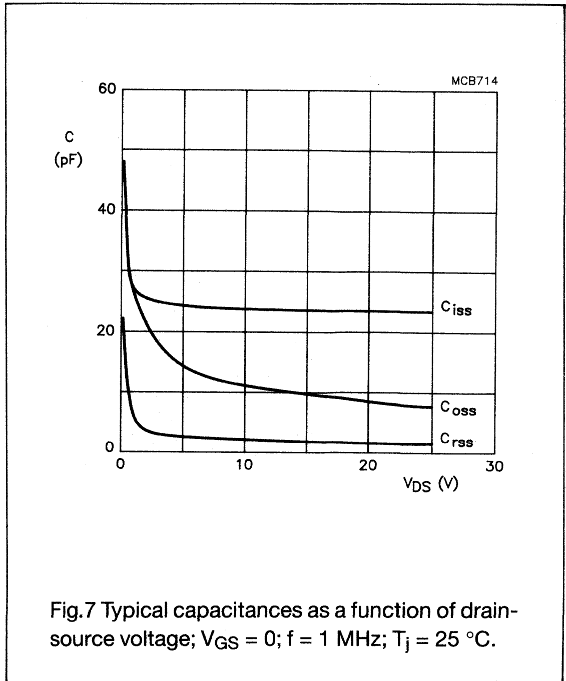


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

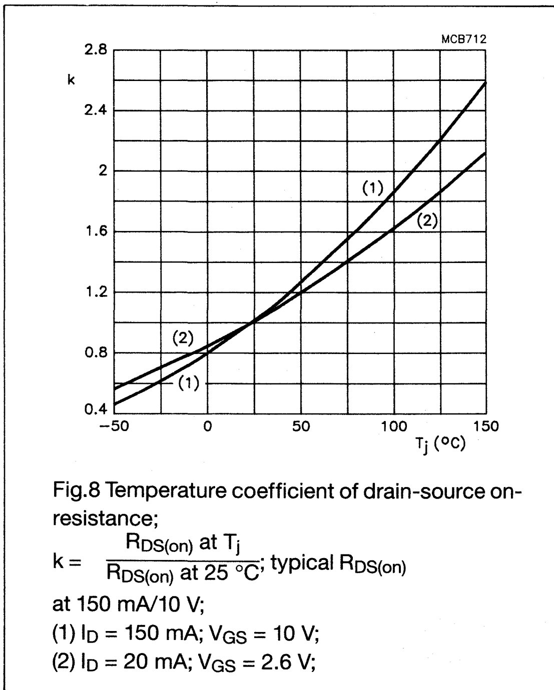


Fig.8 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}; \text{ typical } R_{DS(on)}$$

at 150 mA/10 V;

(1) I_D = 150 mA; V_{GS} = 10 V;

(2) I_D = 20 mA; V_{GS} = 2.6 V;

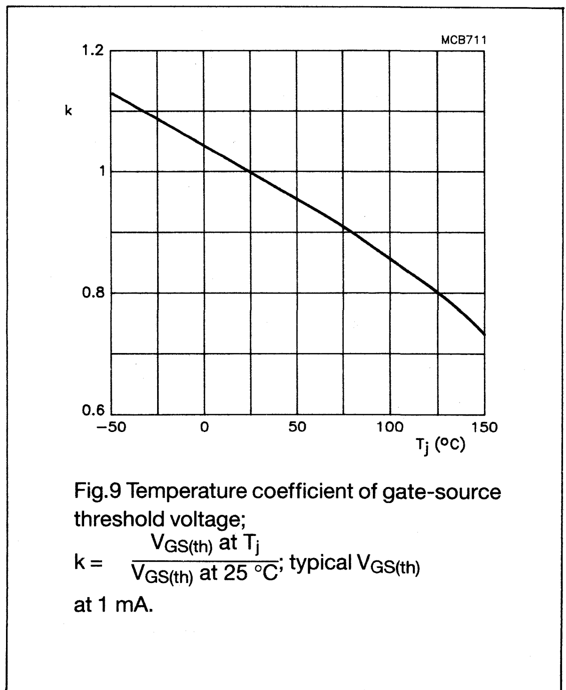


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}; \text{ typical } V_{GS(th)}$$

at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BS107

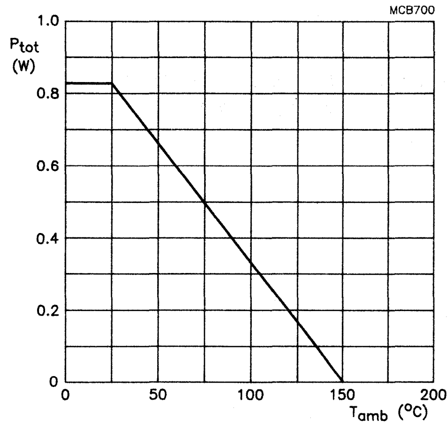


Fig.10 Power derating curve.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5 Ω
		max.	6.4 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min.	200 mS
		typ.	350 mS

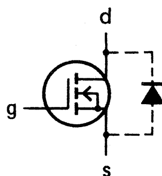
MECHANICAL DATA

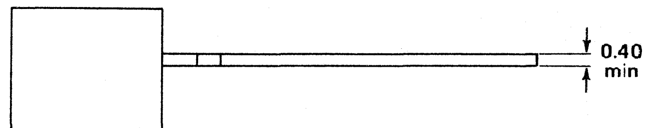
Dimensions in mm

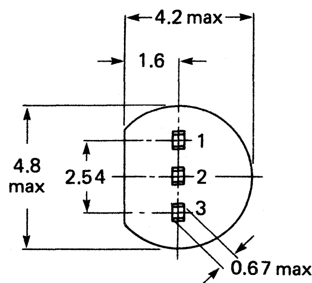
Fig.1 TO-92

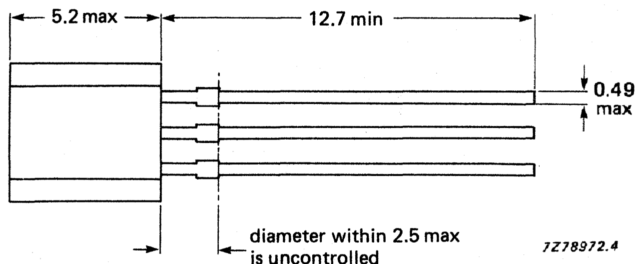
Pinning

1 = source
2 = gate
3 = drain









Note: Various pinnings are available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	500 mA
Total power dissipation up to $T_{case} = 25\ ^oC$	P_{tot}	max.	0.6 W
Storage temperature	T_{stg}		−55 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

Parameter	Symbol		Value
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Parameter	Symbol		Value
Drain-source breakdown voltage $I_D = 10\ \mu A$; $V_{GS} = 0$	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current $V_{DS} = 130$ V; $V_{GS} = 0$	I_{DSS}	max.	30 nA
Gate-source leakage current $V_{GS} = 15$ V; $V_{DS} = 0$	I_{GSS}	max.	10 nA
Gate threshold voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	min.	1.0 V
		max.	3.0 V
Drain-source ON-resistance $I_D = 250$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	4.5 Ω
		max.	6.4 Ω
$I_D = 100$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	4.2 Ω
		max.	6.0 Ω
Transfer admittance $I_D = 250$ mA; $V_{DS} = 25$ V	$\lvert y_{fs} \rvert$	min.	200 mS
		typ.	350 mS
Input capacitance at f = 1 MHz $V_{DS} = 25$ V; $V_{GS} = 0$	C_{iss}	typ.	45 pF
Output capacitance at f = 1 MHz $V_{DS} = 25$ V; $V_{GS} = 0$	C_{oss}	typ.	15 pF
Feedback capacitance at f = 1 MHz $V_{DS} = 25$ V; $V_{GS} = 0$	C_{rss}	typ.	3.5 pF
Switching times (see Figs 2 and 3) $I_D = 250$ mA; $V_{DD} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ.	5 ns
	t_{off}	typ.	15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

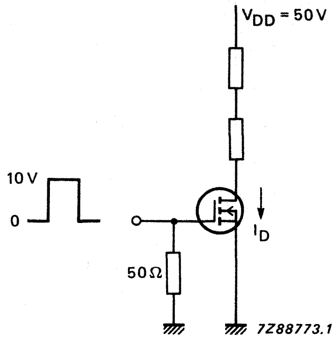


Fig.2 Switching times test circuit.

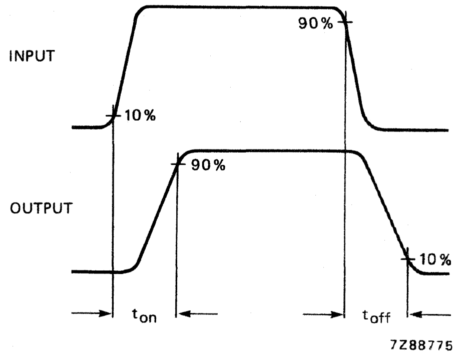


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BS108

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

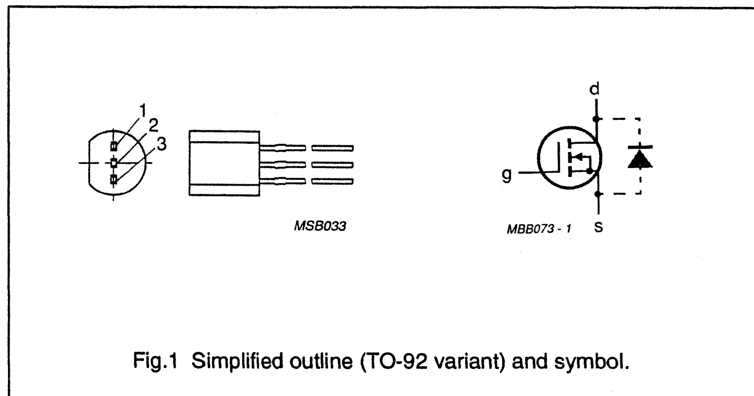


Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 x 10 mm

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

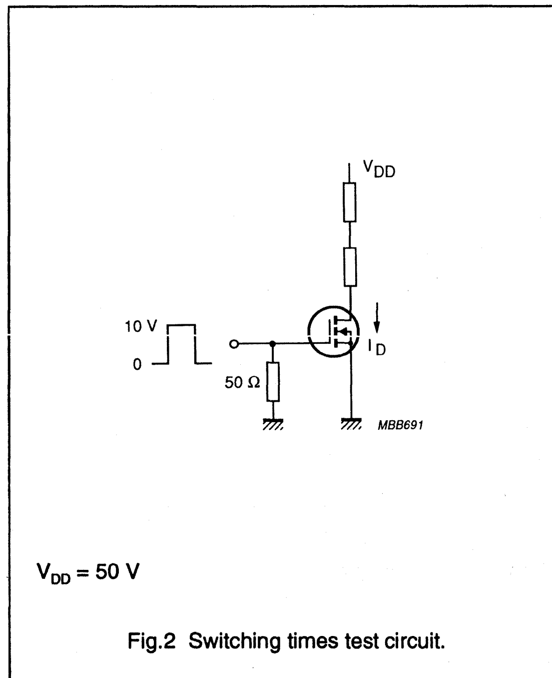


Fig.2 Switching times test circuit.

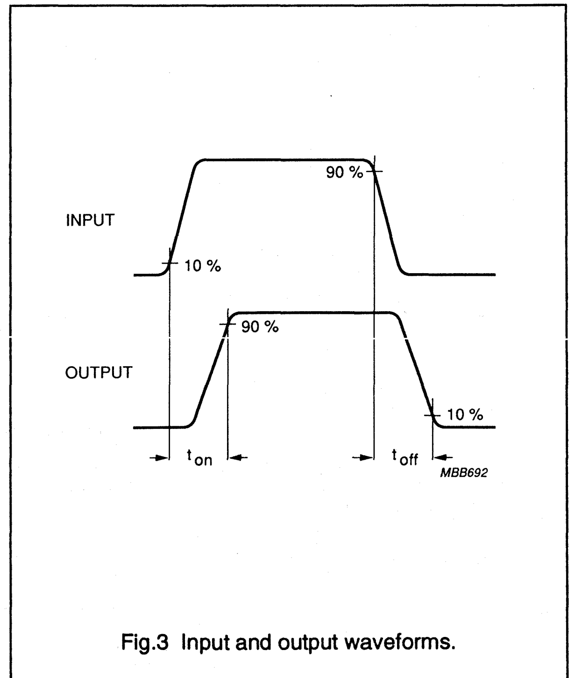


Fig.3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830	mW
Junction temperature	T_j	max.	150	°C
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	max.	5	Ω

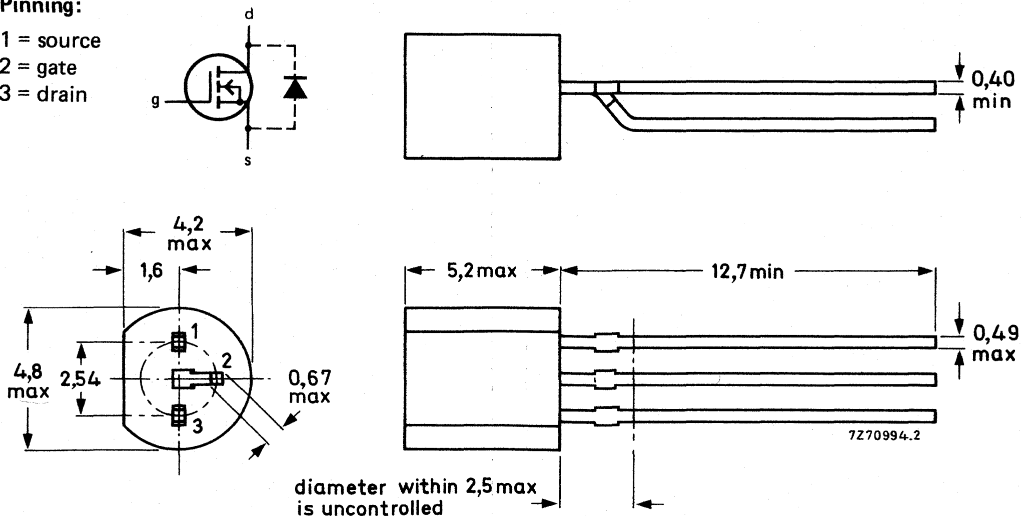
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pin configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Drain-gate voltage	V_{DG}	max.	60 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (DC) at T_c = 25 °C	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Storage temperature range	T_{stg}		−55 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage V_{GS} = 0; I_D = 100 μA	$V_{(BR)DS}$	min.	60 V
		typ.	90 V
Gate threshold voltage V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	min.	0.8 V
		max.	3.0 V
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	max.	10 nA
Drain cut-off current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	0.5 μA
Drain-source ON-resistance (note 1) V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	typ.	2.5 Ω
		max.	5.0 Ω
Forward transconductance (note 1) V_{DS} = 10 V; I_D = 200 mA; f = 1 kHz	g_{fs}	typ.	200 mS
Capacitances at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	25 pF
		max.	40 pF
	C_{os}	typ.	22 pF
		max.	30 pF
	C_{rs}	typ.	6 pF
		max.	10 pF
Switching times at I_D = 200 mA I_D = 200 mA; V_{DS} = 50 V;	t_{on}	typ.	4 ns
		max.	10 ns
V_{GS} = 0 to 10 V	t_{off}	typ.	4 ns
		max.	10 ns

Note

1. t_p = 80 μs; δ = 0,01.

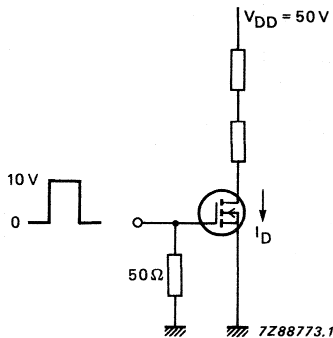


Fig. 2 Switching times test circuit.

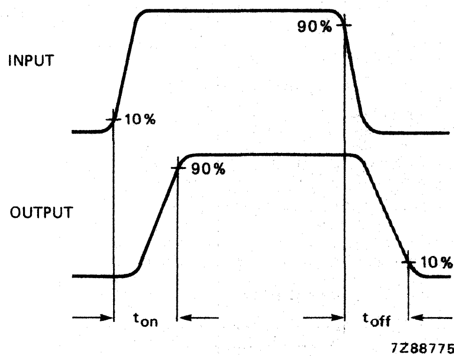


Fig. 3 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

BS208

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in a TO-92 envelope and intended for use in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

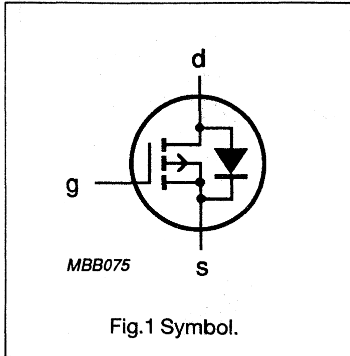


Fig.1 Symbol.

PINNING - TO-92

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	-	20	V
$-I_D$	drain current	DC	-	-	0.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	-	0.83	W
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	-	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
$-I_D$	drain current	DC	-	0.2	A
$-I_{DM}$	drain current	peak value	-	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	0.83	W
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
R_{thj-a}	from junction to ambient	150	K/W

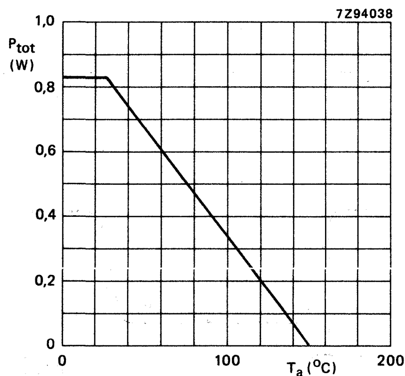


Fig.2 Power derating curve.

P-channel enhancement mode vertical D-MOS transistor

BS208

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 μA	200	-	-	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 130 V V_{GS} = 0	-	-	1	μA
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 70 V $-V_{GS}$ = 0.2 V	-	-	25	μA
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	V_{GS} = V_{DS} $-I_D$ = 1 mA	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	-	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	-	mS
C_{iss}	input capacitances	note 1	-	55	90	pF
C_{oss}	output capacitance	note 1	-	20	30	pF
C_{rss}	feedback capacitance	note 1	-	5	15	pF
t_{on}	turn-on time	note 2	-	5	10	ns
t_{off}	turn-off time	note 2	-	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

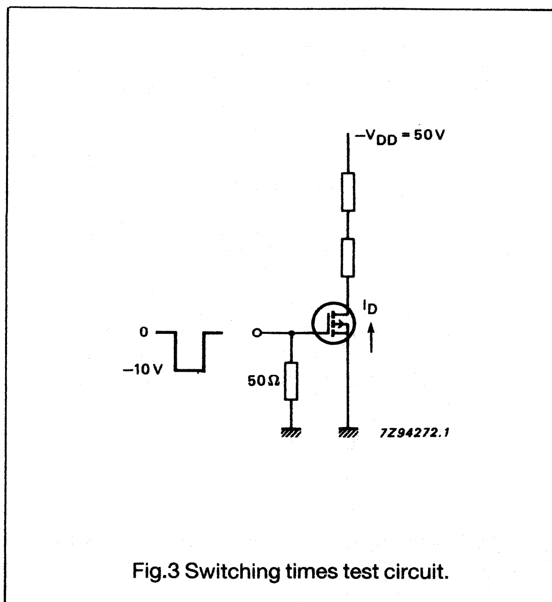


Fig.3 Switching times test circuit.

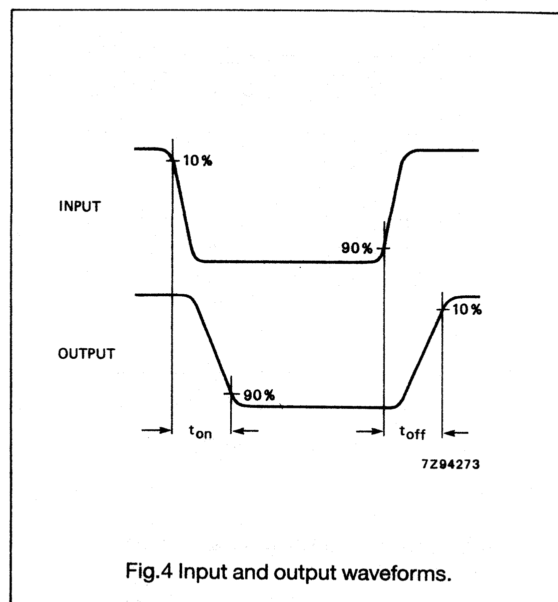


Fig.4 Input and output waveforms.

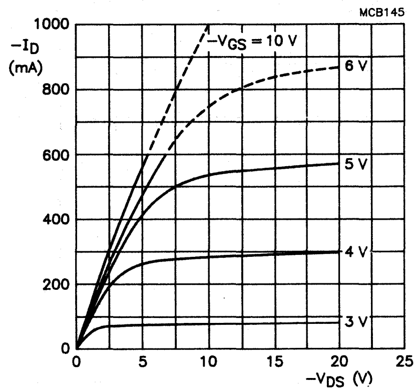


Fig.5 Typical output characteristics; T_j = 25 °C.

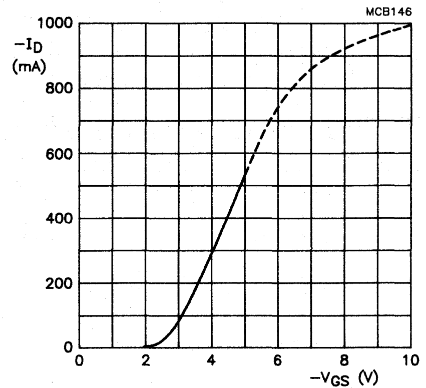


Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

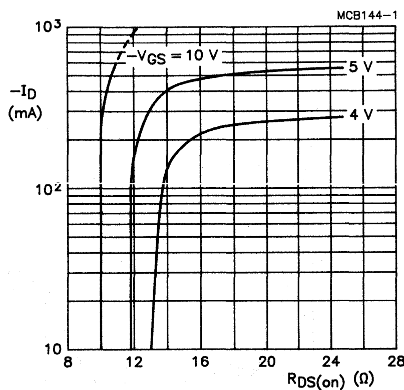


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

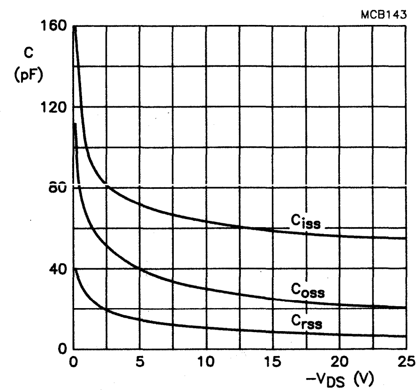


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BS208

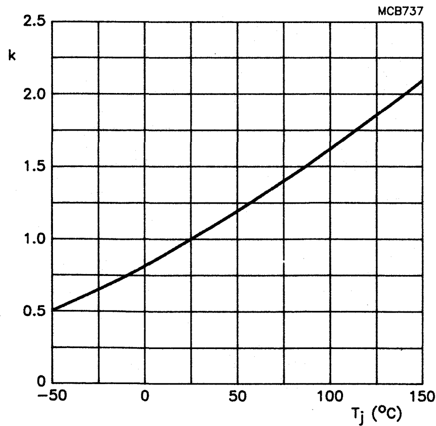


Fig.9 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at 200 mA/10 V;

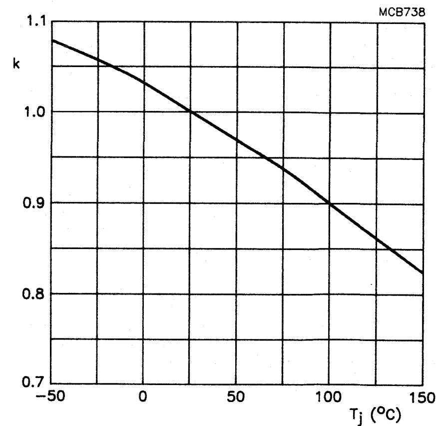


Fig.10 Temperature coefficient of gate-source threshold voltage;

$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ.	9	Ω
		max.	14	Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|y_{fs}\|$	typ.	125	mS

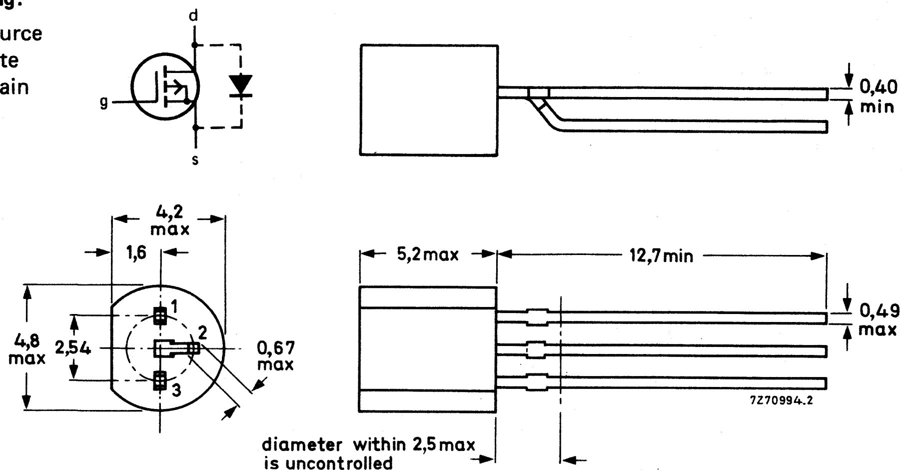
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak value)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	45 V
Drain-source leakage current $-V_{DS}$ = 25 V; V_{GS} = 0	$-I_{DSS}$	max.	0.5 μA
Gate-source leakage current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	20 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.0 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

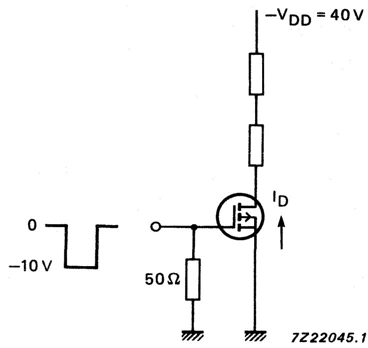


Fig. 2 Switching times test circuit.

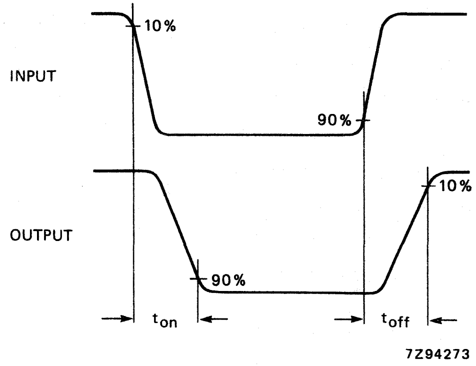


Fig. 3 Input and output waveforms.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type.

The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feedback capacitance $V_{GS} = V_{BS}$ = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

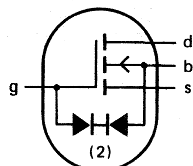
MECHANICAL DATA

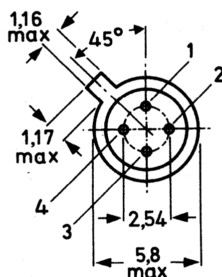
Dimensions in mm

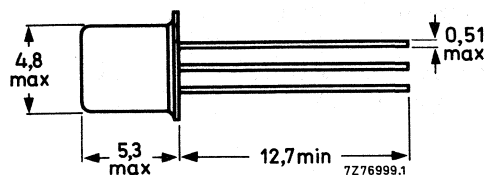
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = substrate (b)
connected to case







Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	+ 15 −15	V V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C in free air	P_{tot}	max.	275	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GBS}	max.	10	nA
Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_S = 20 mA	g_{fs}	min. typ.	10 15	mS mS

Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I_D = 10 μA	$-V_{(P)GS}$	max.	2.0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0 V_{GS} = 5 V	r_{DSon}	typ. max.	25 Ω 50 Ω
V_{GS} = 10 V	r_{DSon}	typ. max.	15 Ω 30 Ω
Capacitances at f = 1 MHz (see Fig. 2) $V_{GS} = V_{BS}$ = −5 V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0.6 pF
Input capacitance	C_{iss}	typ.	2.3 pF
Output capacitance	C_{oss}	typ.	1.9 pF
Switching times (see Fig. 3) V_{DD} = 10 V; V_i = −5 to + 5 V	t_{on}	typ.	1.0 ns
	t_{off}	typ.	5.0 ns

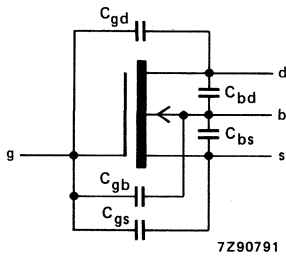
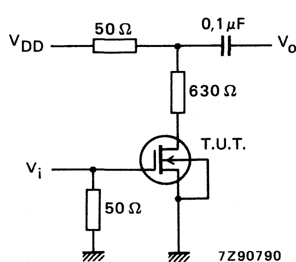


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$

$C_{oss} = C_{gd} + C_{bd}$

$C_{rss} = C_{gd}$



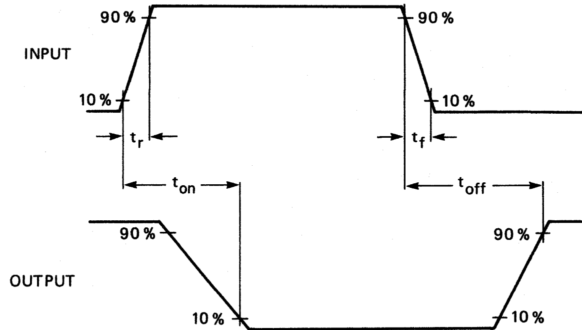


Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; t_r < 0.5 ns; t_f < 1.0 ns; t_p = 20 ns; δ < 0.01.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type. The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feed-back capacitance V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

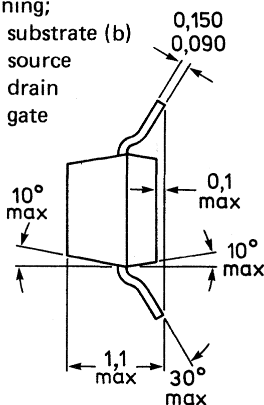
MECHANICAL DATA

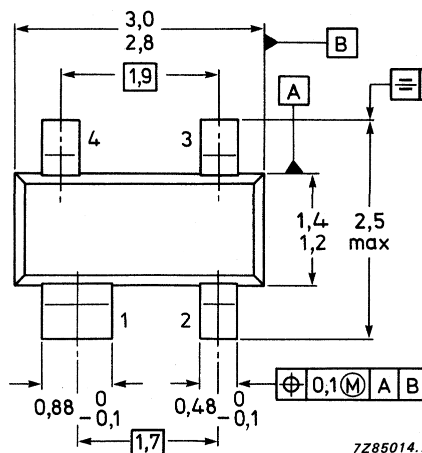
Dimensions in mm

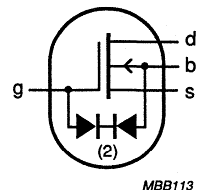
Fig. 1 SOT-143.

Marking code: M32

Pinning;
1 = substrate (b)
2 = source
3 = drain
4 = gate







TOP VIEW

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	± 25	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current $V_{GD} = V_{BD}$ = 5 V; V_{SD} = 10V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current $V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	max.	10	nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

Parameter	Symbol		Value
Forward transconductance at f = 1 kHz			
V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	min.	10 mS
		typ.	15 mS
Gate-source cut-off voltage			
V_{DS} = 10 V; V_{SB} = 0; I I_D = 10 μA	$-V_{(P)GS}$	max.	2.0 V
Drain-source ON-resistance			
I_D = 1 mA; V_{SB} = 0; V_{GS} = 5 V	R_{DSon}	typ.	25 Ω
		max.	50 Ω
V_{GS} = 10 V	R_{DSon}	typ.	15 Ω
		max.	30 Ω
Capacitances at f = 1 MHz			
V_{GS} = V_{BS} = −5V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0.6 pF
Input capacitance	C_{iss}	typ.	1.5 pF
Output capacitance	C_{oss}	typ.	1.0 pF
Switching times (see Fig. 3)			
V_{DD} = 10 V; V_i = −5 V to +5 V	t_{on}	typ.	1.0 ns
	t_{off}	typ.	5.0 ns

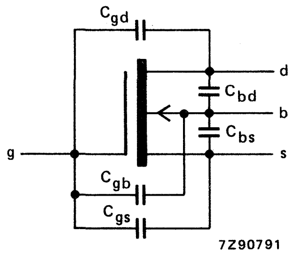
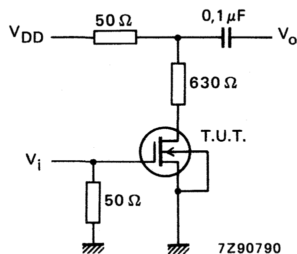


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$

$C_{oss} = C_{gd} + C_{bd}$

$C_{rss} = C_{gd}$



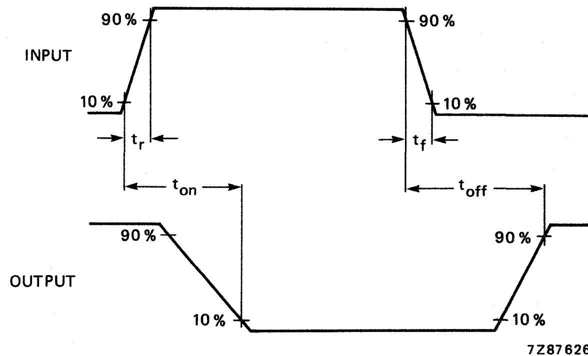


Fig. 3 Switching times and input and output waveforms; R_i = 50 Ω; t_r < 0.5 ns; t_f < 1.0 ns; t_p = 20 ns; δ < 0.01.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analogue and/or digital switch
- switch driver
- converters
- choppers

QUICK REFERENCE DATA

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275				mW
Drain-source resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 15 V	$R_{DS(on)}$	typ.	25				Ω
Feedback capacitance $V_{GS} = V_{BS}$ = −15 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0,6				pF
Junction temperature	T_j	max.	125				°C

MECHANICAL DATA

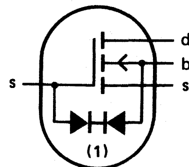
See next page.

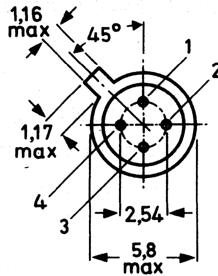
MECHANICAL DATA

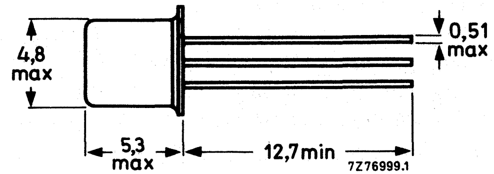
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = source
2 = drain
3 = gate
4 = substrate (b)
connected to case







(1) Diode protection on types BSD213 and BSD215 only.
BSD212 and BSD214 have no protection diode.
To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Source-drain voltage	V_{SD}	max.	10	10	20	20	V
Drain-substrate voltage	V_{DB}	max.	15	15	25	25	V
Source-substrate voltage	V_{SB}	max.	15	15	25	25	V
Gate-substrate voltage	V_{GB}	max.	± 40	± 15	± 40	± 15	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Gate-drain voltage	V_{GD}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275				mW
Storage temperature range	T_{stg}		−65 to + 175				°C
Junction temperature	T_j	max.	125				°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 360 K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage							
$V_{GS} = V_{BS} = -5$ V; $I_S = 10$ nA	$V_{(BR)DSX}$	>	10	10	20	20	V
Source-drain breakdown voltage							
$V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$	>	10	10	20	20	V
Drain-substrate breakdown voltage							
$V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	>	15	15	25	25	V
Source-substrate breakdown voltage							
$V_{GB} = 0$; $I_S = 10$ nA; open drain	$V_{(BR)SBO}$	>	15	15	25	25	V
Drain-source leakage current							
$V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V	I_{DSoff}	typ.	1,0	1,0	—	—	nA
$V_{GS} = V_{BS} = -5$ V; $V_{DS} = 20$ V	I_{DSoff}	typ.	—	—	1,0	1,0	nA
Source-drain leakage current							
$V_{GD} = V_{BD} = -5$ V; $V_{SD} = 10$ V	I_{SDoff}	typ.	1,0	1,0	—	—	nA
$V_{GD} = V_{BD} = -5$ V; $V_{SD} = 20$ V	I_{SDoff}	typ.	—	—	1,0	1,0	nA
Gate-substrate leakage current							
$V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 40$ V	I_{GBS}	<	0,1	—	0,1	—	nA
$V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GBS}	<	—	10	—	10	nA
Threshold voltage							
$V_{DS} = V_{GS} = V_{GS(th)}$; $V_{SB} = 0$; $I_S = 1\ \mu A$	$V_{GS(th)}$		0,1 to 2,0				V

			BSD212	BSD213	BSD214	BSD215	
Drain-source resistance							
$I_D = 1,0$ mA; $V_{SB} = 0$;							
$V_{GS} = 5$ V	$R_{DS(on)}$	typ.	50	50	50	50	Ω
		<	70	70	70	70	Ω
$V_{GS} = 10$ V	$R_{DS(on)}$	typ.	30	30	30	30	Ω
		<	45	45	45	45	Ω
$V_{GS} = 15$ V	$R_{DS(on)}$	typ.	25	25	25	25	Ω
$V_{GS} = 25$ V	$R_{DS(on)}$	typ.	15		15		Ω

DYNAMIC CHARACTERISTICS

Forward transconductance at f = 1 kHz				
$V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	typ.	15	mS
		>	10	mS
Capacitance at f = 1 MHz (see Fig. 2)				
$V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V				
Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	2,3	pF
Output capacitance	C_{oss}	typ.	1,9	pF

DYNAMIC CHARACTERISTICS (continued)

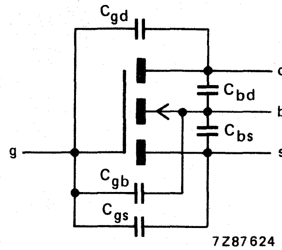


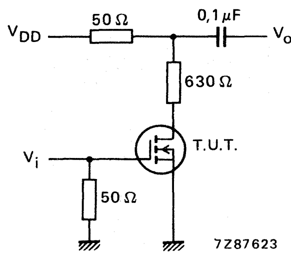
Fig. 2 Capacitances model.

$C_{iss} = C_{GS} + C_{GD} + C_{GB}$

$C_{oss} = C_{GD} + C_{BD}$

$C_{rss} = C_{GD}$

Switching times (see Fig. 3)				
V_{DD} = 10 V; V_i = –5 V to +5 V	t_{on}	typ.	1,0	ns
	t_{off}	typ.	5,0	ns



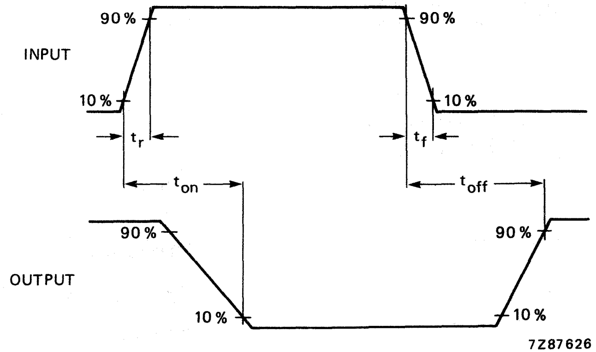


Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

R_i = 50 Ω

t_r < 0,5 ns

t_f < 1,0 ns

t_p = 20 ns

δ < 0,01

N-channel depletion mode vertical D-MOS transistors

BSD254; BSD254A; BSD254AR

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
BSD254	
1	gate
2	drain
3	source
BSD254A	
1	source
2	gate
3	drain
BSD254AR	
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	200	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	0.85	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	−1.65	−0.75	V

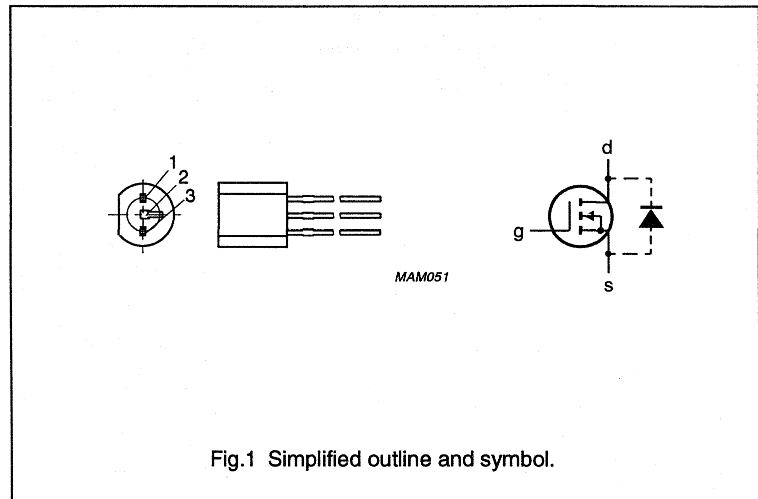


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	200	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	0.85	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	145 K/W

Note

1. Device mounted on an epoxy printed circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = −3 V	250	–	V
I_{DSX}	drain-source cut-off leakage current	V_{DS} = 200 V; V_{GS} = −3 V	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	100	nA
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	−1.65	−0.75	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = 3 V	−1.4	−0.6	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
		I_D = 250 mA; V_{GS} = 5 V	–	12	Ω
I_{DSS}	drain saturation current	V_{DS} = 25 V; V_{GS} = 0	70	–	mA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	15	pF
Switching times (see Figs 2 and 3)					
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = −3 to +5 V	–	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = +5 to −3 V	–	30	ns

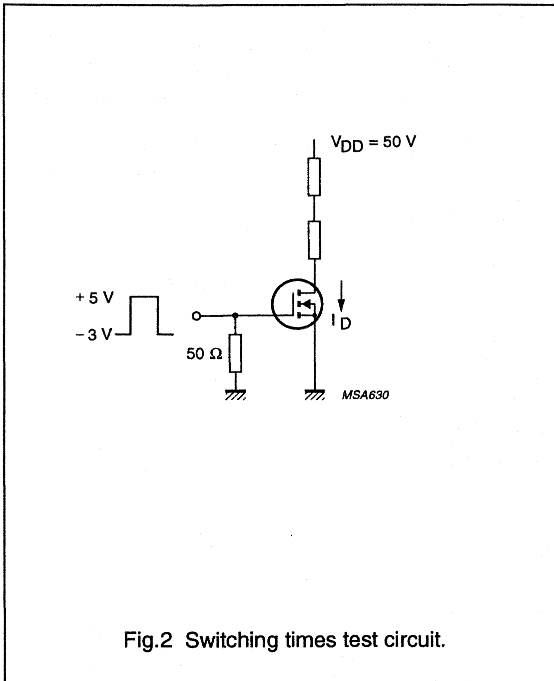


Fig.2 Switching times test circuit.

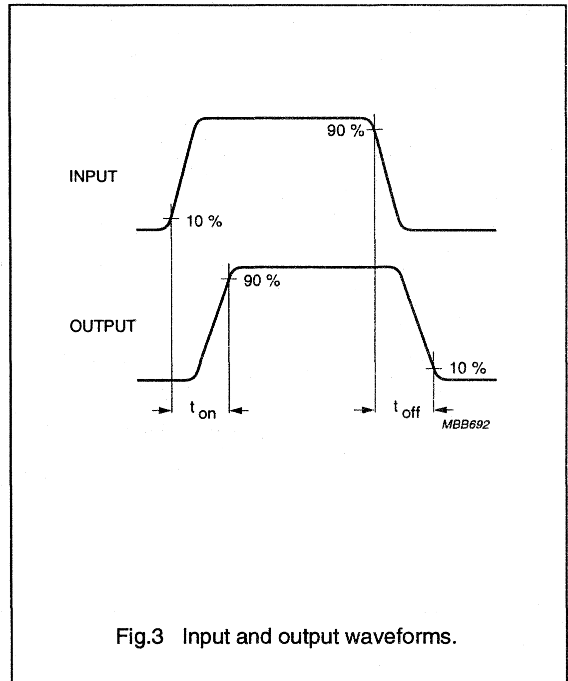


Fig.3 Input and output waveforms.

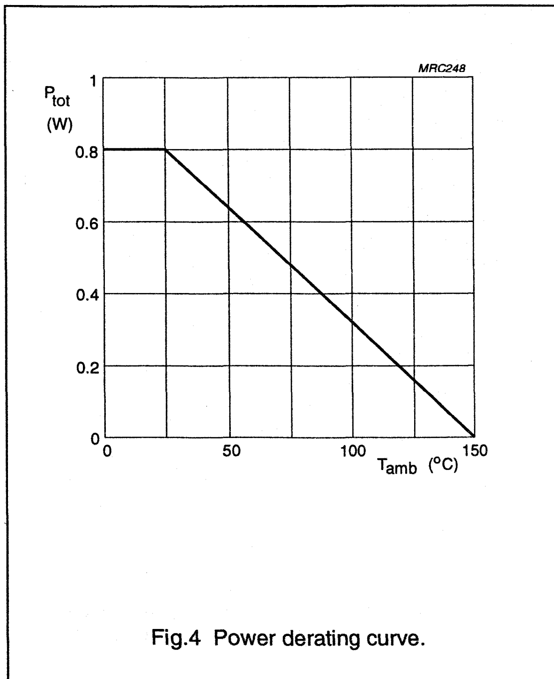
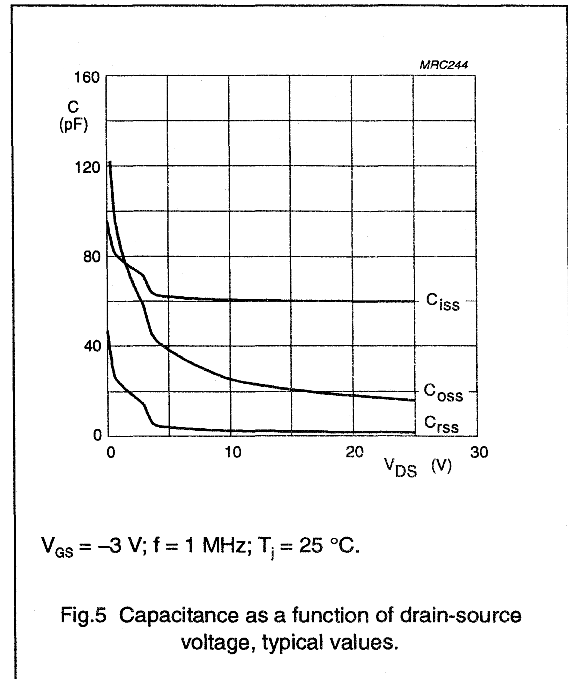
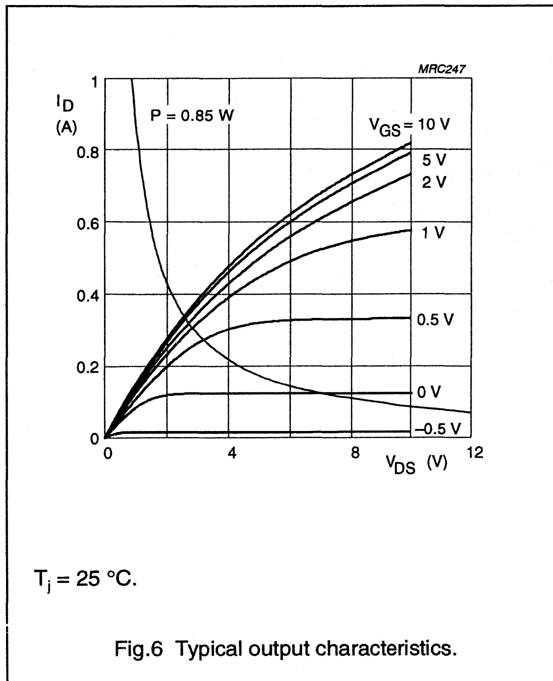


Fig.4 Power derating curve.



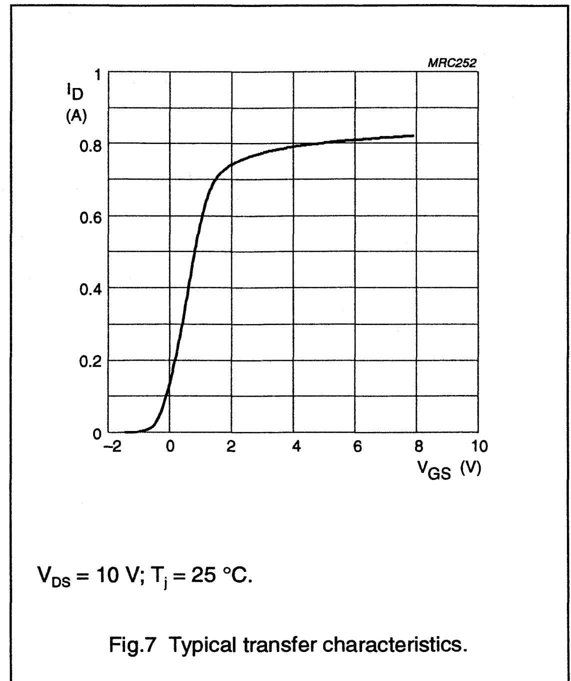
V_{GS} = −3 V; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



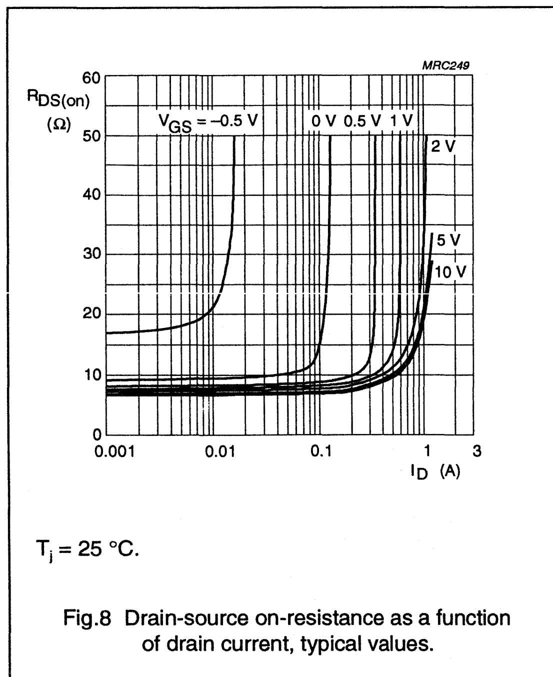
T_j = 25 °C.

Fig.6 Typical output characteristics.



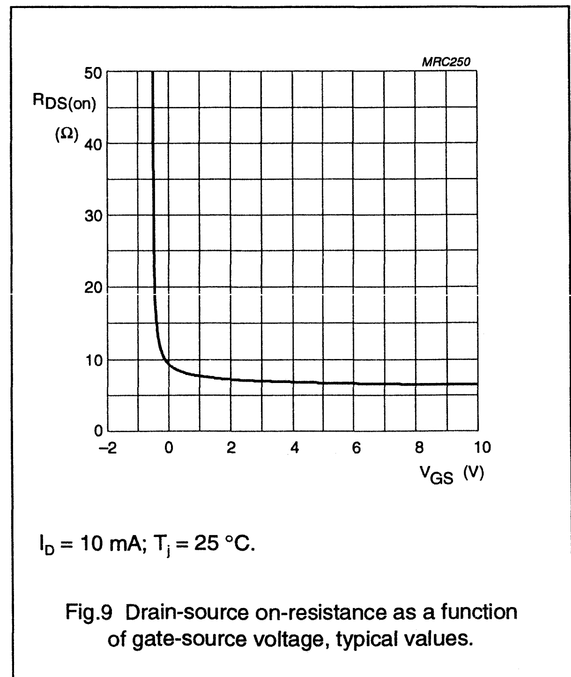
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



I_D = 10 mA; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

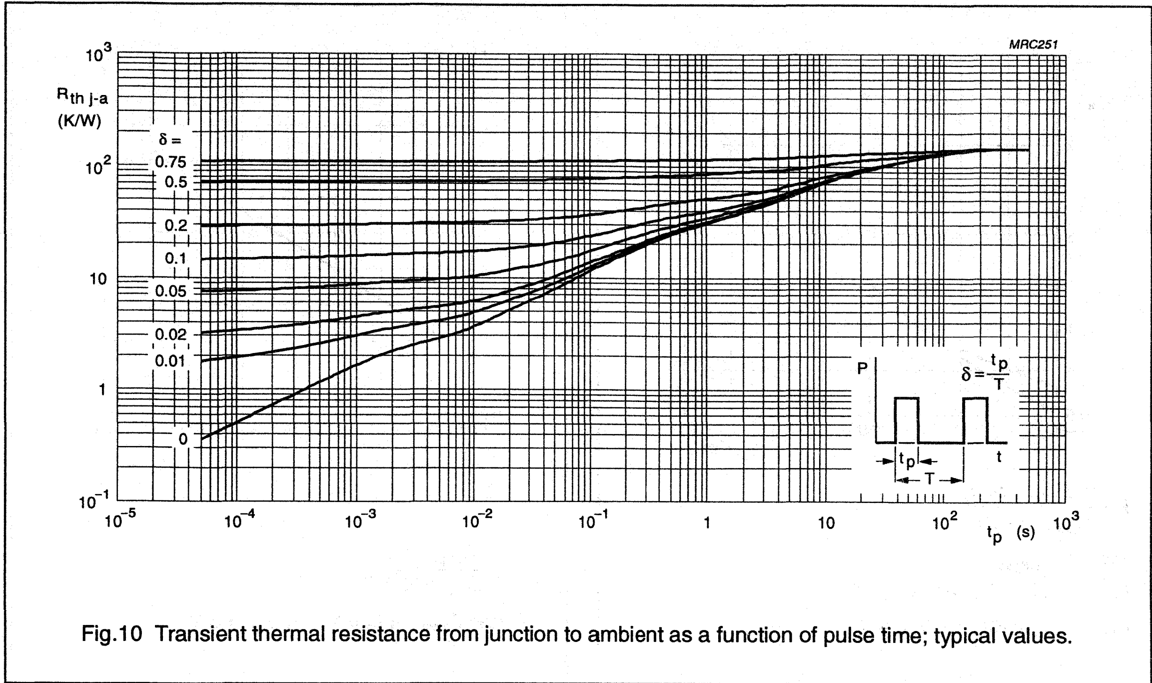
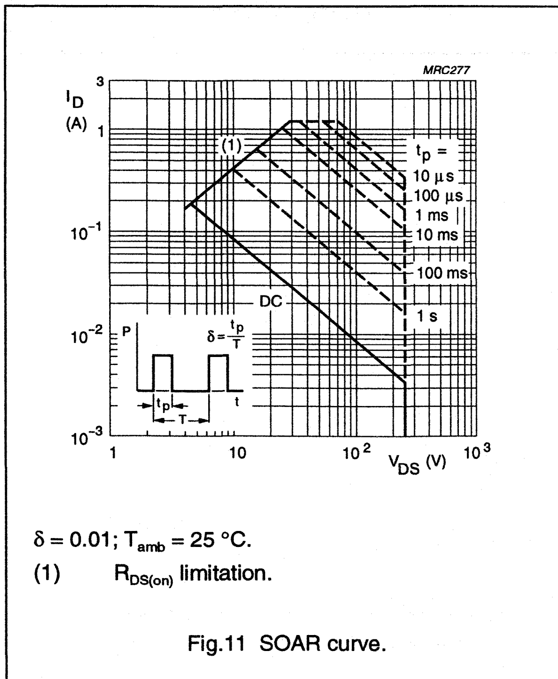


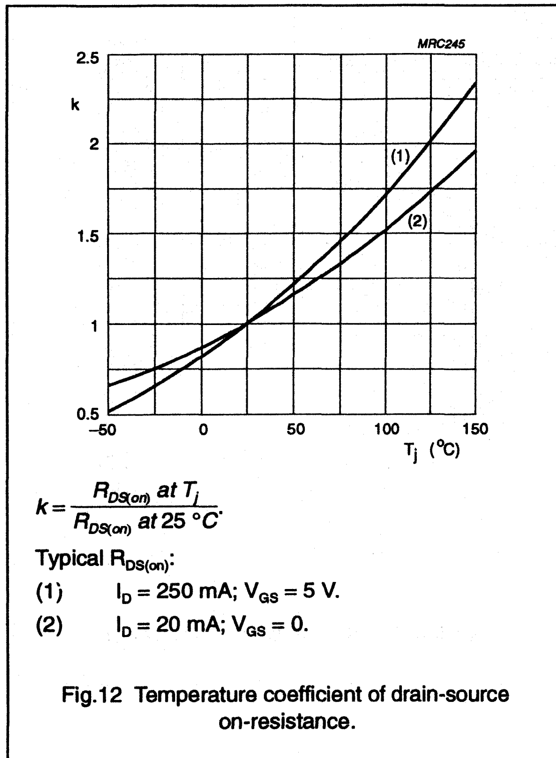
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.



$\delta = 0.01$; $T_{amb} = 25$ °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



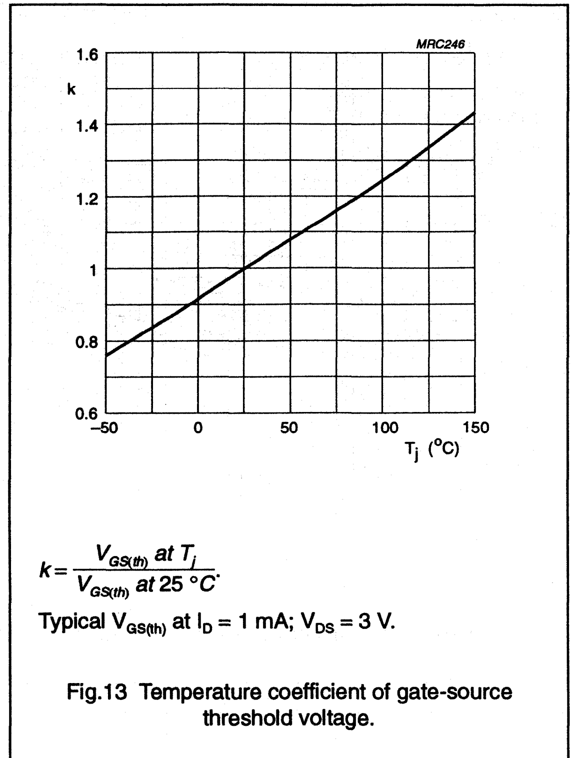
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$:

(1) I_D = 250 mA; V_{GS} = 5 V.

(2) I_D = 20 mA; V_{GS} = 0.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Typical $V_{GS(th)}$ at I_D = 1 mA; V_{DS} = 3 V.

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel silicon field-effect transistors

BSJ108; BSJ109; BSJ110

FEATURES

- High-speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-18 envelope, designed for use in such applications as analog switches, choppers, commutators, etc.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current				
	BSJ108		80	–	mA
	BSJ109		40	–	mA
	BSJ110		10	–	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	275	mW
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 0.1 V; V_{GS} = 0			
	BSJ108		–	8	Ω
	BSJ109		–	12	Ω
	BSJ110		–	18	Ω
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 μA; V_{DS} = 5 V			
	BSJ108		3	10	V
	BSJ109		2	6	V
	BSJ110		0.5	4	V

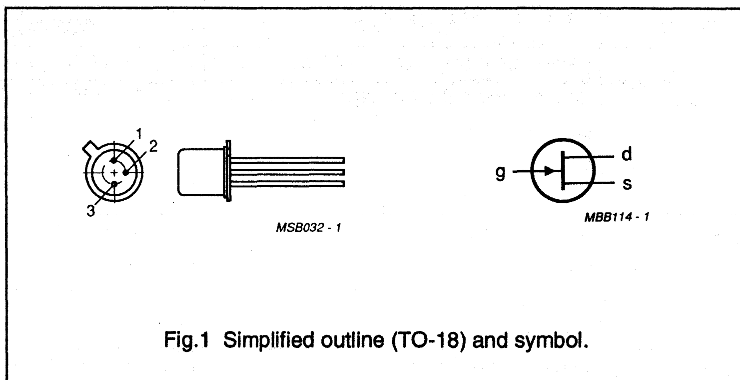


Fig.1 Simplified outline (TO-18) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage	open drain	–	25	V
$-V_{GDO}$	gate-drain voltage	open source	–	25	V
I_G	DC forward gate current		–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	275	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	360 K/W

Note

1. Device mounted on printed circuit board, maximum lead length 4 mm, mounting pad for the drain lead 10 mm x 10 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA; V_{DS} = 0	–	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 μA; V_{DS} = 5 V			
	BSJ108		3	10	V
	BSJ109		2	6	V
	BSJ110		0.5	4	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BSJ108		80	–	mA
	BSJ109		40	–	mA
	BSJ110		10	–	mA
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	3	nA
I_{DSX}	drain-source cut-off current	V_{DS} = 5 V; $-V_{GS}$ = 10 V	–	3	nA
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 0.1 V; V_{GS} = 0			
	BSJ108		–	8	Ω
	BSJ109		–	12	Ω
	BSJ110		–	18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{iss}	input capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	15	30	pF
		V_{DS} = 0; $-V_{GS}$ = 0; T_{amb} = 25 °C; f = 1 MHz	50	85	pF
C_{rss}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	8	15	pF
Switching times; test conditions: V_{DD} = 1.5 V; V_{GS} = 0 to $V_{GS(off)}$; R_L = 100 Ω; $-V_{GS(off)}$ = 12 V (BSJ108), 7 V (BSJ109) and 5 V (BSJ110); (see also Figs 2 and 3)					
t_{on}	turn-on time		4	–	ns
t_{off}	turn-off time		6	–	ns
t_d	delay time		2	–	ns
t_s	storage time		4	–	ns

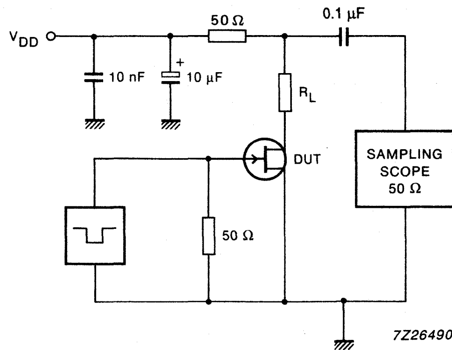


Fig.2 Switching times test circuit.

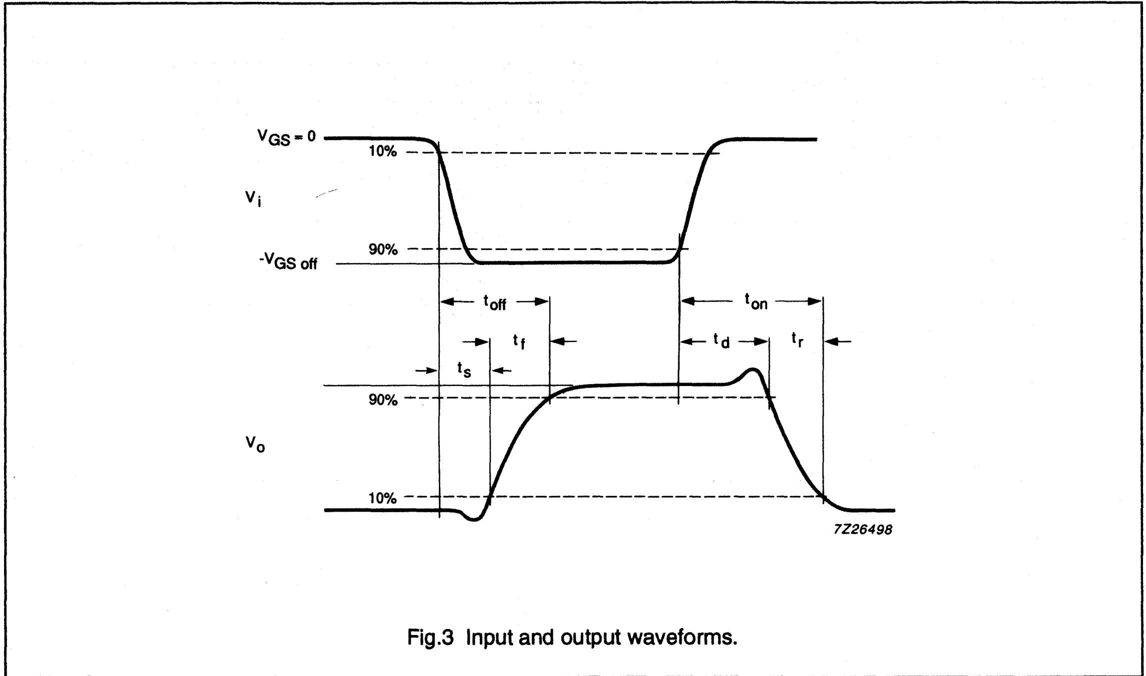


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSN10; BSN10A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use in general purpose fast switching applications.

PINNING

PIN	DESCRIPTION
	BSN10
1	gate
2	drain
3	source
	BSN10A
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	175	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

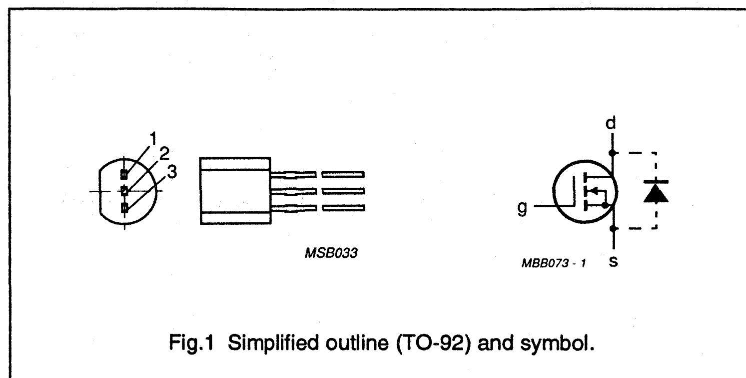


Fig.1 Simplified outline (TO-92) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	175	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	8	15	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	12	20	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	18	30	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	40	80	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	7	15	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns

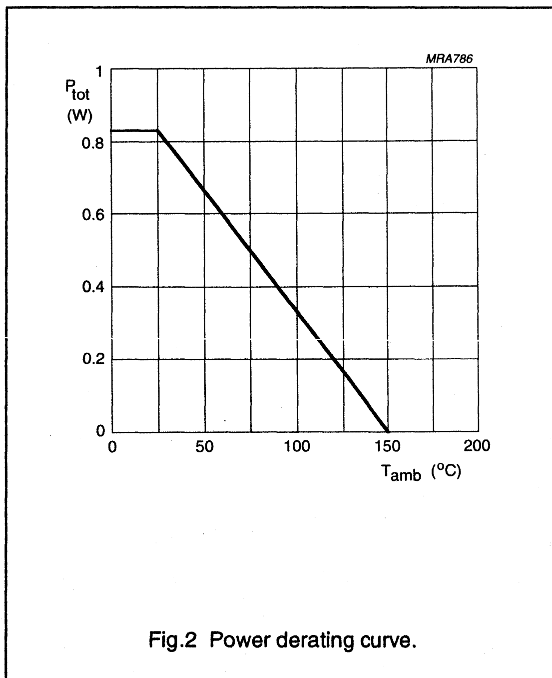
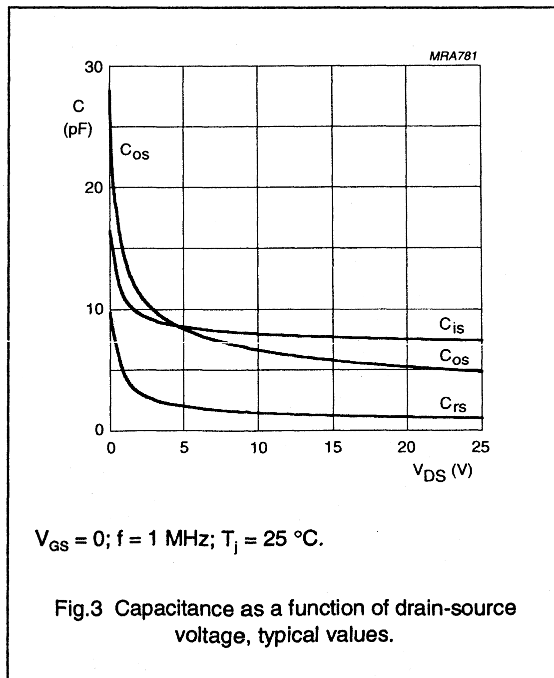
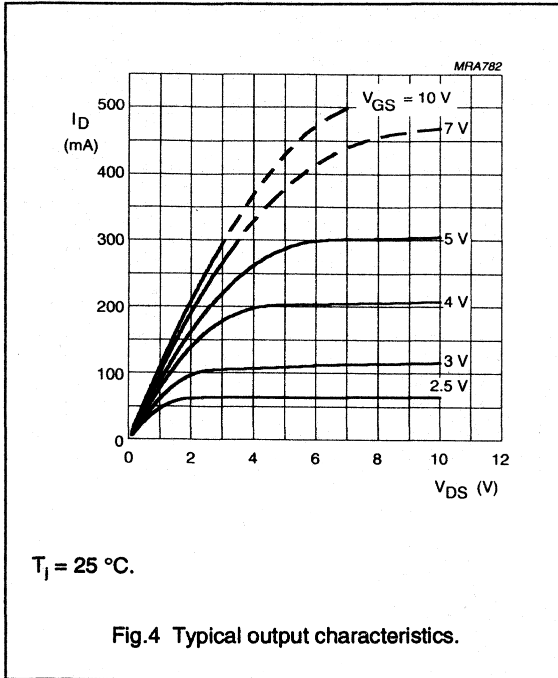


Fig.2 Power derating curve.



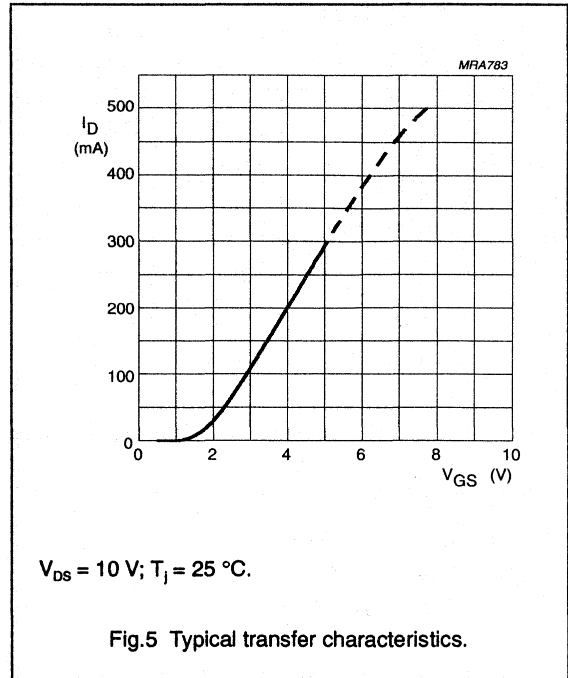
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.3 Capacitance as a function of drain-source voltage, typical values.



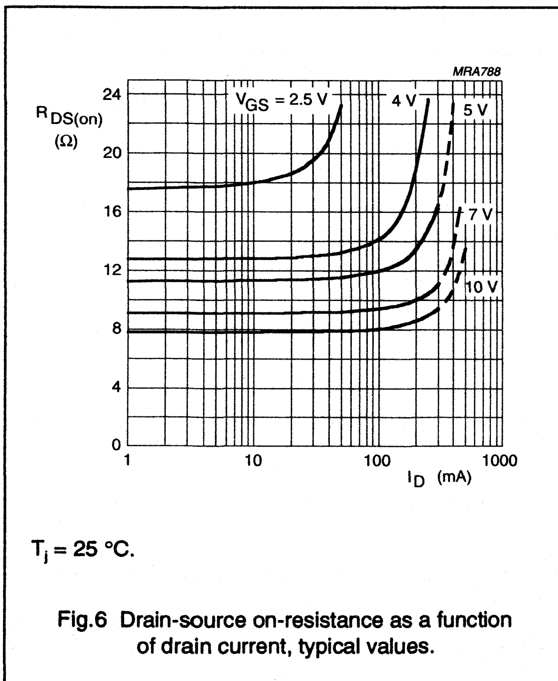
T_j = 25 °C.

Fig.4 Typical output characteristics.



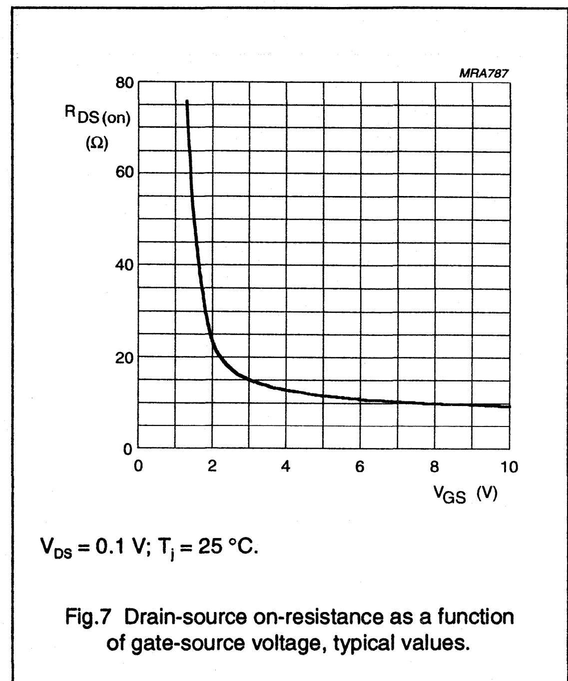
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



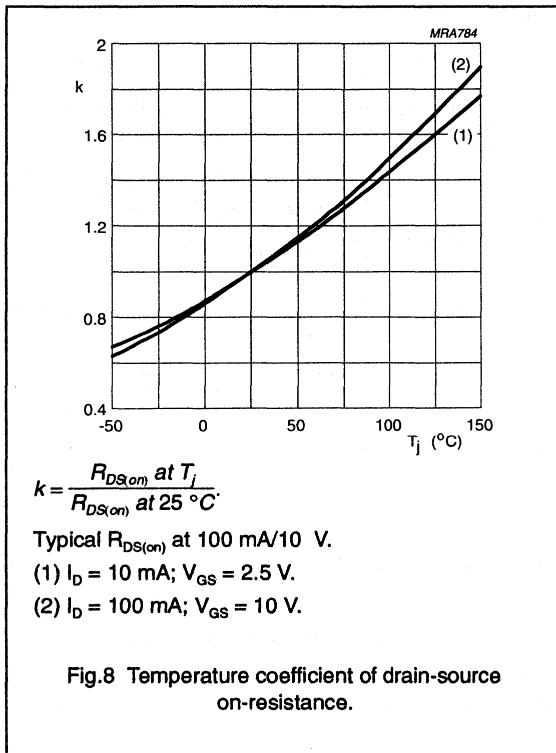
T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

Fig.7 Drain-source on-resistance as a function of gate-source voltage, typical values.



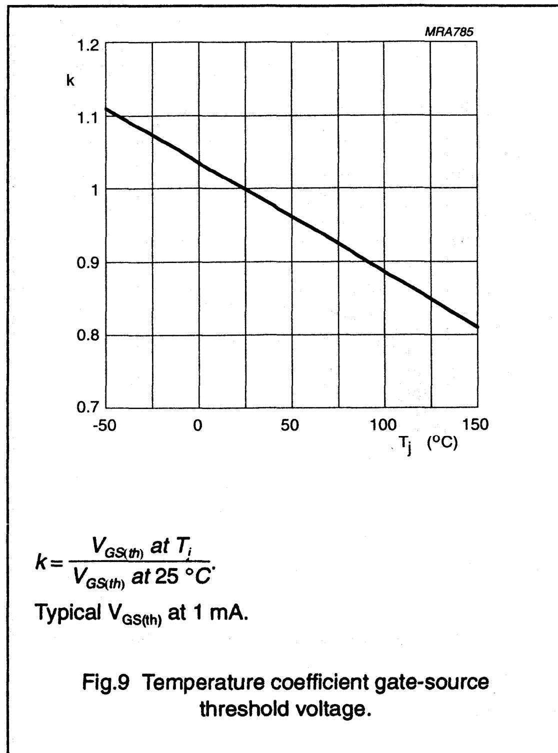
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$ at 100 mA/10 V.

(1) I_D = 10 mA; V_{GS} = 2.5 V.

(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.8 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.9 Temperature coefficient gate-source threshold voltage.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use in general purpose small-signal fast switching applications.

PINNING

PIN	DESCRIPTION
BSN12	
1	gate
2	drain
3	source
BSN12A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	150	mA
$R_{DS(on)}$	drain-source on-resistance	30	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

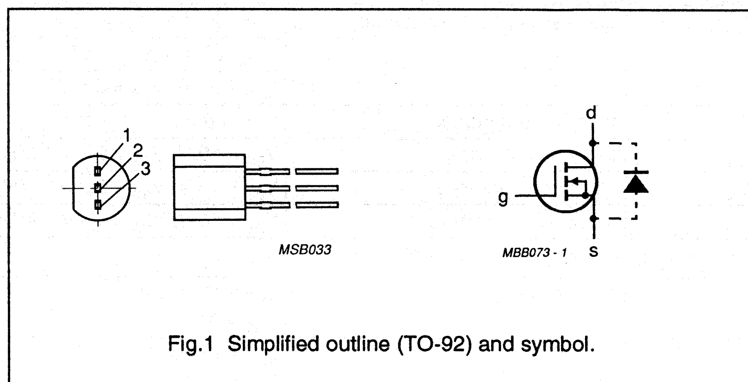


Fig.1 Simplified outline (TO-92) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	150	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm, mounting pad for the drain lead 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	12	20	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	20	30	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	30	50	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	30	60	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	6	10	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	1	3	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	–	4	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	8	ns

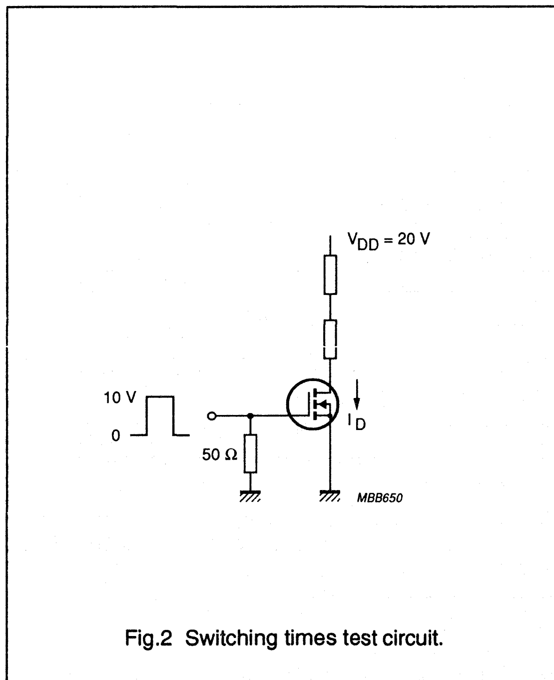


Fig.2 Switching times test circuit.

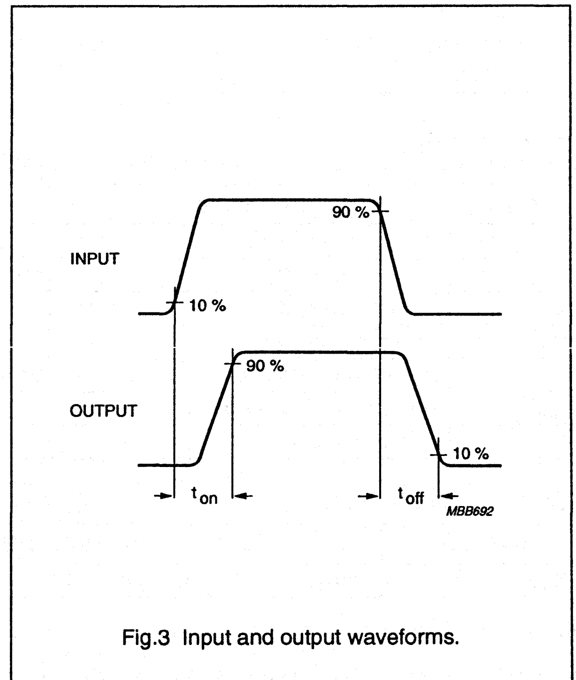


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSN20

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a surface-mounted device in thin and thick film circuits and in general purpose fast switching applications.

PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	100	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

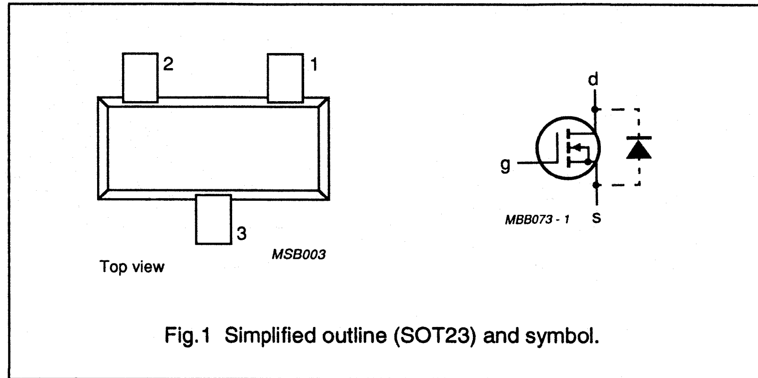


Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	300	mW
		up to T_{amb} = 25 °C (note 2)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430 K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500 K/W

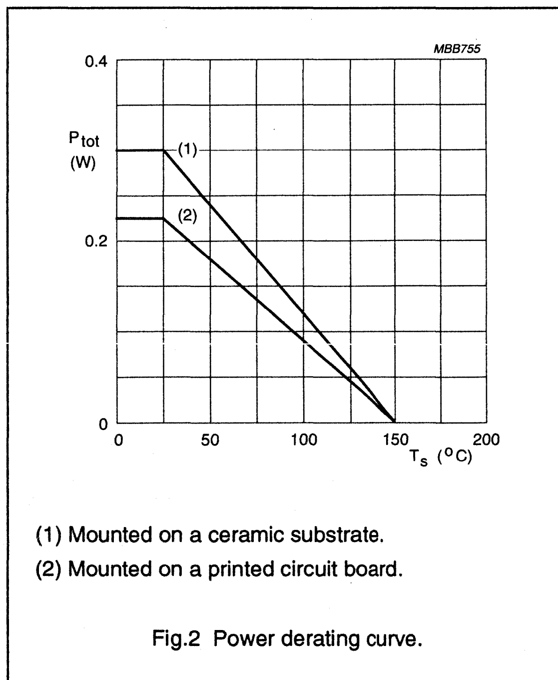
Notes

1. Transistor mounted on a ceramic substrate, 10 x 8 x 0.7 mm.
2. Transistor mounted on a printed circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

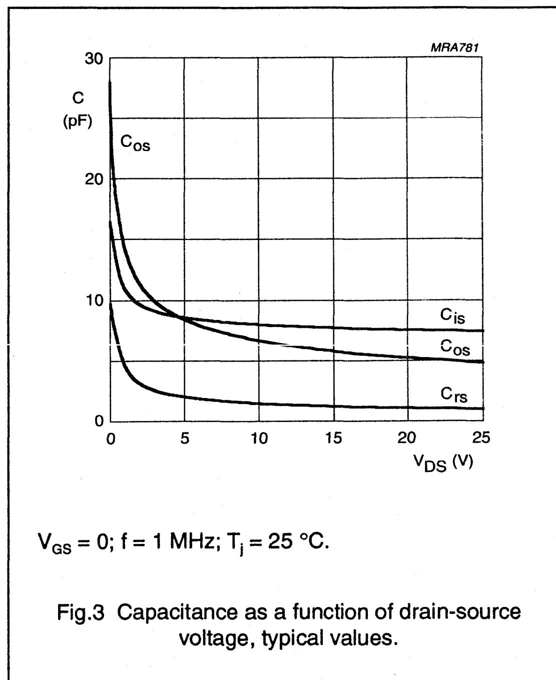
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	8	15	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	14	20	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	18	30	Ω
$\lvert Y_{fs}\rvert$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	40	80	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	7	15	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	5	10	ns



(1) Mounted on a ceramic substrate.

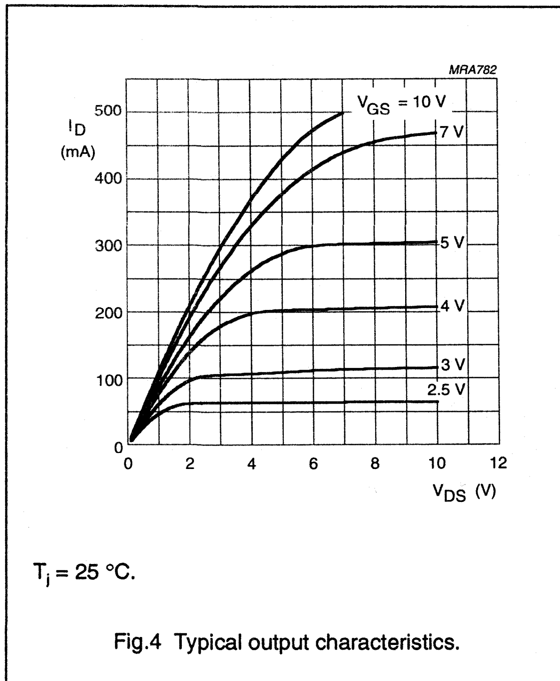
(2) Mounted on a printed circuit board.

Fig.2 Power derating curve.



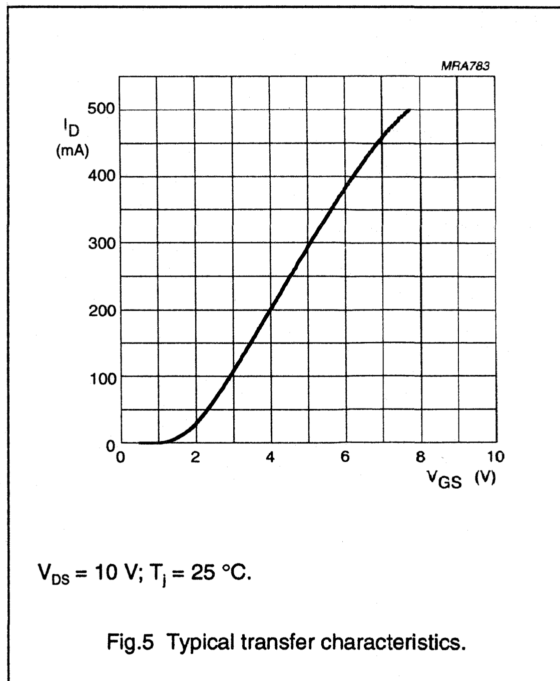
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.3 Capacitance as a function of drain-source voltage, typical values.



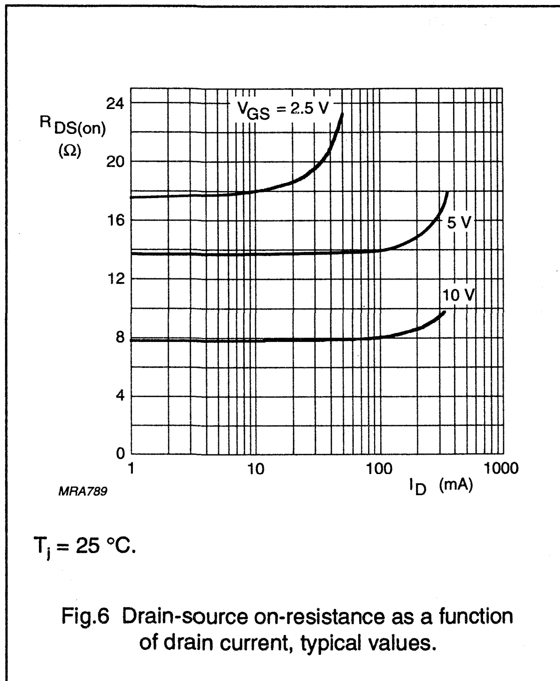
T_j = 25 °C.

Fig.4 Typical output characteristics.



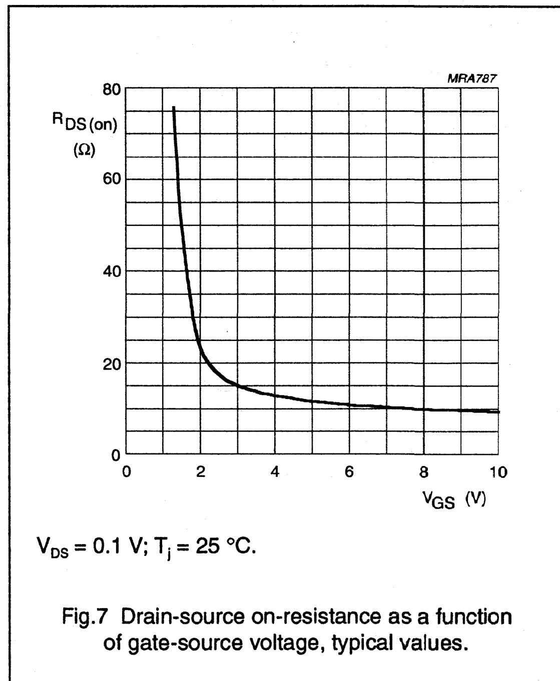
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



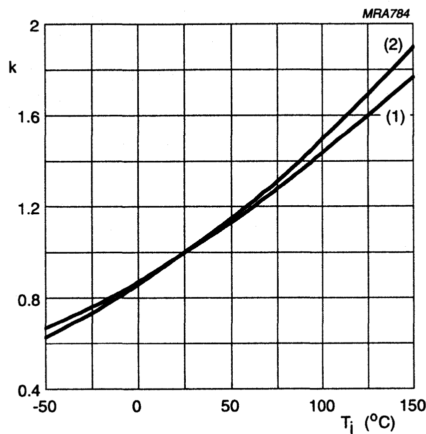
T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

Fig.7 Drain-source on-resistance as a function of gate-source voltage, typical values.



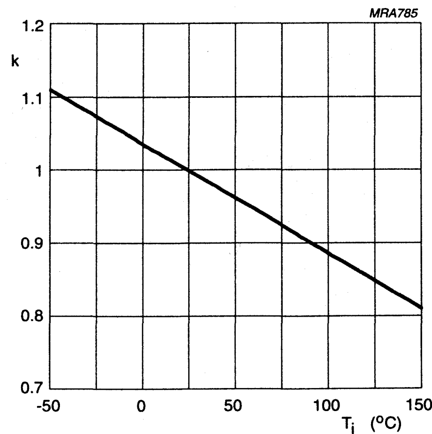
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$ at 100 mA/10 V.

(1) I_D = 10 mA; V_{GS} = 2.5 V.

(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.8 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSN22

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a surface-mounted device in general purpose small-signal fast switching applications.

PINNING

PIN	DESCRIPTION
Code: M18	
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	100	mA
$R_{DS(on)}$	drain-source on-resistance	50	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

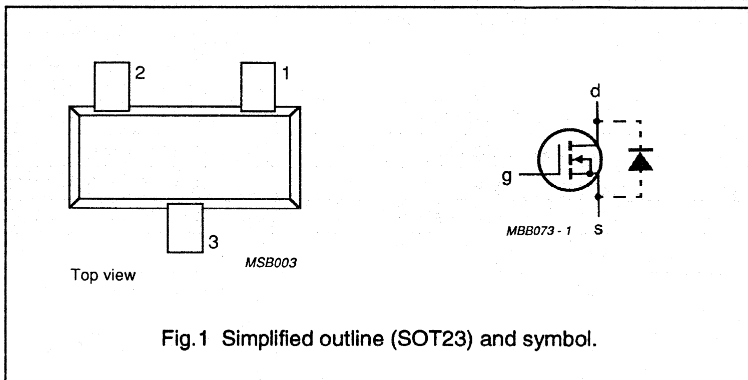


Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Transistor mounted on an FR-4 printboard.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	12	20	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	20	30	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	30	50	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	30	60	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	6	10	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	1	3	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	–	4	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	8	ns

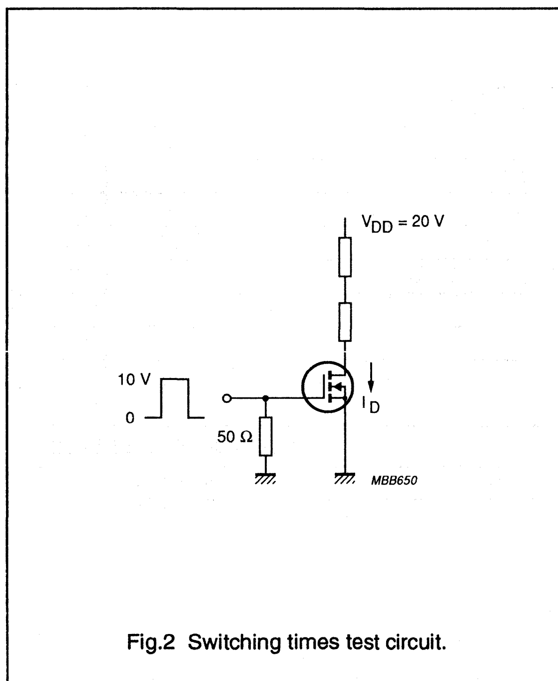


Fig.2 Switching times test circuit.

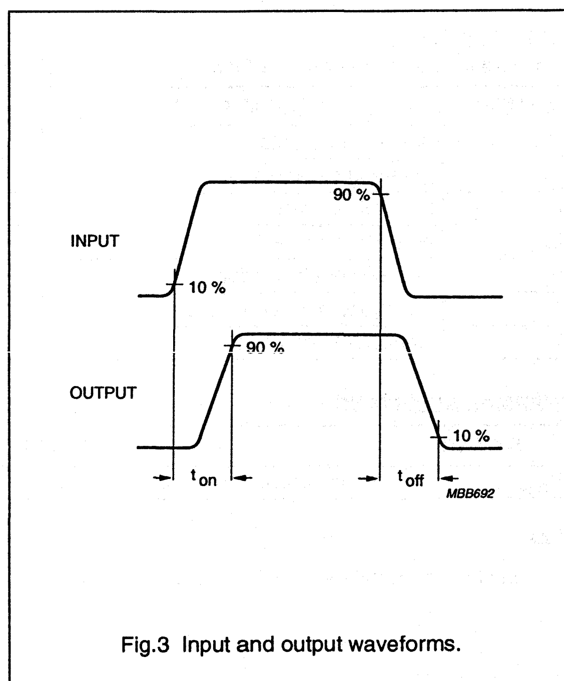


Fig.3 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	December 1990

BSN204/BSN204A
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 (BSN204)

PIN	DESCRIPTION
1	source
2	gate
3	drain

PINNING - TO-92 (BSN204A)

PIN	DESCRIPTION
1	gate
2	drain
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA V_{GS} = 2.8 V	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	1.8	V

PIN CONFIGURATION

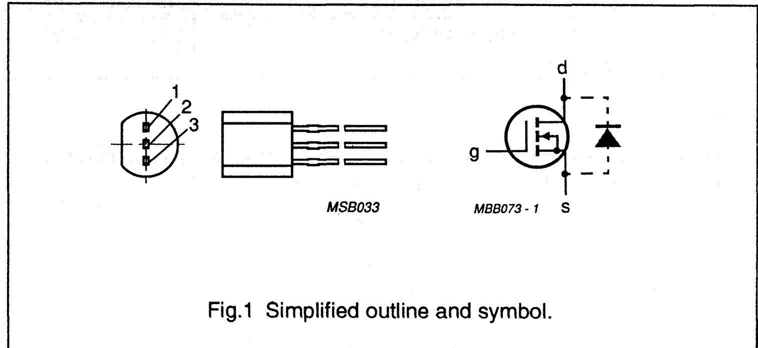


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	250	mA
I_{DM}	drain current	peak value	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.4	1	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA V_{GS} = 2.8 V	–	5	8	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 300 mA V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	20	30	ns

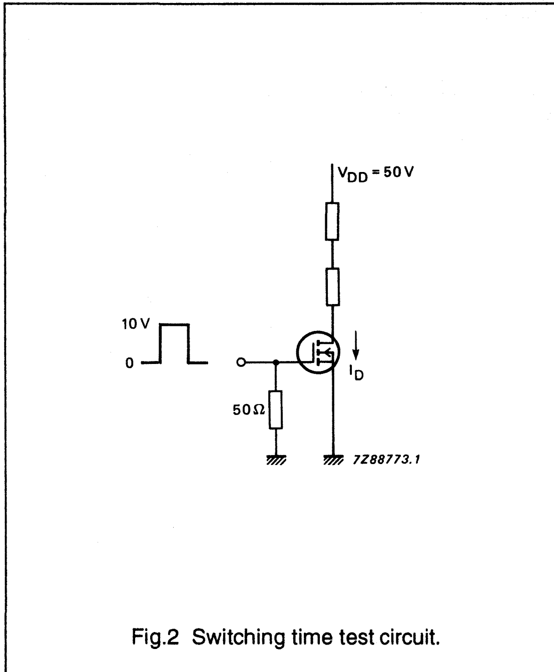


Fig.2 Switching time test circuit.

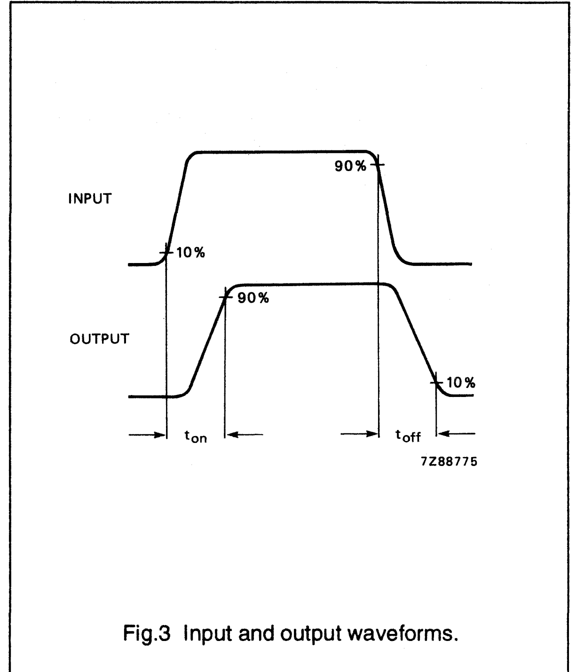


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Parameter	Symbol		Value
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5 Ω
		max.	6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	200 mS
		typ.	350 mS

MECHANICAL DATA

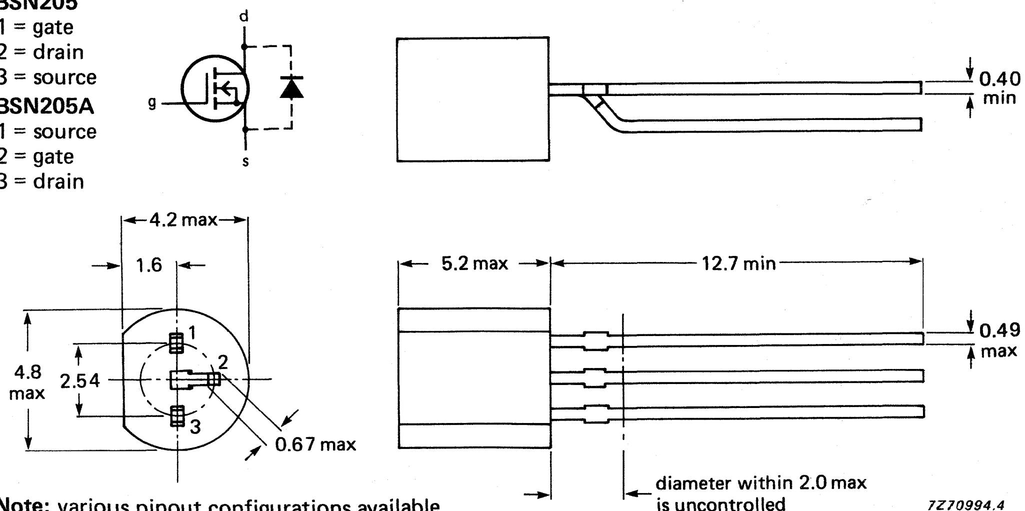
Dimensions in mm

Fig.1 TO-92 variant.

Pinning

BSN205
1 = gate
2 = drain
3 = source

BSN205A
1 = source
2 = gate
3 = drain



Note: various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	15 ns 20 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

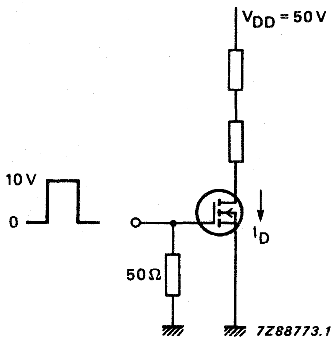


Fig.2 Switching time test circuit.

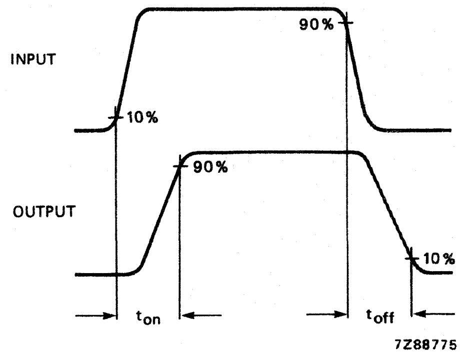


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTORS

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 7.0	Ω Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2	V

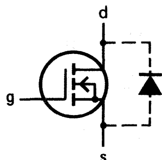
MECHANICAL DATA

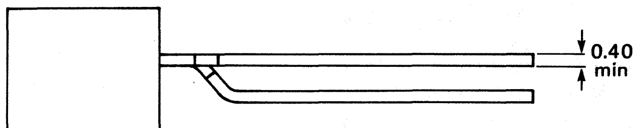
Dimensions in mm

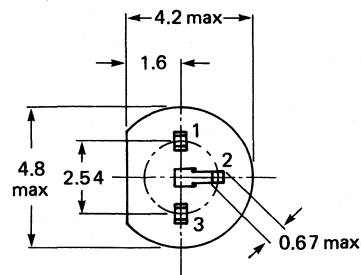
Fig.1 TO-92 variant.

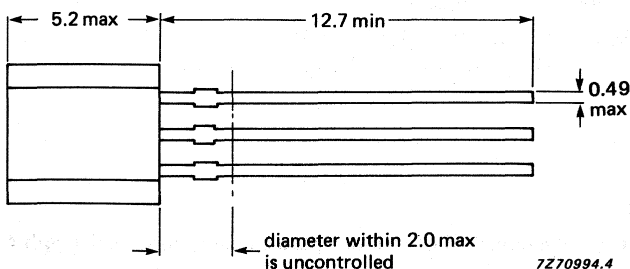
Pinning (BSN254)
1 = gate
2 = drain
3 = source

Pinning (BSN254A)
1 = source
2 = gate
3 = drain









Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250	V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1	μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.0	V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
I_D = 20mA; V_{GS} = 2.4V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs}\rvert$	min.	200	mS
		typ.	400	mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	65	pF
		max.	90	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	15	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD}= 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5	ns
		max.	10	ns
	t_{off}	typ.	20	ns
		max.	30	ns

Note

1. Device mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

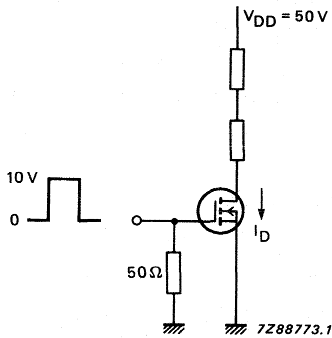


Fig.2 Switching times test circuit.

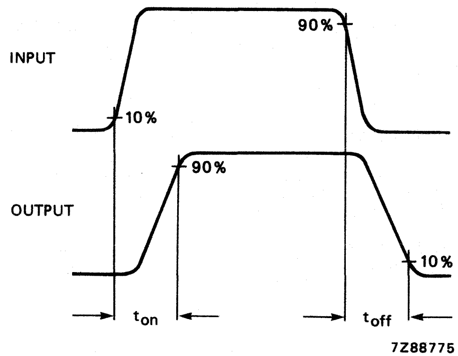


Fig.3 Input and output waveforms.

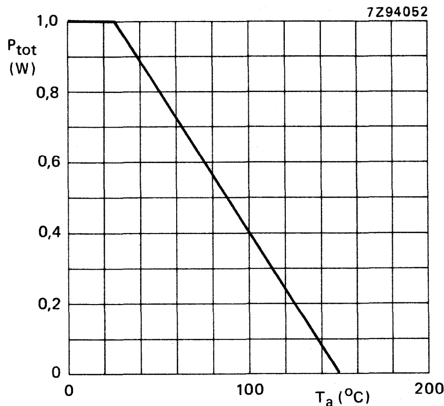


Fig.4 Power derating curve.

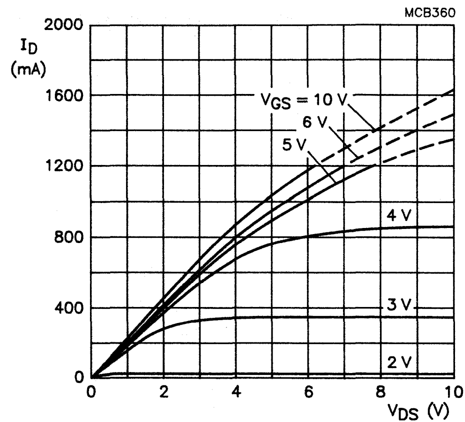


Fig.5 Output characteristics; T_j = 25 °C; typical values.

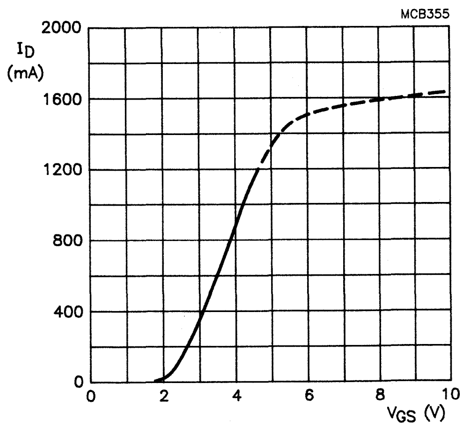


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

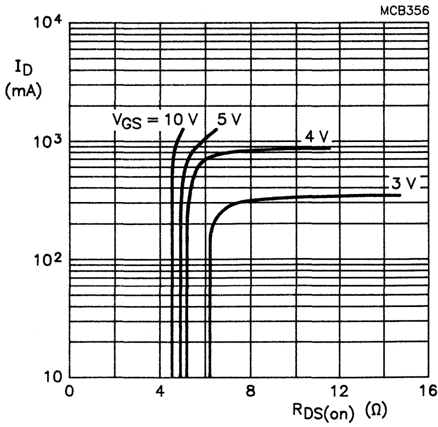


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

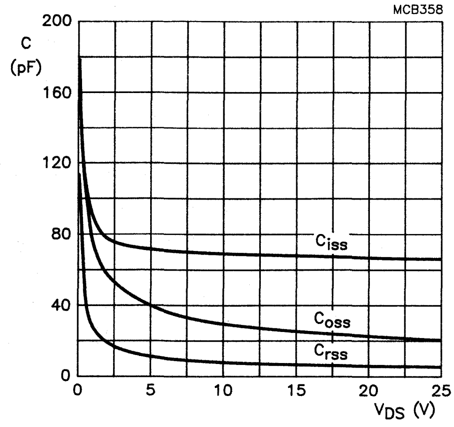


Fig.8 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

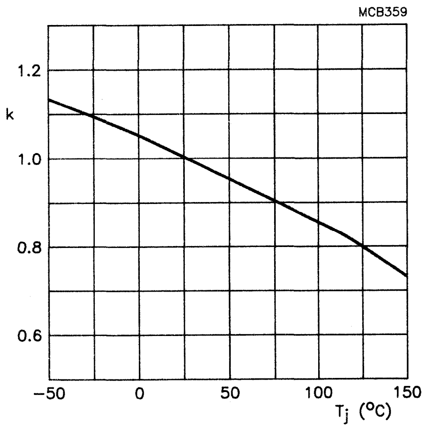


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$;

$V_{GS(th)}$ at 1 mA; typical values.

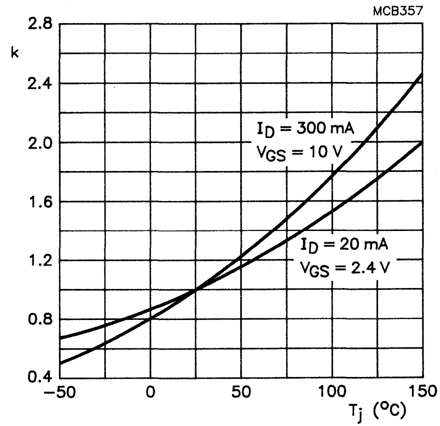


Fig.10 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^oC}$;

typical values.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October 1990

BSN274/BSN274A

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	drain current (DC)	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	threshold voltage	2	V

MECHANICAL DATA

Dimensions in mm

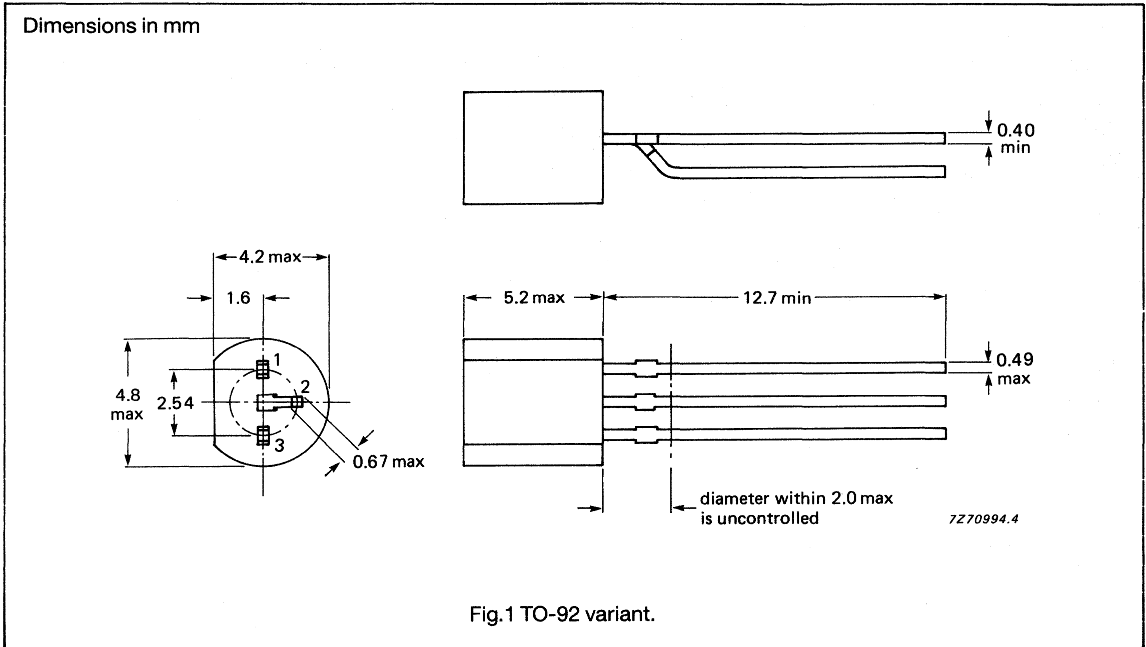


Fig.1 TO-92 variant.

PIN CONFIGURATION

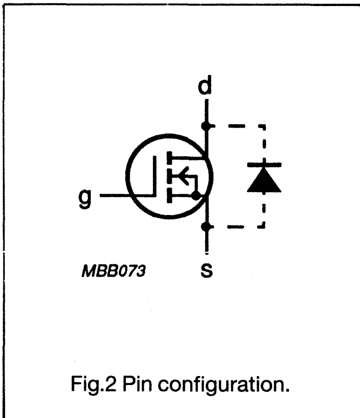


Fig.2 Pin configuration.

PINNING (BSN274)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING (BSN274A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	250	mA
I_{DM}	drain current	peak	-	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain leads minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	270	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V V_{GS} = 0	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA V_{GS} = 10 V	-	6.5	8	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.4 V	-	9	14	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA V_{DS} = 25 V	200	400	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	65	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	5	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	20	30	ns

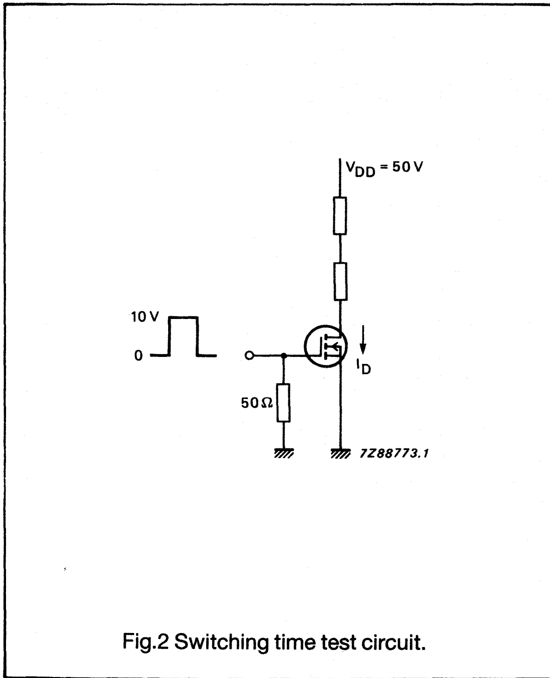


Fig.2 Switching time test circuit.

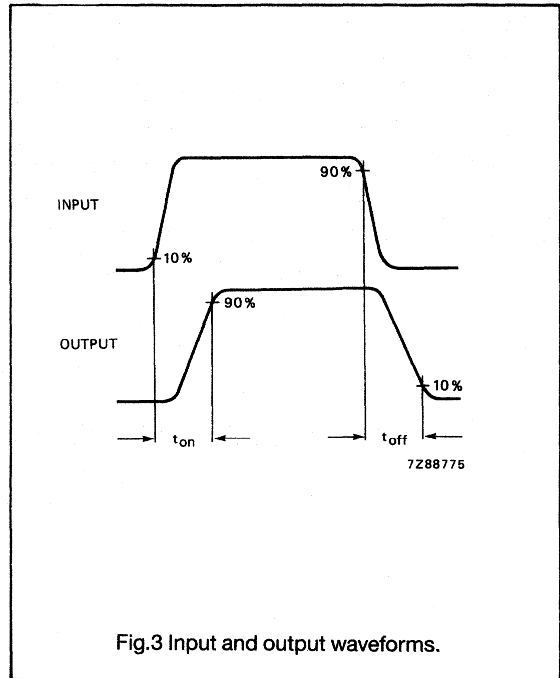


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSN304; BSN304A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
BSN304	
1	gate
2	drain
3	source
BSN304A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{GS} = V_{DS}$	0.8	2	V

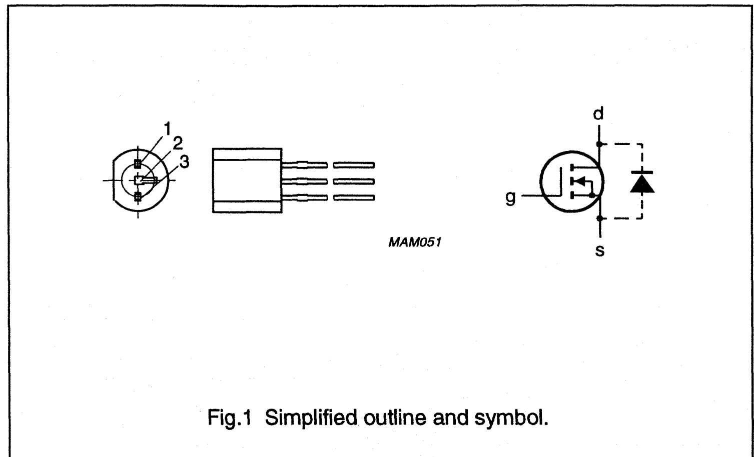


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	125 K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

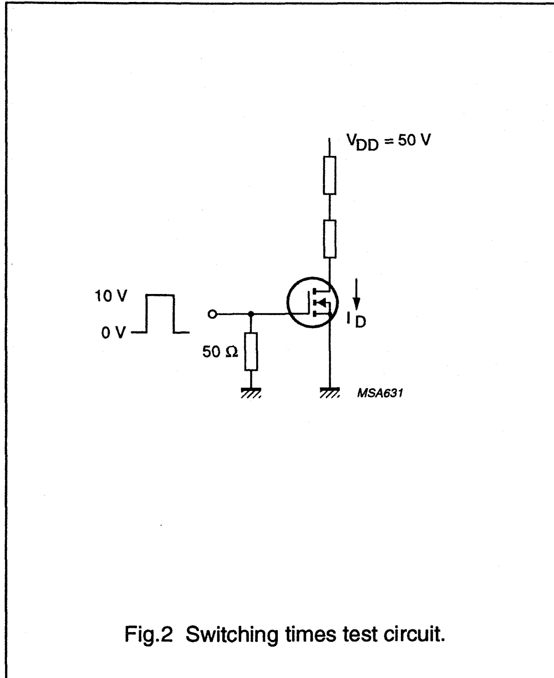


Fig.2 Switching times test circuit.

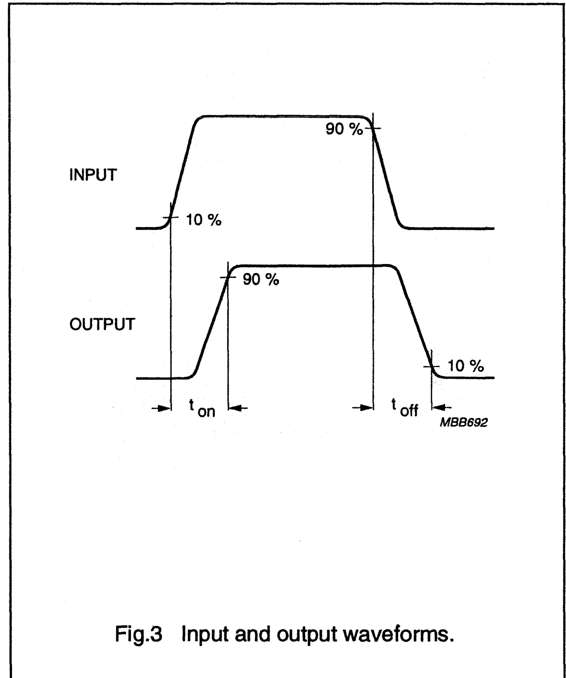


Fig.3 Input and output waveforms.

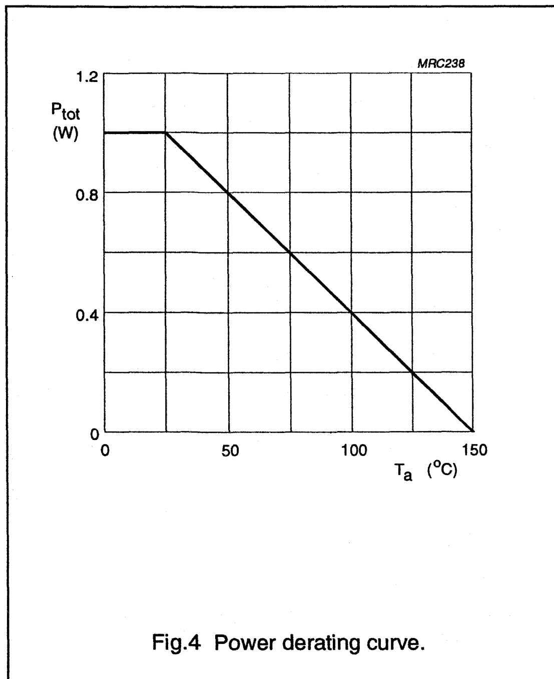
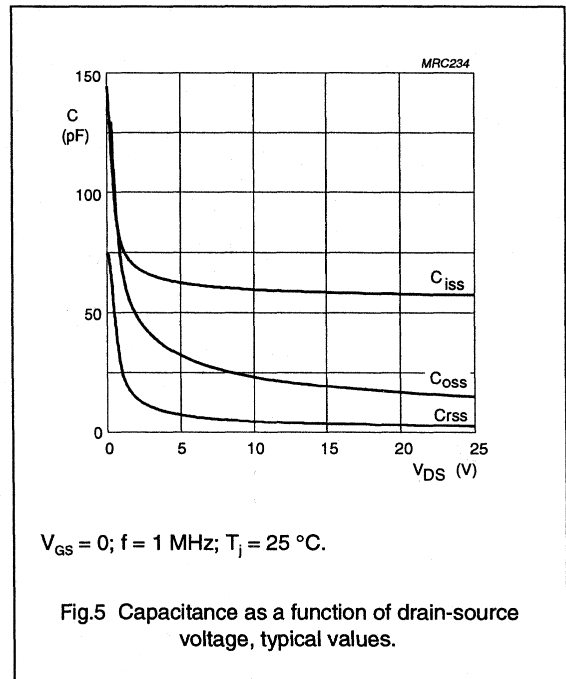
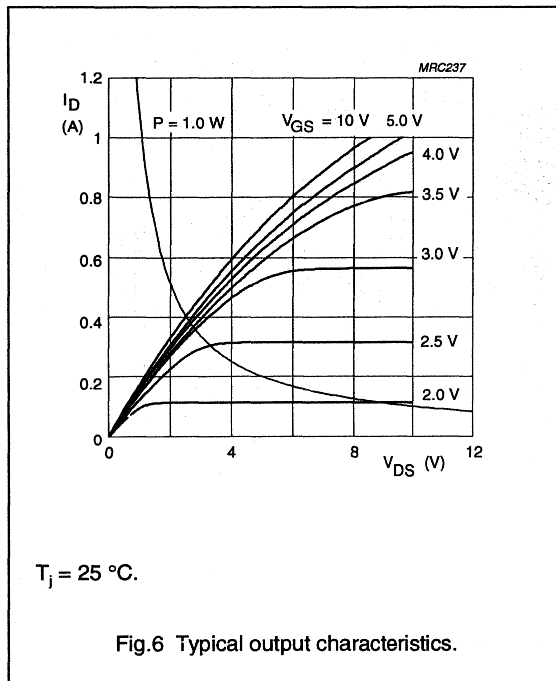


Fig.4 Power derating curve.



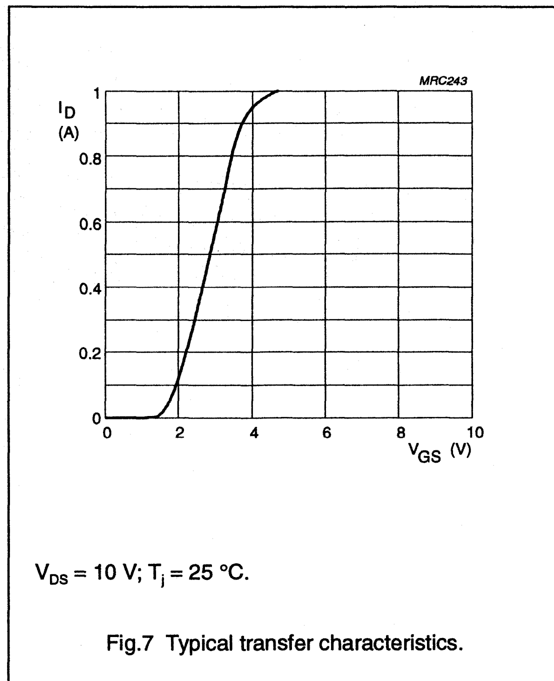
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



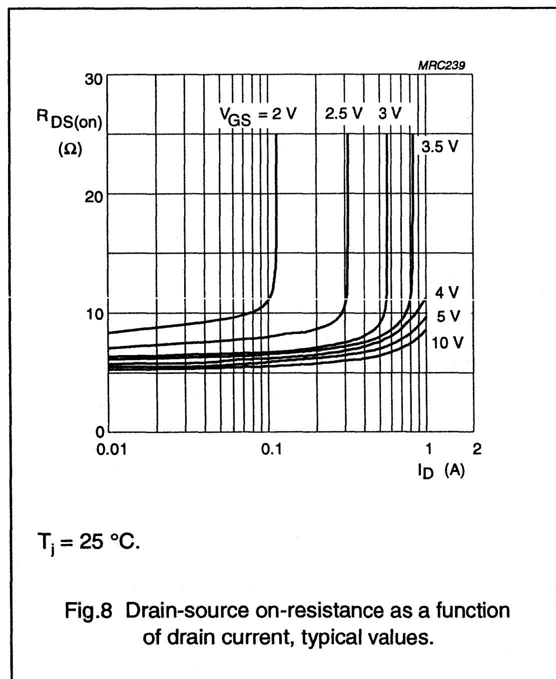
T_j = 25 °C.

Fig.6 Typical output characteristics.



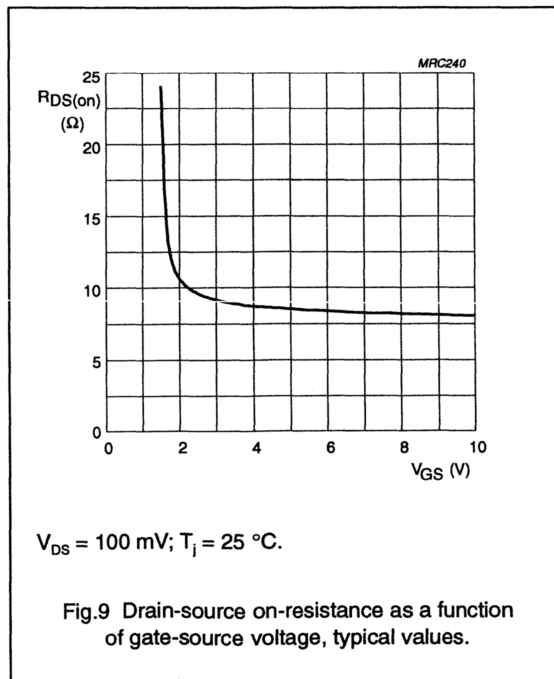
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

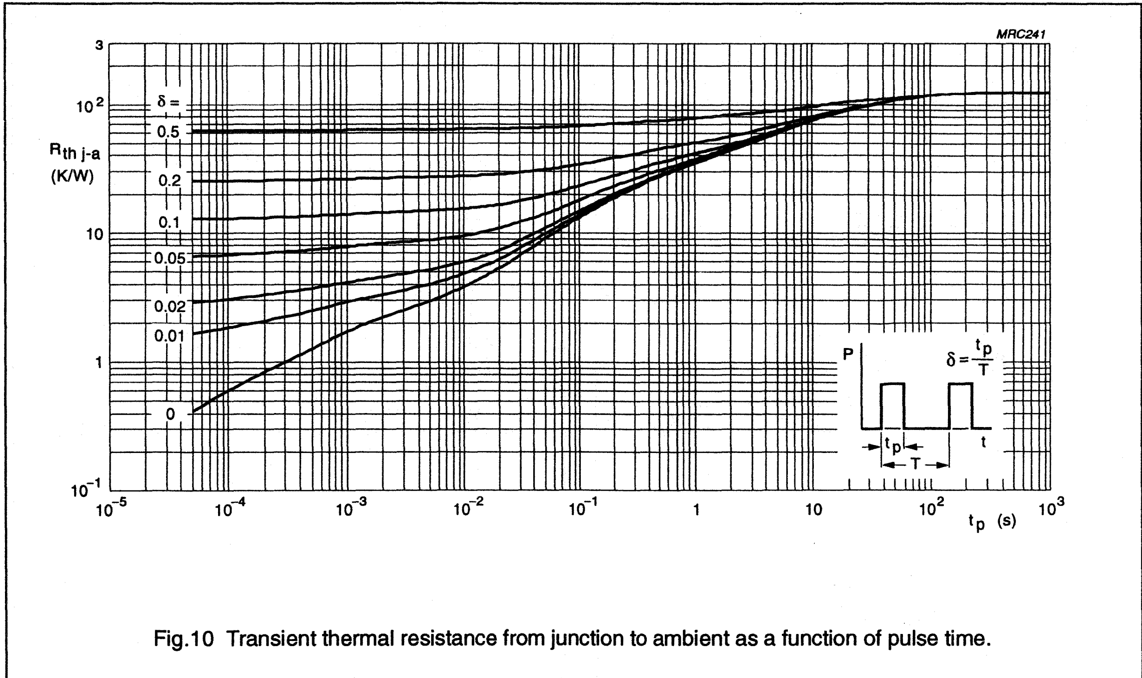
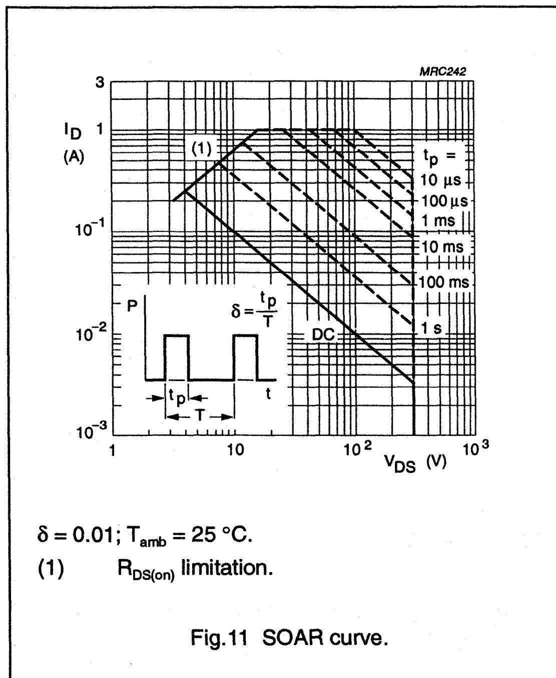


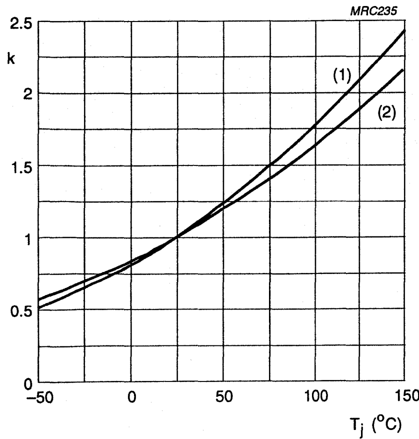
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



$\delta = 0.01$; $T_{amb} = 25$ °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



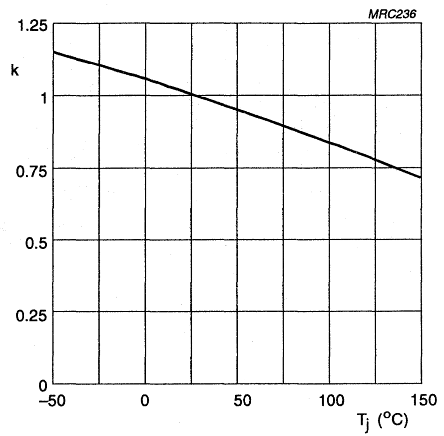
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 10 V.

(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSP89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptors in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

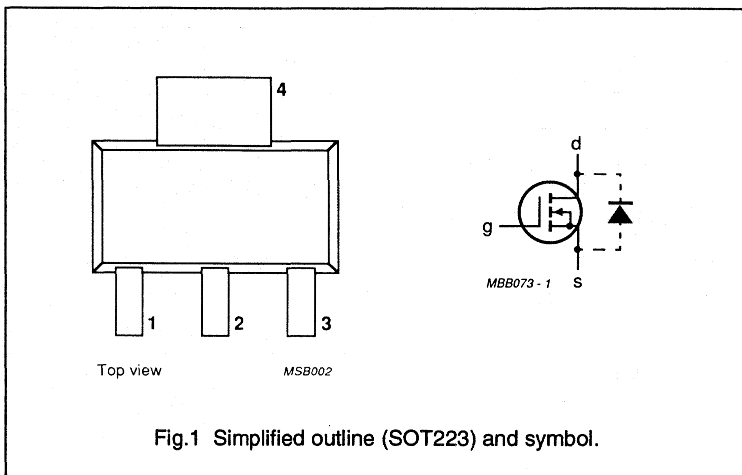


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	240	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	200	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 340 mA; V_{GS} = 10 V	–	4	6	Ω
		I_D = 340 mA; V_{GS} = 4.5 V	–	–	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 340 mA; V_{DS} = 25 V	140	350	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	65	140	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	9	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

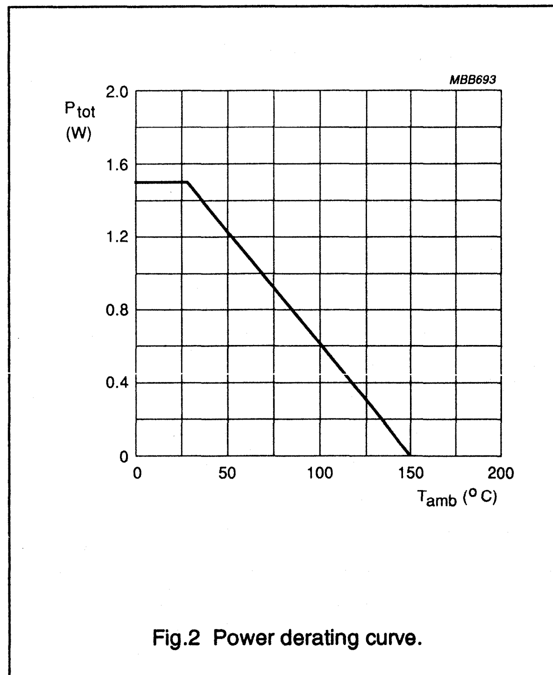
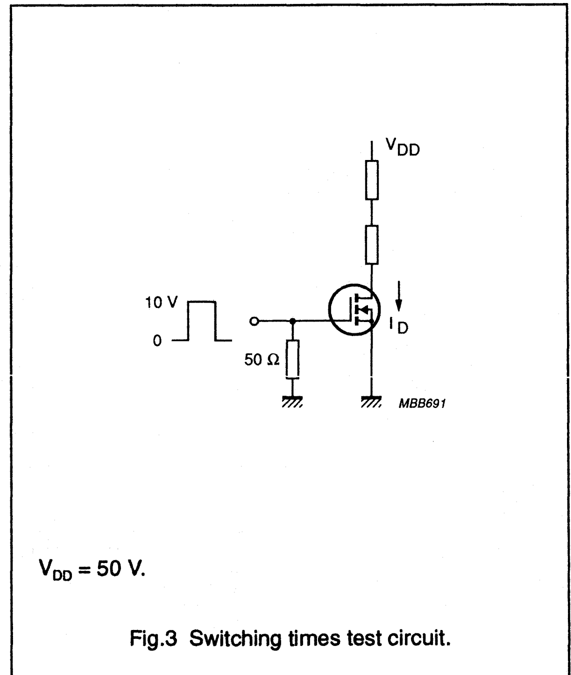


Fig.2 Power derating curve.



V_{DD} = 50 V.

Fig.3 Switching times test circuit.

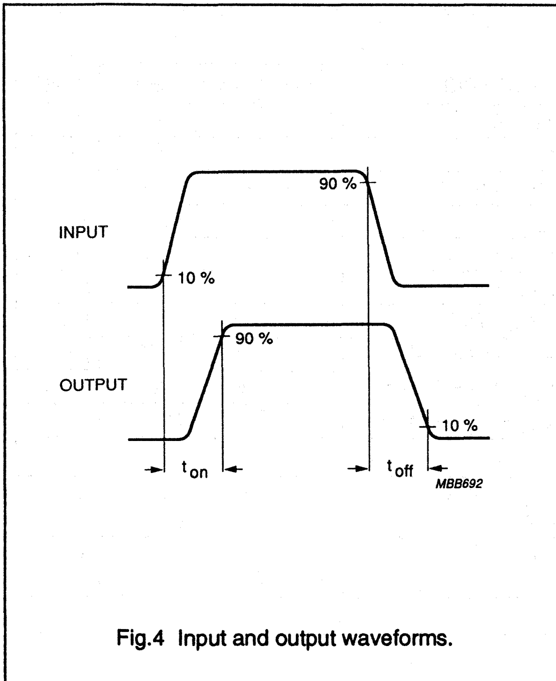


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSP92

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V

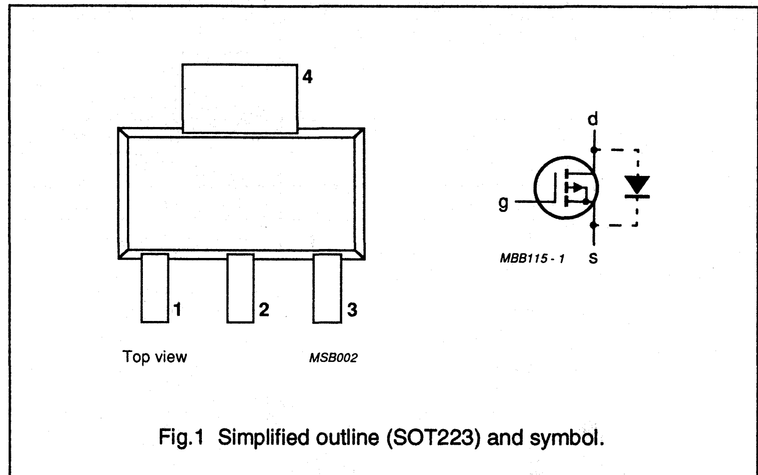


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 µA; V_{GS} = 0	240	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V; V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$-V_{GS}$	gate-source voltage	$-I_D$ = 50 mA; $-V_{DS}$ = 5 V	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 180 mA; $-V_{GS}$ = 10 V	–	10	20	Ω
		$-I_D$ = 100 mA; $-V_{GS}$ = 5 V	–	–	18	Ω
		$-I_D$ = 25 mA; $-V_{GS}$ = 2.8 V	–	–	20	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 180 mA; $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	6	15	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	20	30	ns

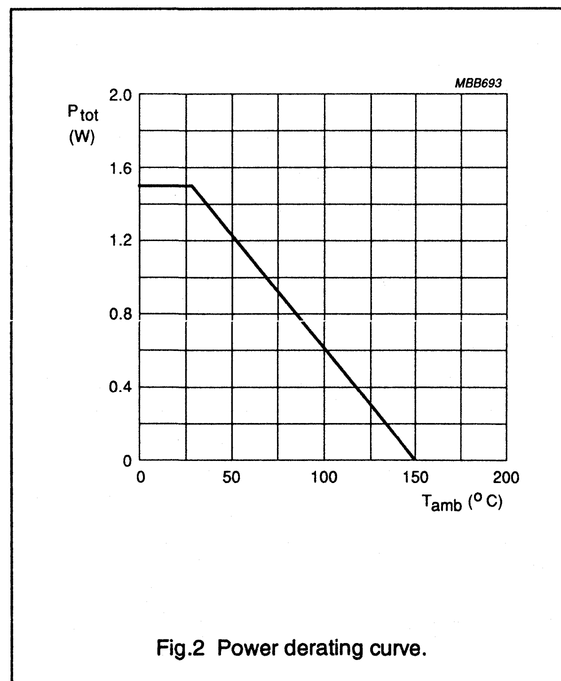
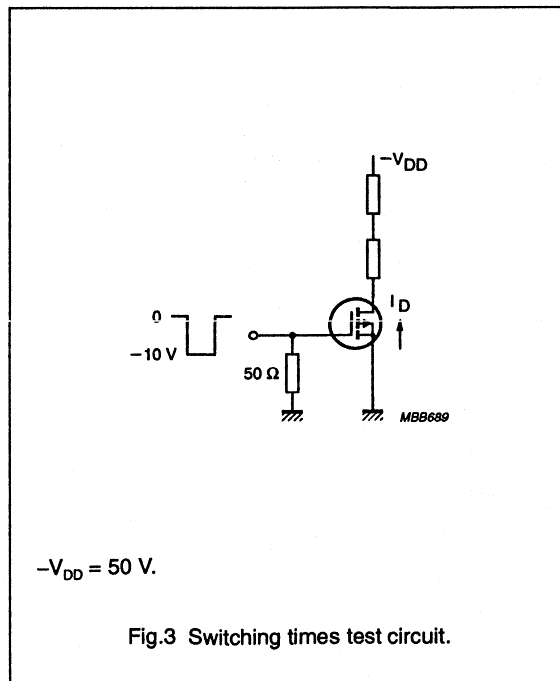


Fig.2 Power derating curve.



$-V_{DD}$ = 50 V.

Fig.3 Switching times test circuit.

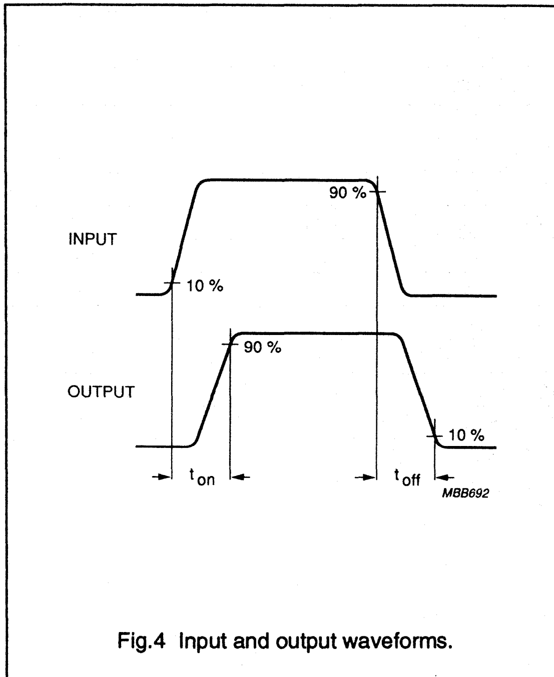


Fig.4 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October 1990

BSP106
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage	–	60	V
I_D	drain current	DC value	425	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	4	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

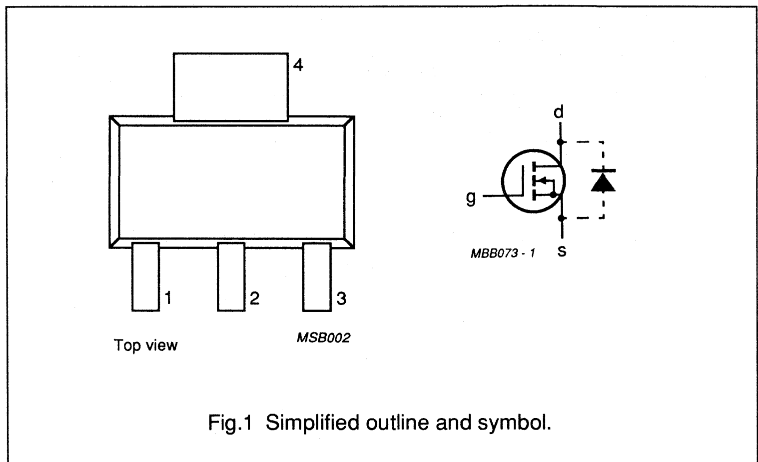


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP106

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
I_D	drain current	DC value	–	425	mA
I_{DM}	drain current	peak value	–	850	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
		V_{DS} = 25 V V_{GS} = 0	–	–	0.5	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	–	2.5	4	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10	–	10	15	ns

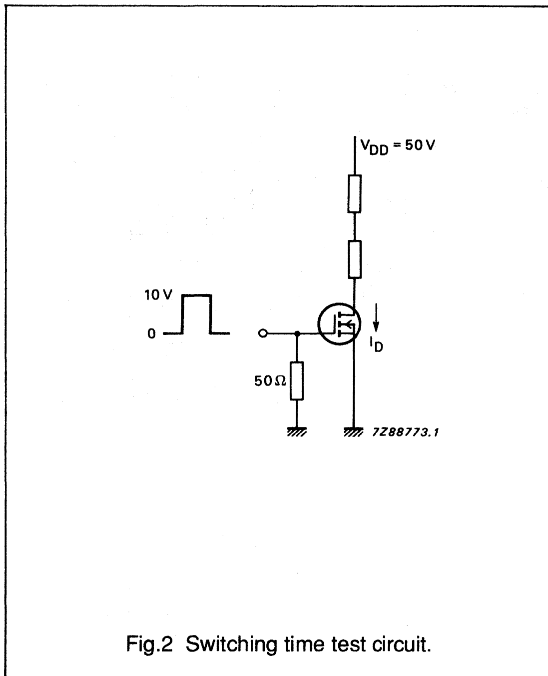


Fig.2 Switching time test circuit.

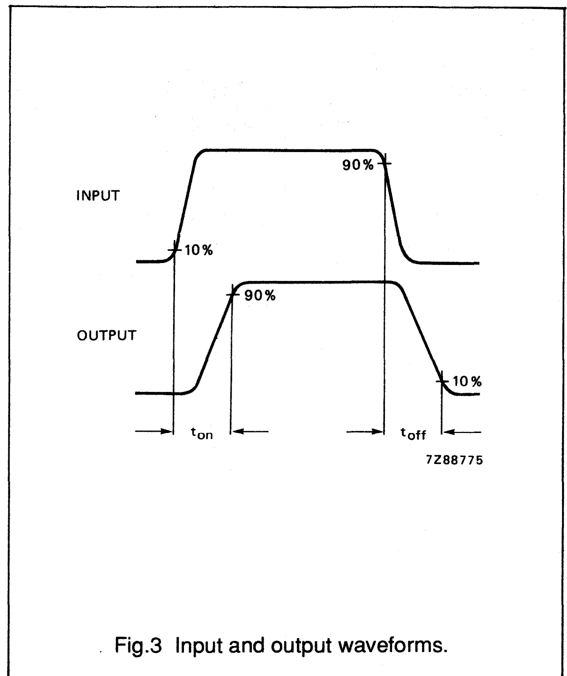


Fig.3 Input and output waveforms.

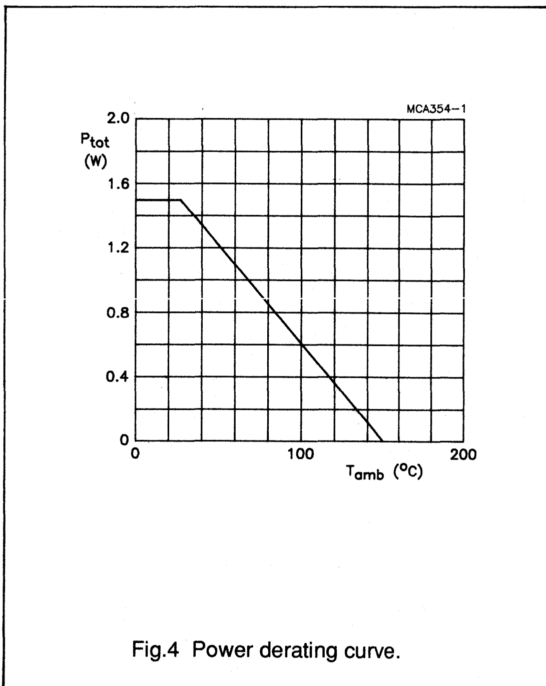


Fig.4 Power derating curve.

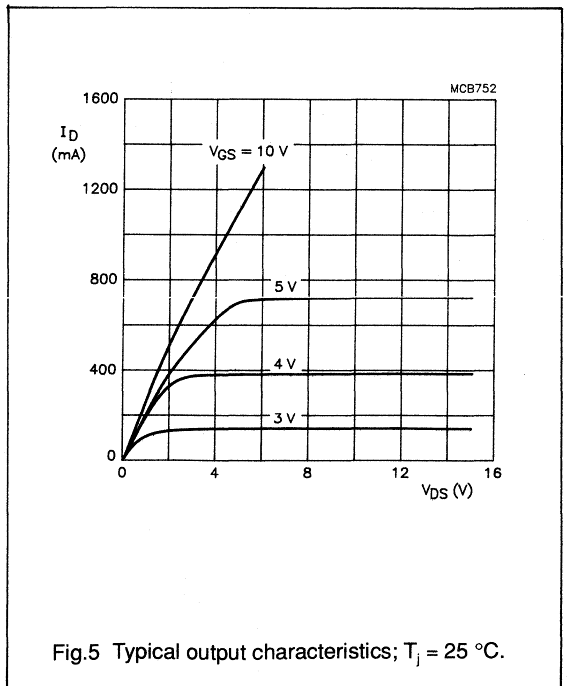


Fig.5 Typical output characteristics; T_j = 25 °C.

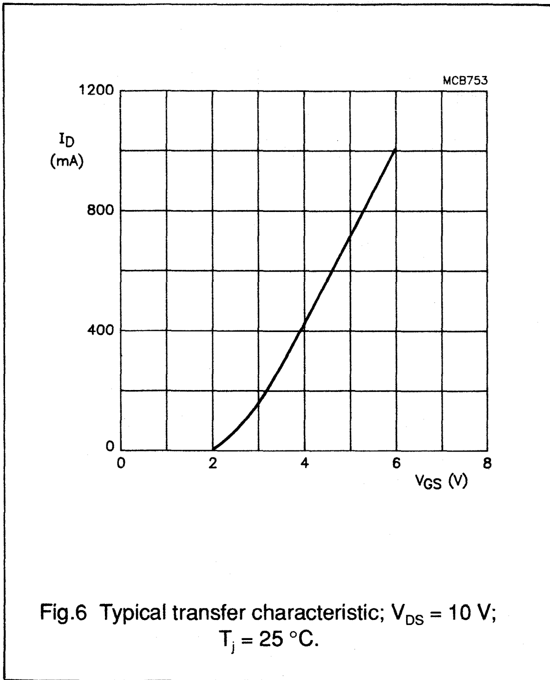


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

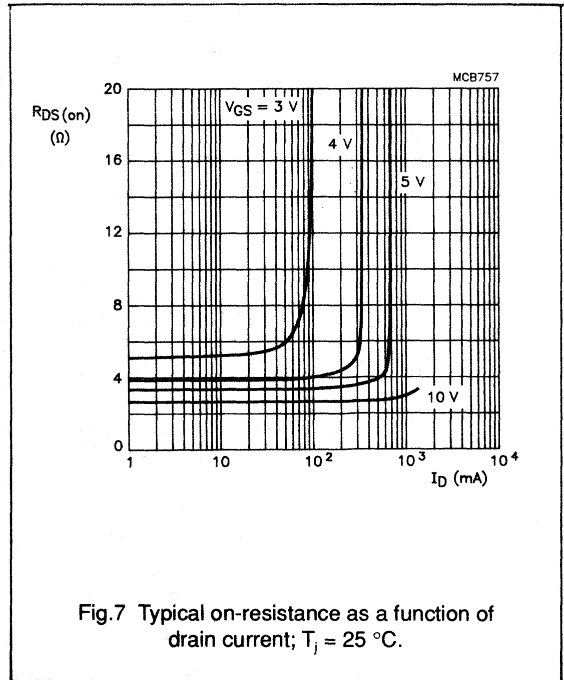


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

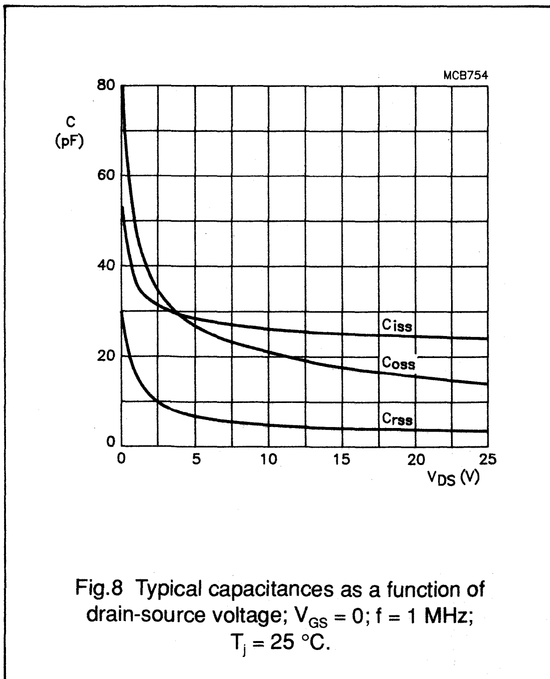


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

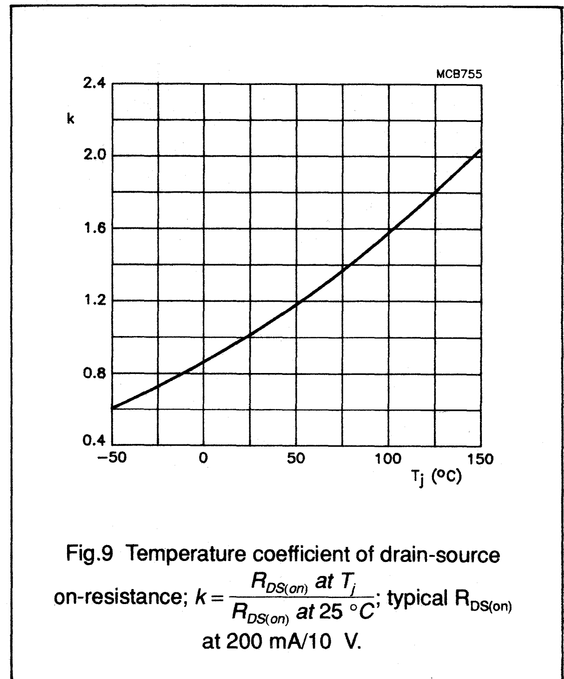


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at 200 mA/10 V.

N-channel enhancement mode vertical D-MOS transistor

BSP106

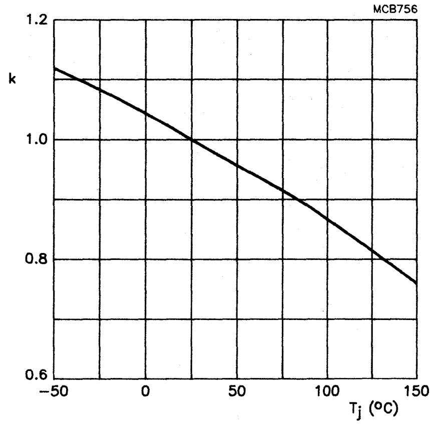
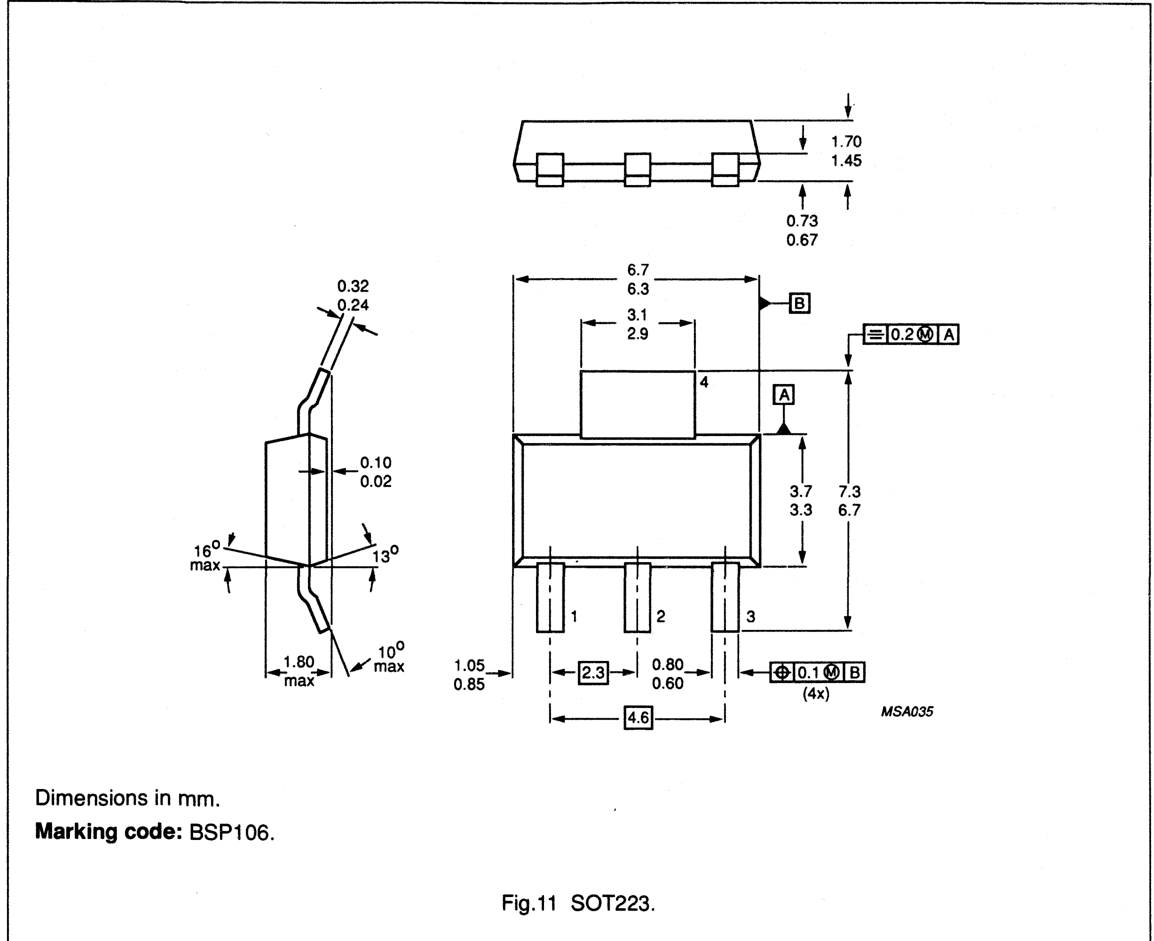


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

PACKAGE OUTLINE



Dimensions in mm.

Marking code: BSP106.

Fig.11 SOT223.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October 1990

BSP107

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer driver switching.

PIN CONFIGURATION

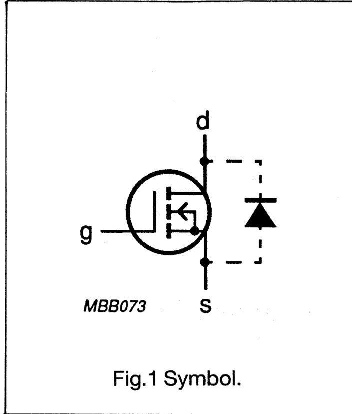


Fig.1 Symbol.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	drain current	200	mA
$R_{DS(on)}$	drain-source on-resistance	28	Ω
$V_{GS(th)}$	gate threshold voltage	2.4	V

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	200	mA
I_{DM}	drain current	peak	-	350	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Notes

1. Device mounted on an epoxy printed circuit board, 40 mm x 40 mm x 1.5 mm. Mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	-	-	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	-	-	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA $V_{DS} = V_{GS}$	0.8	-	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	-	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	-	14	-	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	-	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	5	20	ns

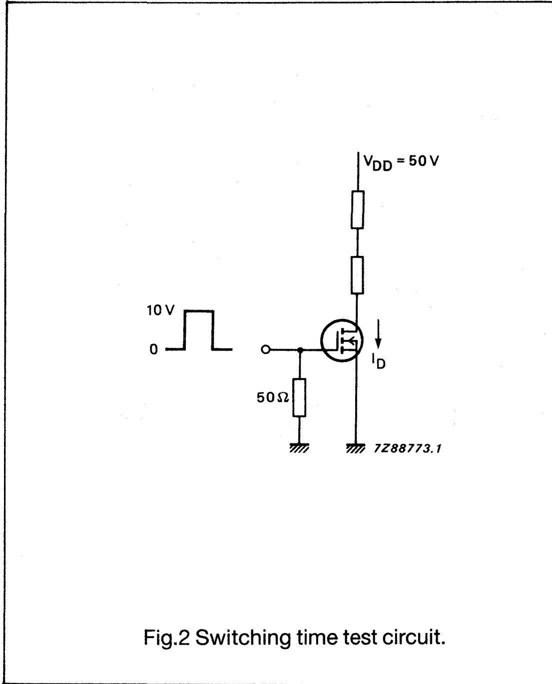


Fig.2 Switching time test circuit.

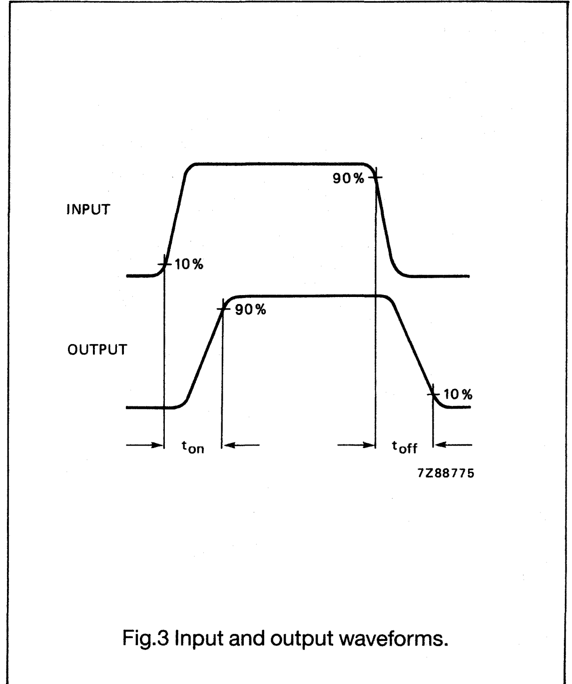


Fig.3 Input and output waveforms.

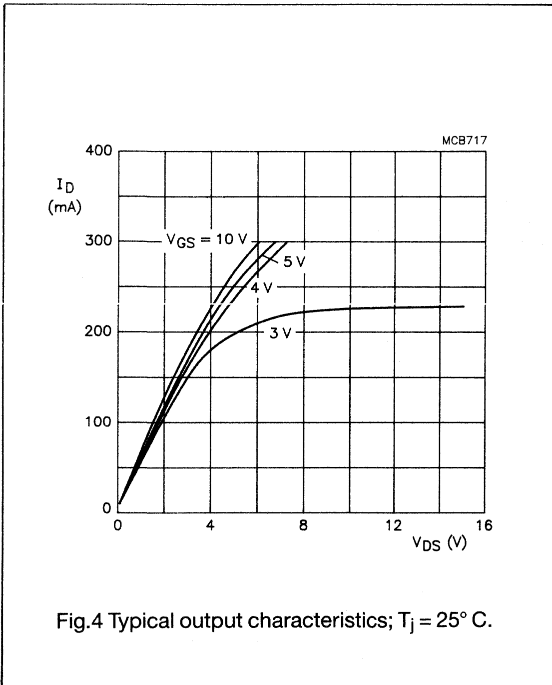


Fig.4 Typical output characteristics; T_j = 25° C.

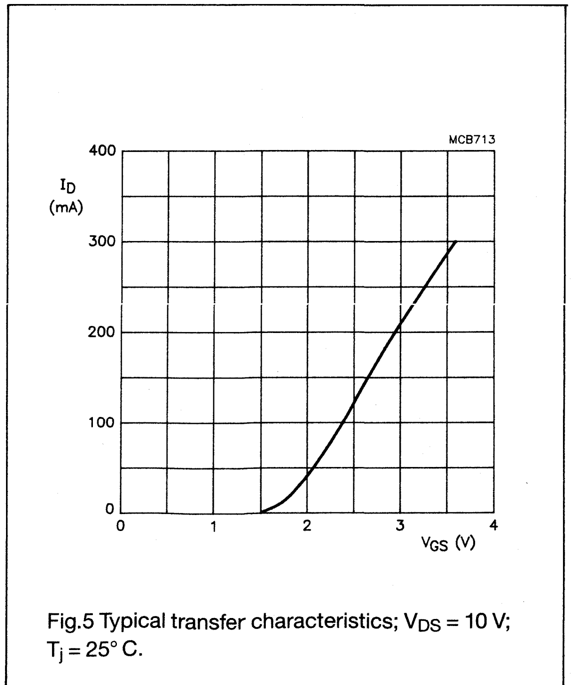


Fig.5 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25° C.

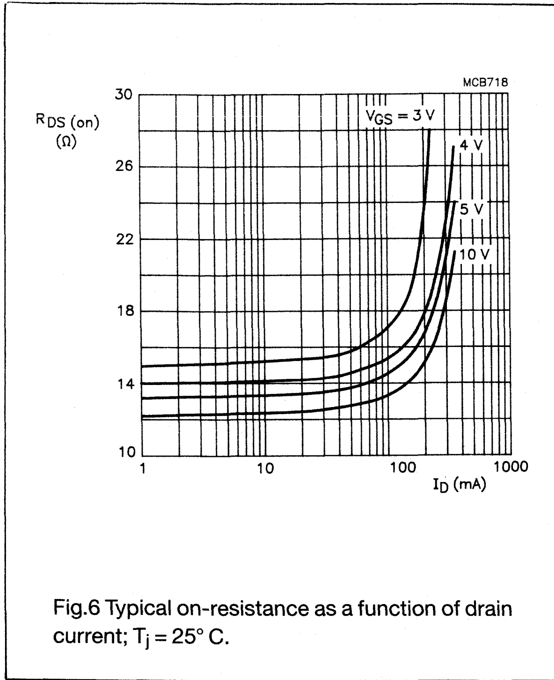


Fig.6 Typical on-resistance as a function of drain current; T_j = 25° C.

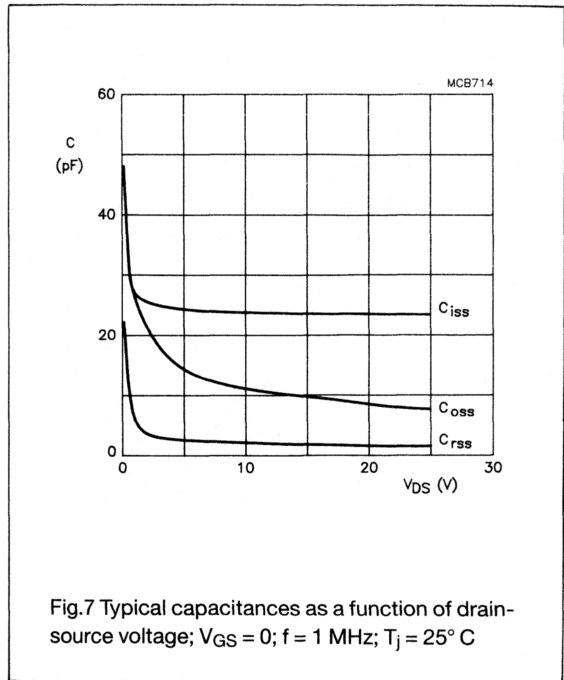


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25° C

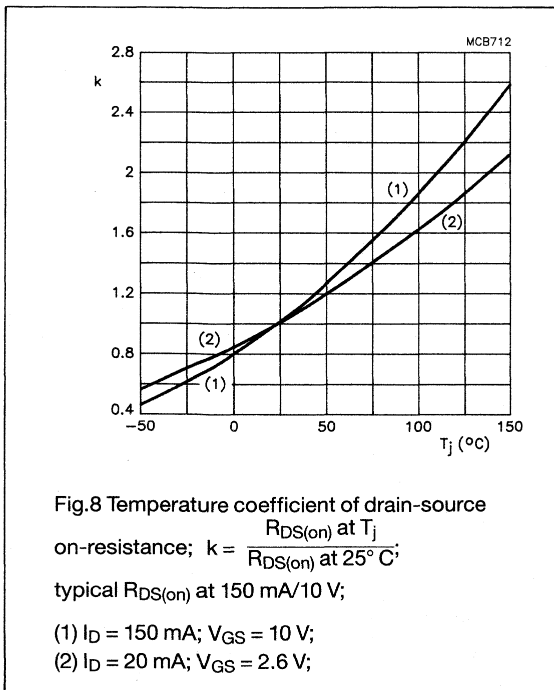


Fig.8 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25° C}$; typical $R_{DS(on)}$ at 150 mA/10 V;

(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V;

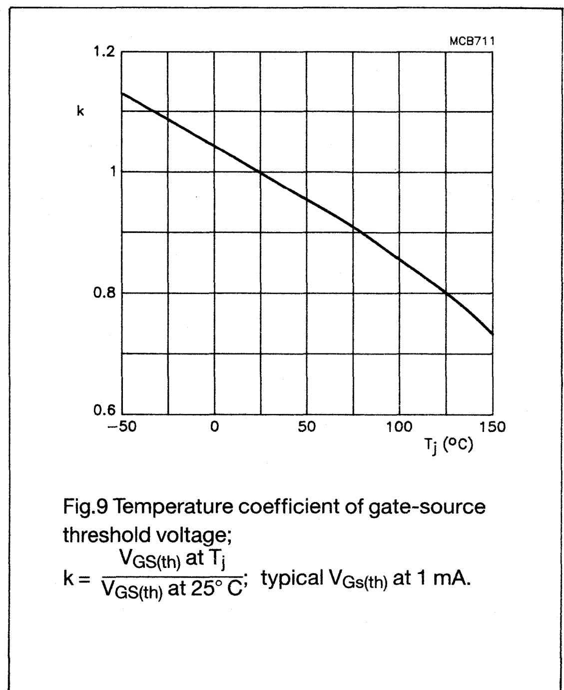


Fig.9 Temperature coefficient of gate-source threshold voltage;
$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25° C}$; typical $V_{GS(th)}$ at 1 mA.

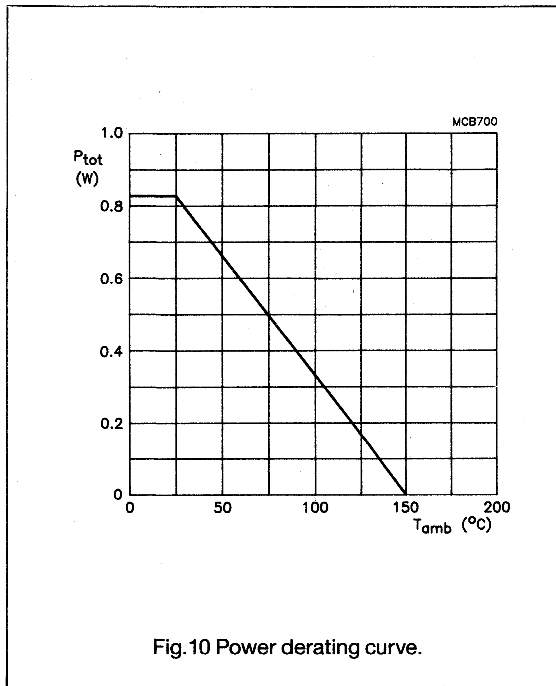


Fig.10 Power derating curve.

PACKAGE OUTLINE

Dimensions in mm

Marking code:

BSP107 = BSP107

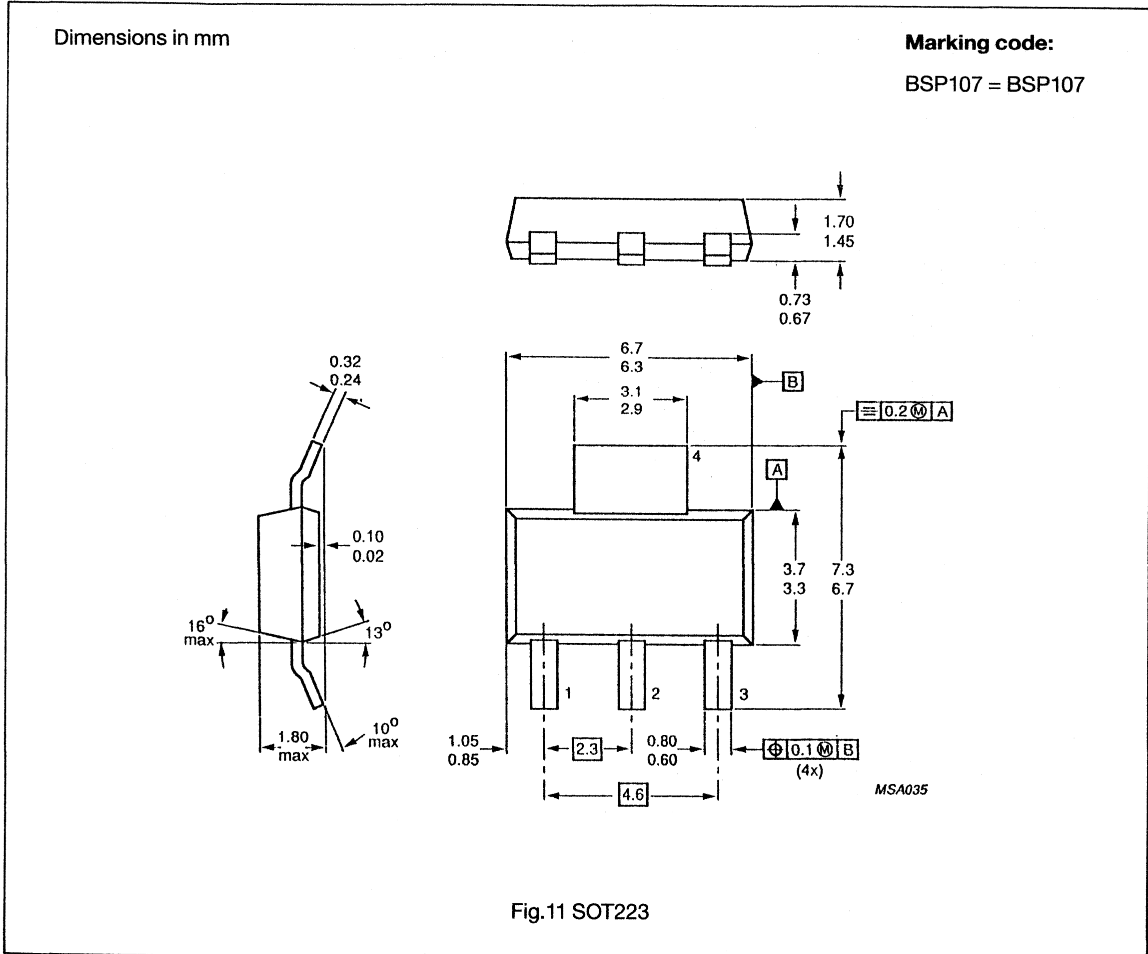


Fig.11 SOT223

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance				
I_D = 500 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ.	2.0	Ω
		max.	3.0	Ω
Transfer admittance				
I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	min.	150	mS
		typ.	300	mS

MECHANICAL DATA

Dimensions in mm

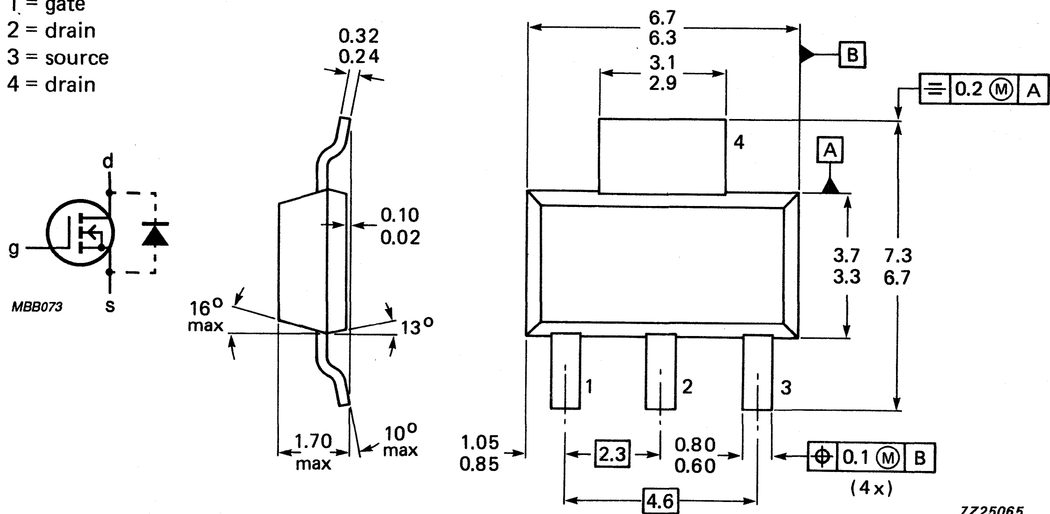
Fig.1 SOT223.

Marking code

BSP108

Pinning

1 = gate
2 = drain
3 = source
4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	500	mA
Drain current (peak)	I_{DM}	max.	1.0	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	$R_{DS\ on}$	typ. max.	2.0 3.0	Ω Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs}\rvert$	min. typ.	150 300	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 60	pF pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 8	ns ns
	t_{off}	typ. max.	10 15	ns ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

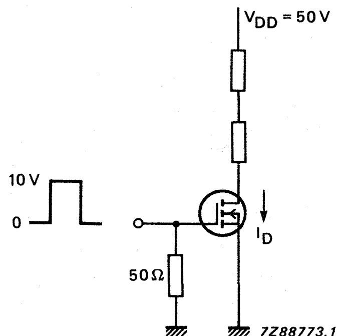


Fig.2 Switching times test circuit.

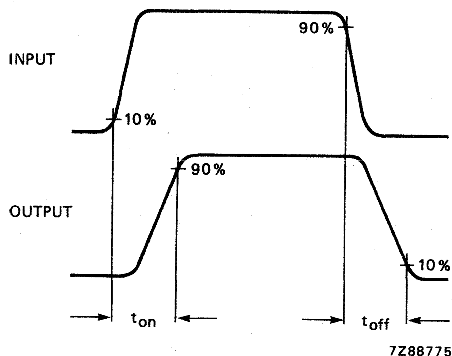


Fig.3 Input and output waveforms.

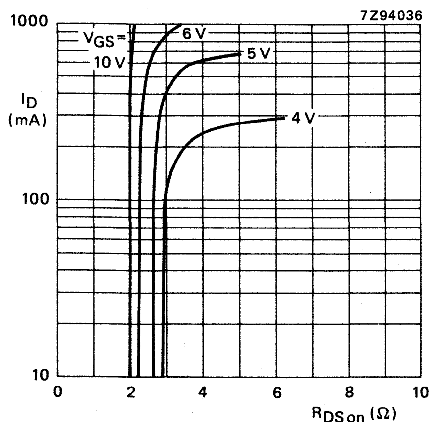


Fig.4 T_j = 25 °C; typical values.

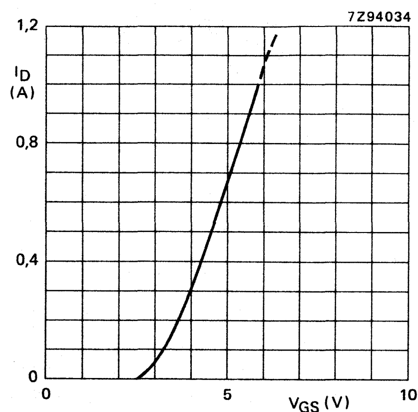


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

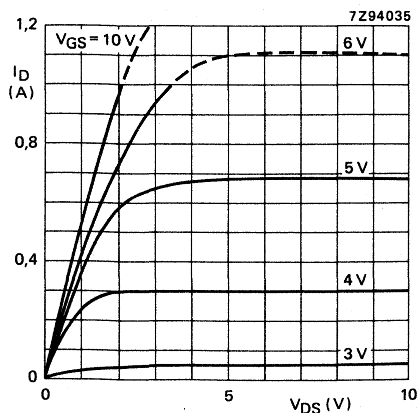


Fig.6 T_j = 25 °C; typical values.

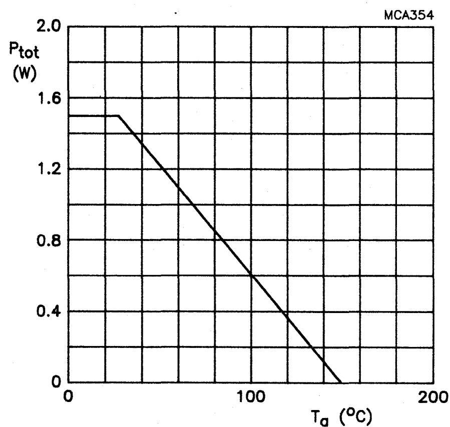


Fig.7 Power derating curve.

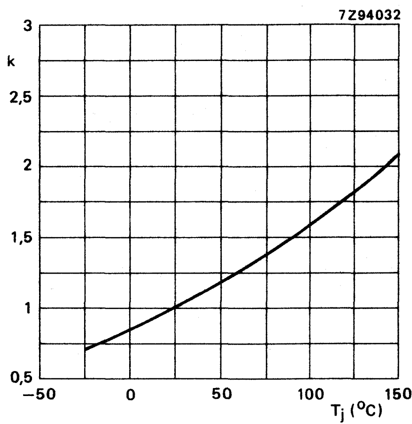


Fig.8 $k = \frac{R_{DS\,on} \text{ at } T_j}{R_{DS\,on} \text{ at } 25\ ^{o}C}$; typ. values at 500 mA/10 V.

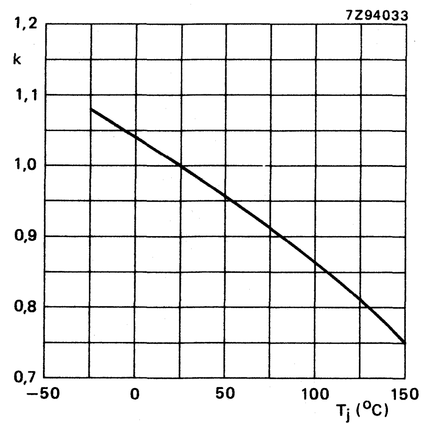


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

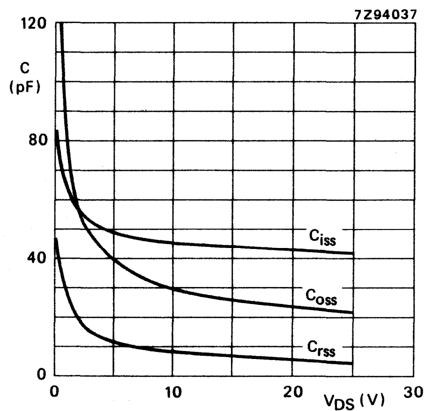


Fig.10 $T_j = 25\ ^{o}C$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance $I_D = 200$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	4.5	Ω
		max.	7	Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 15$ V	$\lvert Y_{fs} \rvert$	min.	75	mS
		typ.	150	mS

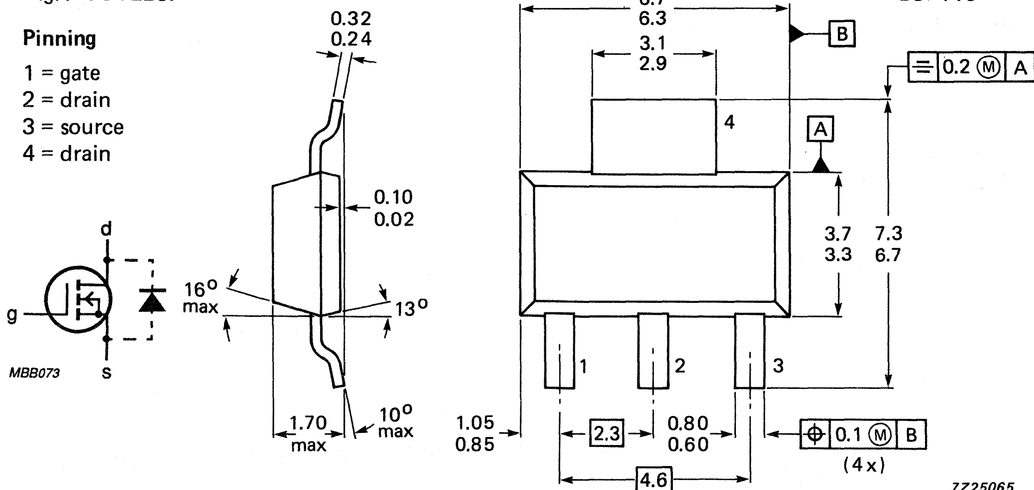
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT223.

Marking code

BSP110



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Drain current (peak)	I_{DM}	max.	650	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source ON-resistance (see Fig.4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ.	7	Ω
		max.	10	Ω
I_D = 200 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5	Ω
		max.	7	Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	min.	75	mS
		typ.	150	mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	15	pF
		max.	30	pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	13	pF
		max.	20	pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3 pF
		max.	6 pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	2 ns
		max.	5 ns
	t_{off}	typ.	5 ns
		max.	10 ns

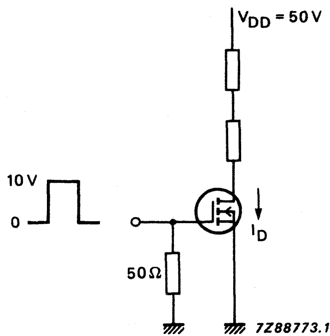


Fig.2 Switching time test circuit.

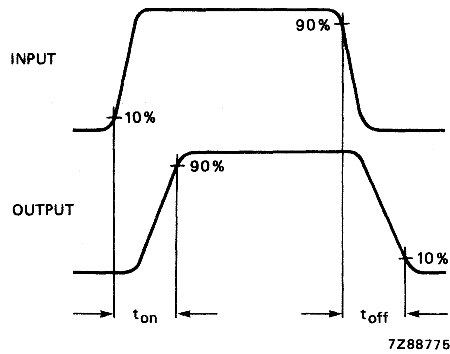


Fig.3 Input and output waveforms.

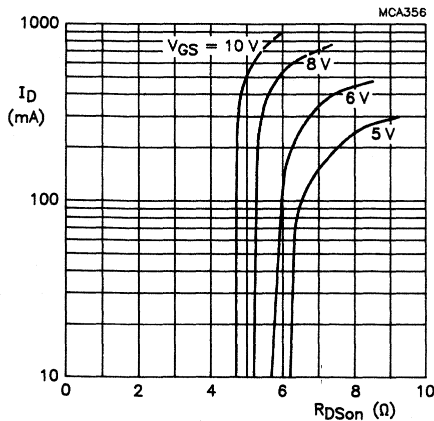


Fig.4 T_j = 25 °C; typical values.

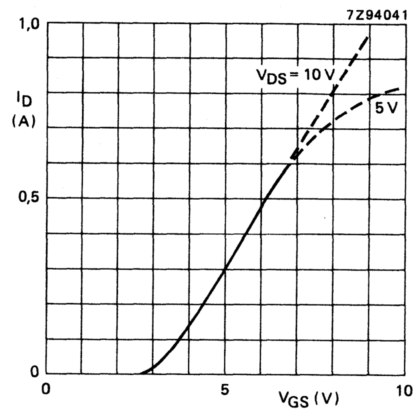


Fig.5 T_j = 25 °C; typical values.

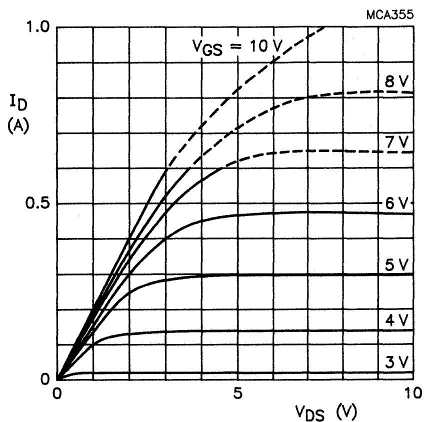


Fig.6 T_j = 25 °C; typical values.

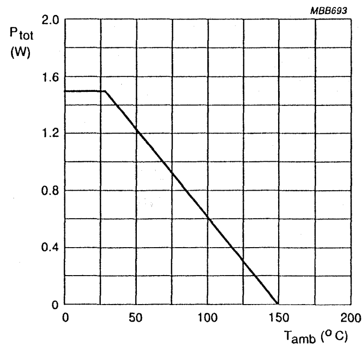


Fig.7 Power derating curve.

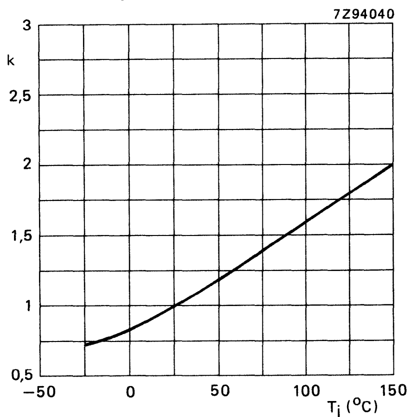


Fig.8 $k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ ^oC}$;

typical values at 150 mA/5 V.

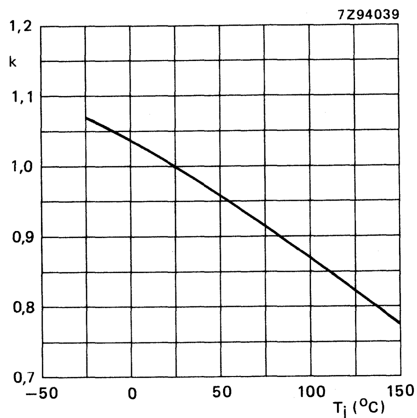


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$;

$V_{GS(th)}$ at 1 mA; typical values.

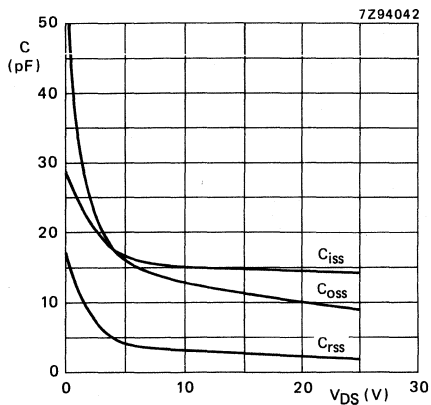


Fig.10 T_j = 25 °C; V_{GS} = 0;
f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Drain-current (DC)	I_D	max.	250 mA
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	7 Ω
		max.	12 Ω
Gate threshold voltage	$V_{GS(th)}$	max.	2.8 V

MECHANICAL DATA

Dimensions in mm

Marking code

BSP120

Fig.1 SOT223.

Pinning

1 = gate
2 = drain
3 = source
4 = drain

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Drain-source ON-resistance (see Fig.4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	7 12	Ω Ω
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	min. typ.	125 250	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 65	pF pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V;
V_{GS} = 0 to 10 V

t_{on}	typ.	3	ns
	max.	6	ns
t_{off}	typ.	15	ns
	max.	20	ns

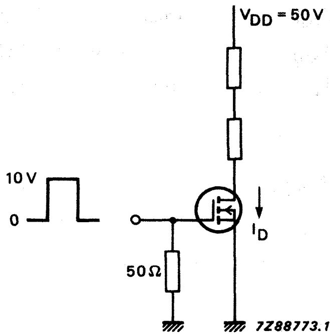


Fig.2 Switching time test circuit.

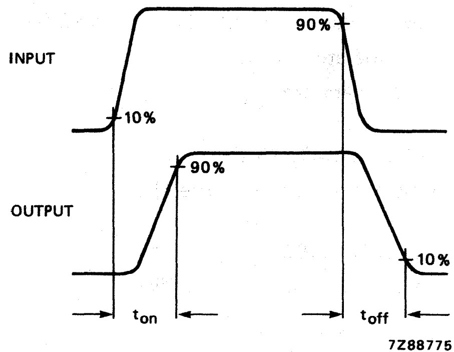


Fig.3 Input and output waveforms.

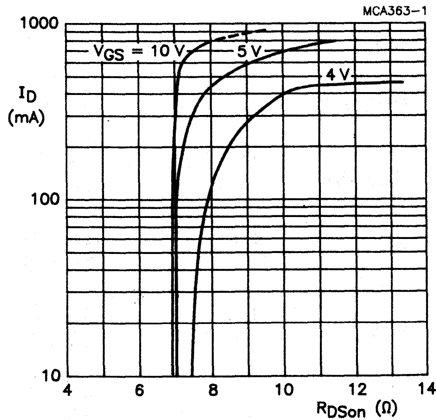


Fig.4 T_j = 25 °C; typical values.

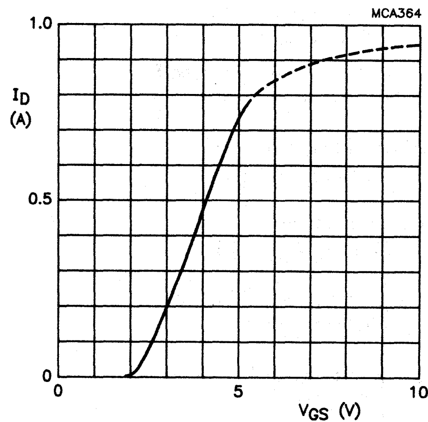


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

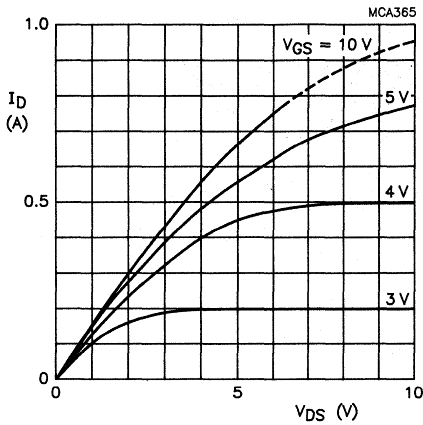


Fig.6 $T_j = 25\ ^oC$; typical values.

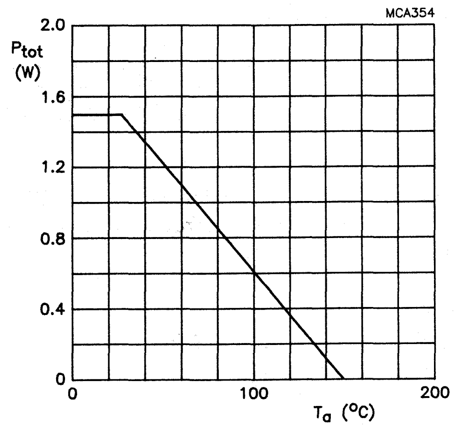


Fig.7 Power derating curve.

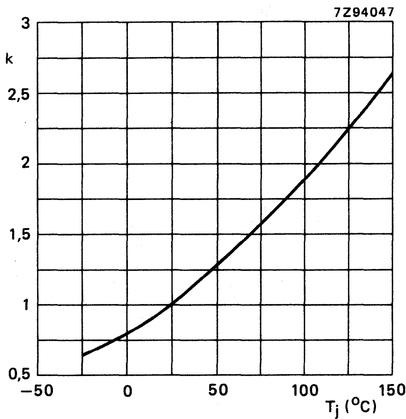


Fig.8 $k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ ^oC}$; at 250 mA/10 V; typical values.

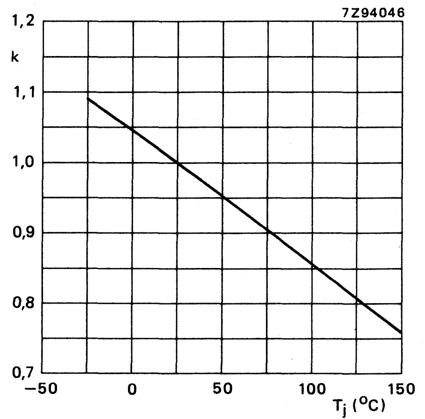


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

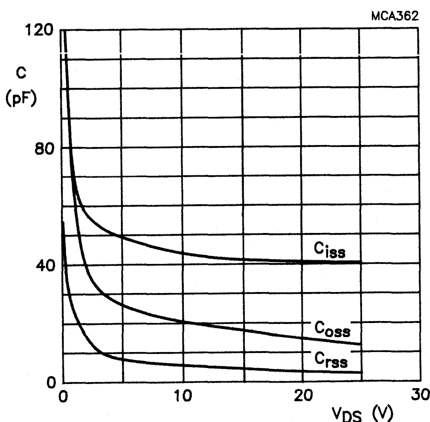


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1.5	W
Drain-source on-resistance $I_D = 400$ mA; $V_{GS} = 10$ V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6.0	Ω
Transfer admittance $I_D = 400$ mA; $V_{DS} = 25$ V	$\lvert Y_{fs}\rvert$	min.	200	mS
		typ.	350	mS

MECHANICAL DATA

Dimensions in mm

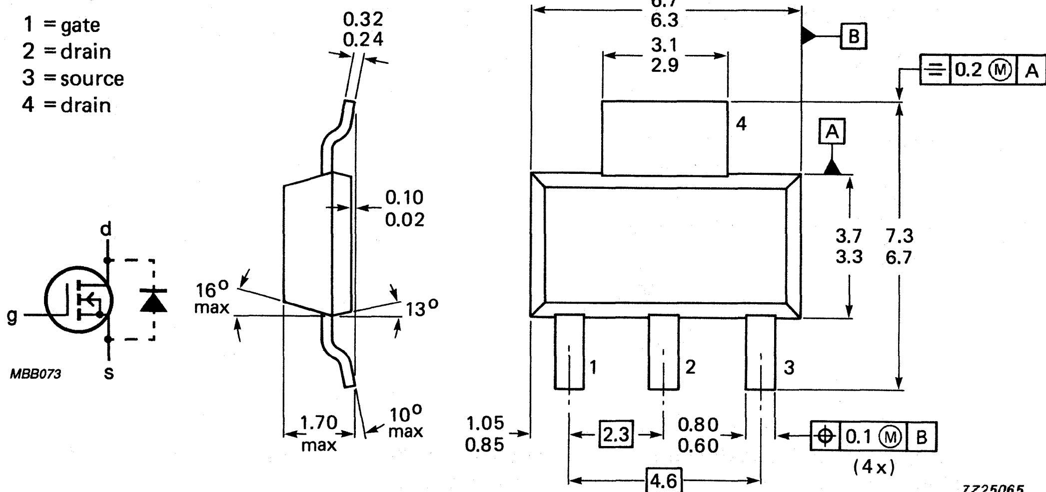
Fig.1 SOT223.

Marking code

BSP121

Pinning:

1 = gate
2 = drain
3 = source
4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

Parameter	Symbol		Value
From junction to ambient (note 1)	$R_{th j-a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V

t_{on}	typ.	5	ns
	max.	10	ns
t_{off}	typ.	15	ns
	max.	20	ns

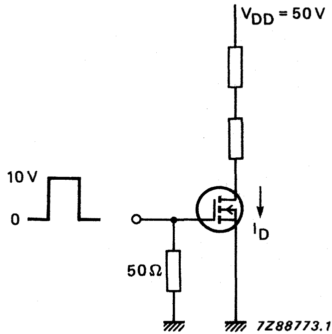


Fig.2 Switching time test circuit

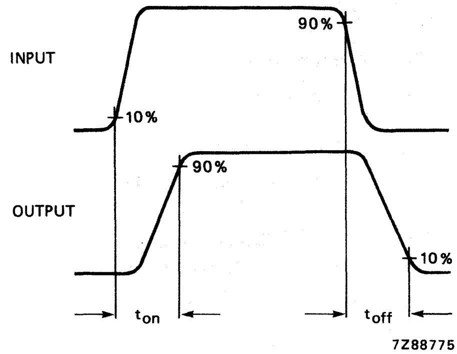


Fig.3 Input and output waveforms.

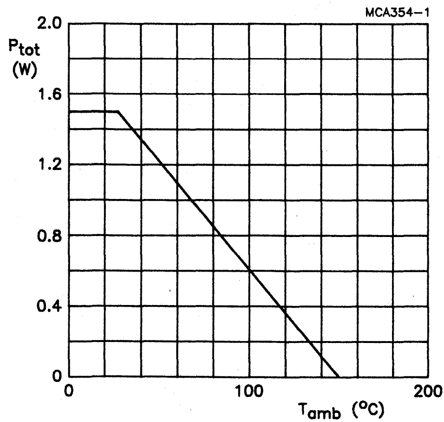


Fig.4 Power derating curve.

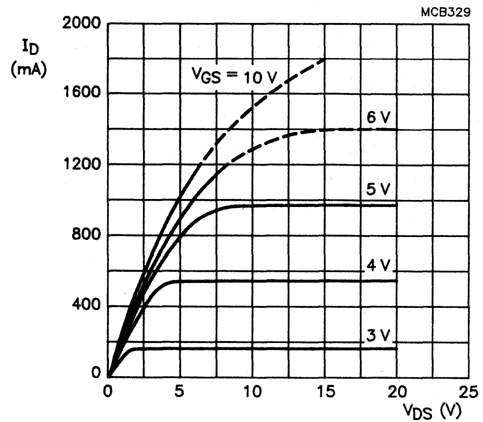


Fig.5 Output characteristic; T_j = 25 °C; typical value.

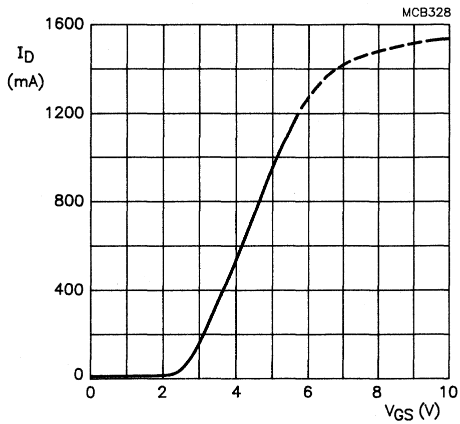


Fig.6 Transfer characteristic;
V_{DS} = 10 V; T_j = 25 °C; typical values.

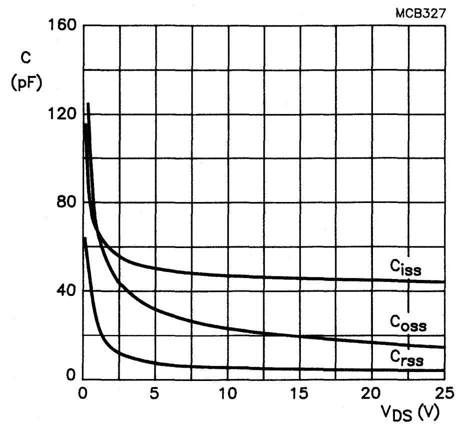


Fig.7 Capacitance as a function of drain-source voltage; V_{GS} = 0;
f = 1 MHz; T_j = 25 °C; typical values.

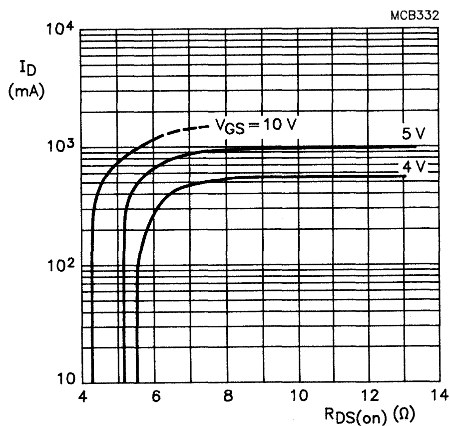


Fig.8 T_j = 25 °C; typical values.

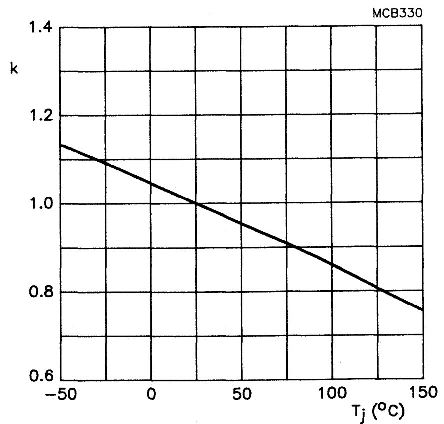


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

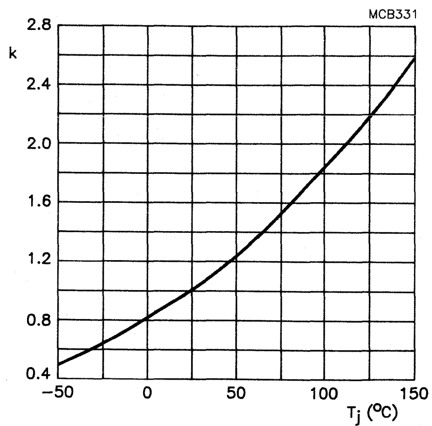


Fig.10 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^oC}$; at 400 mA/10V; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP122

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	550	mA
$R_{DS(on)}$	drain-source on-resistance	2.5	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

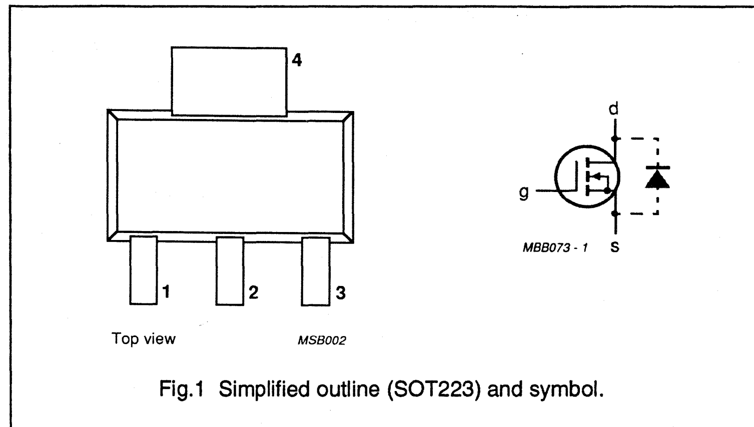


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	550	mA
I_{DM}	peak drain current		–	3	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient (note 1)	83.3 K/W

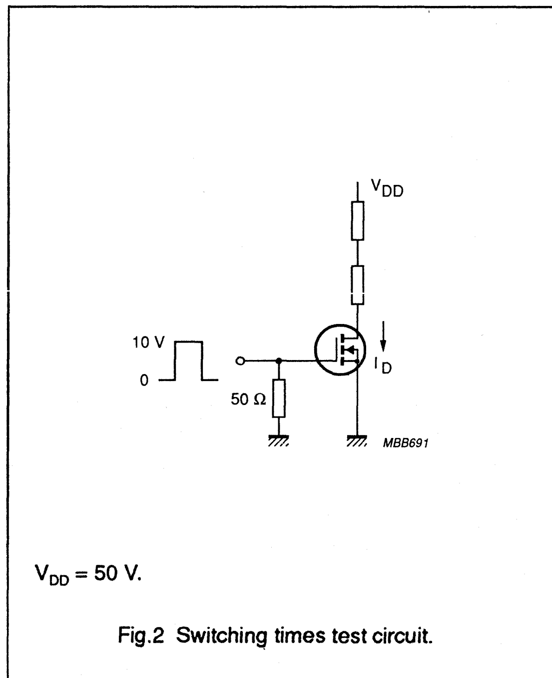
Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	1.6	2.5	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	2.5	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 750 mA; V_{DS} = 25 V	400	800	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	165	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	40	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	9	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	35	ns
t_{off}	turn-off time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	50	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

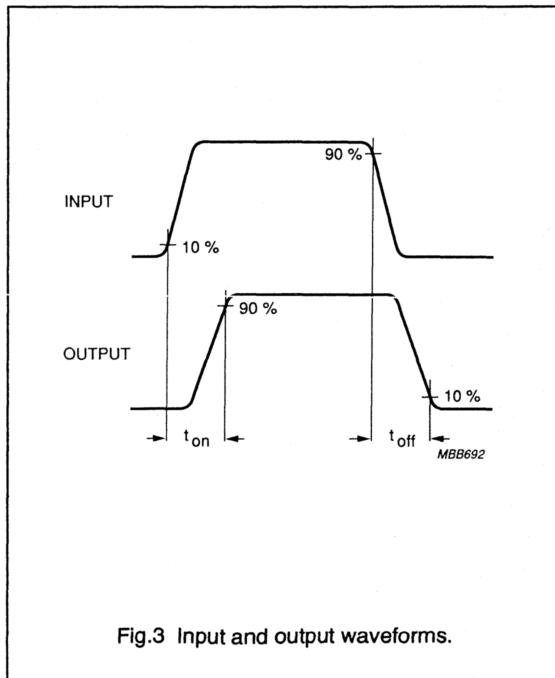


Fig.3 Input and output waveforms.

N-channel depletion mode vertical D-MOS transistor

BSP124

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 µA; V_{DS} = 60 V	−1.65	−0.75	V

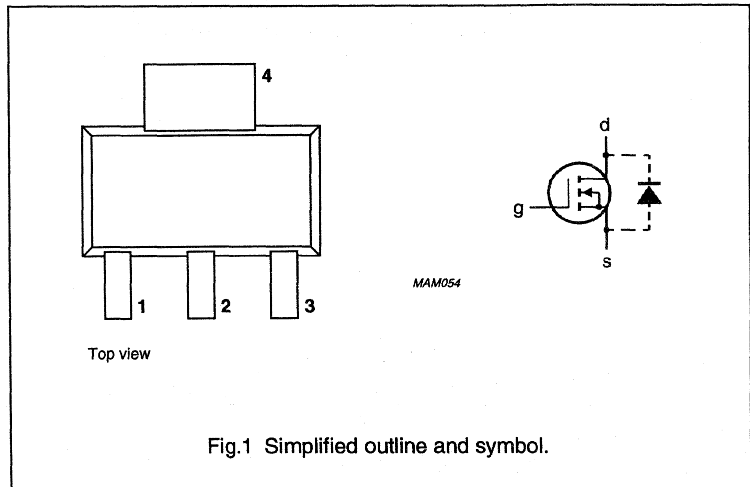


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = −3 V	250	–	V
I_{DSX}	drain-source cut-off leakage current	V_{DS} = 200 V; V_{GS} = −3 V	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	100	nA
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 µA; V_{DS} = 60 V	−1.65	−0.75	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = 3 V	−1.4	−0.6	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
		I_D = 250 mA; V_{GS} = 5 V	–	12	Ω
I_{DSS}	drain current	V_{DS} = 25 V; V_{GS} = 0	70	–	mA
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	15	pF
Switching times (see Figs 2 and 3)					
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = −3 to +5 V	–	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = +5 to −3 V	–	30	ns

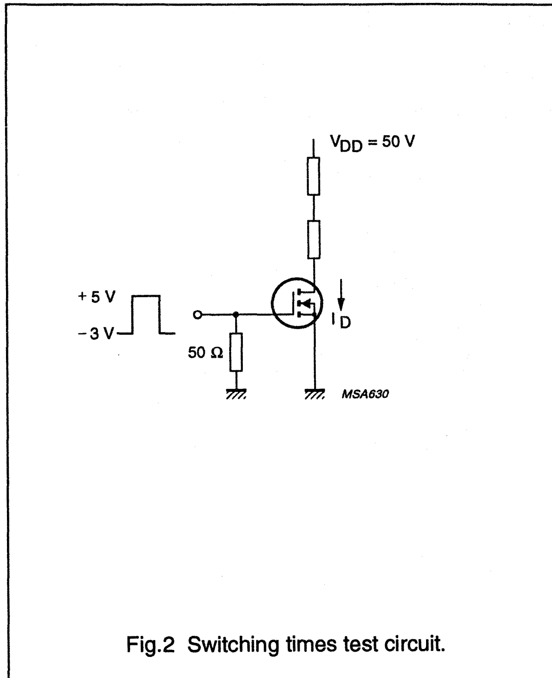


Fig.2 Switching times test circuit.

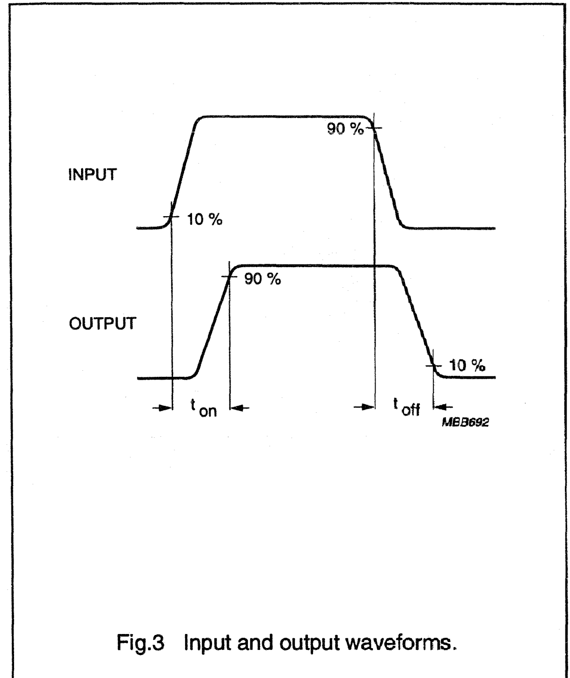


Fig.3 Input and output waveforms.

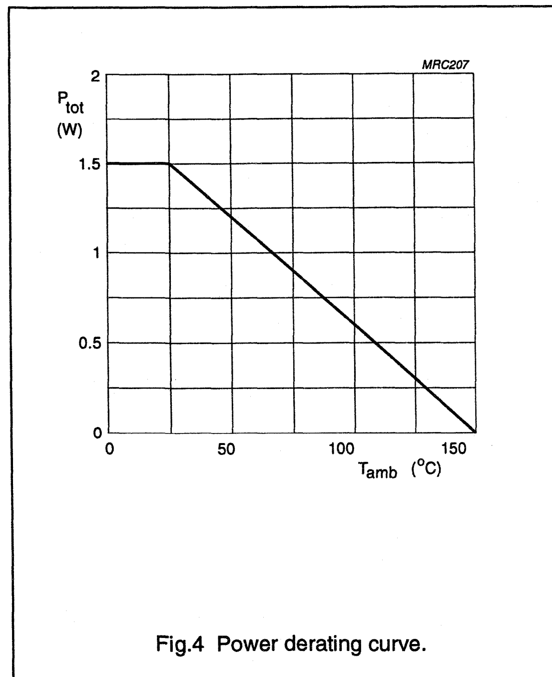
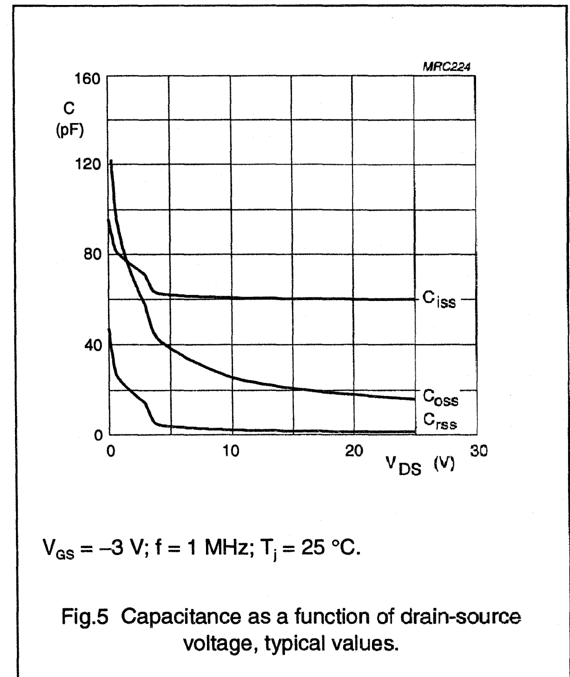
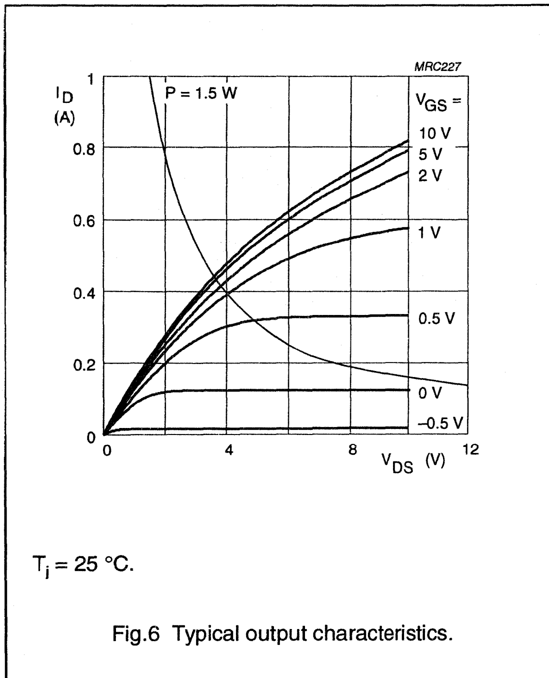


Fig.4 Power derating curve.



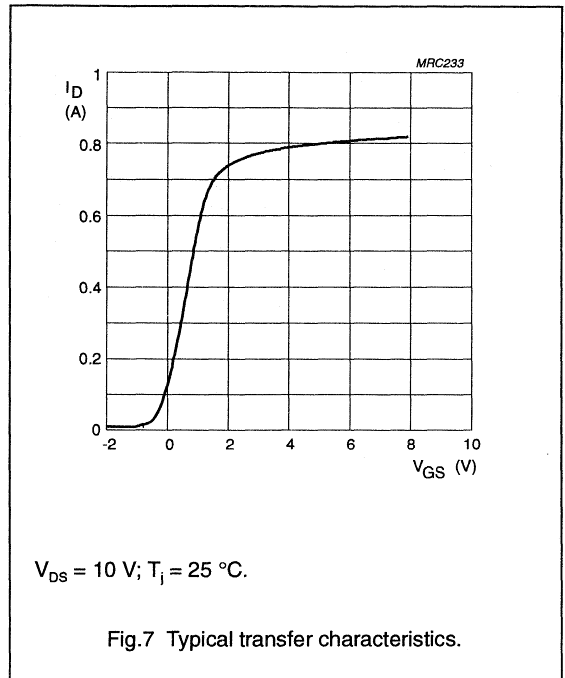
V_{GS} = −3 V; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



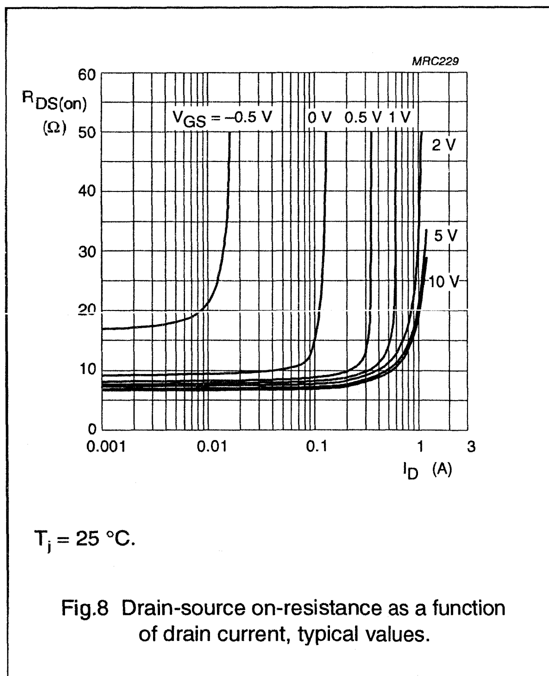
T_j = 25 °C.

Fig.6 Typical output characteristics.



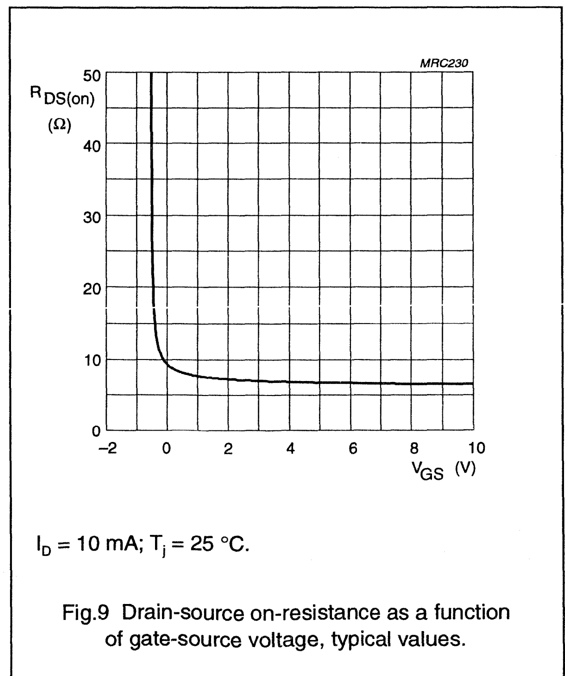
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



I_D = 10 mA; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

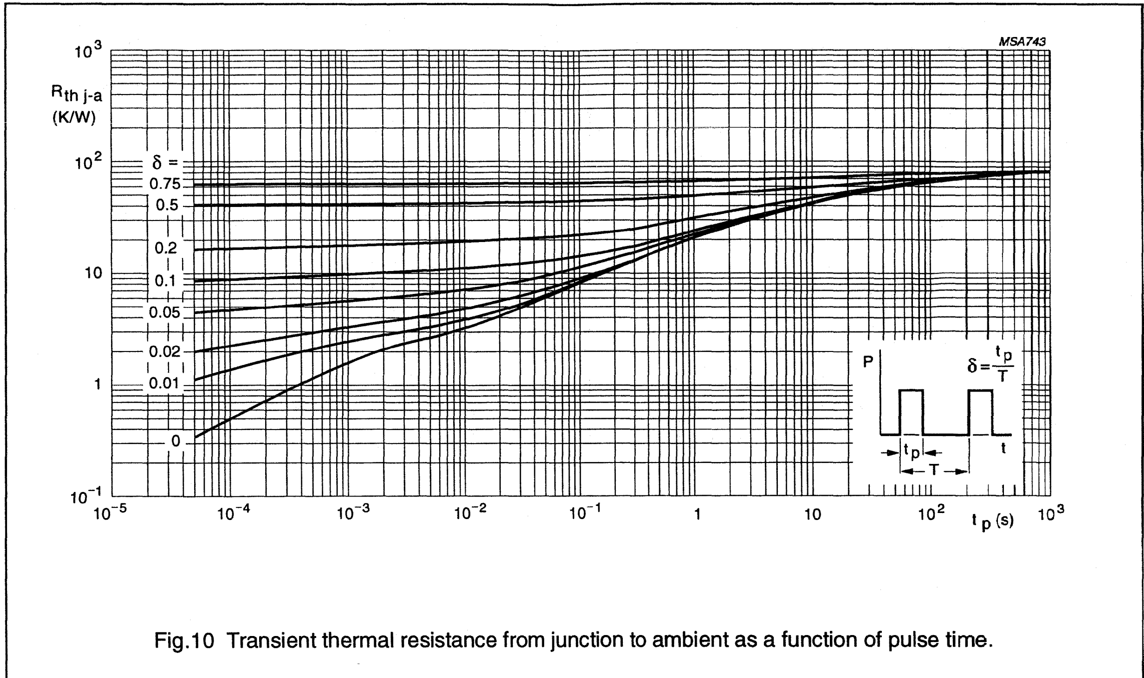
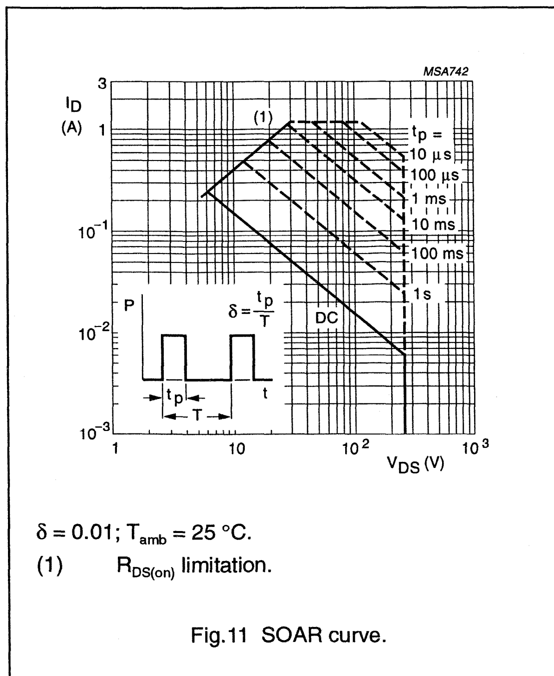


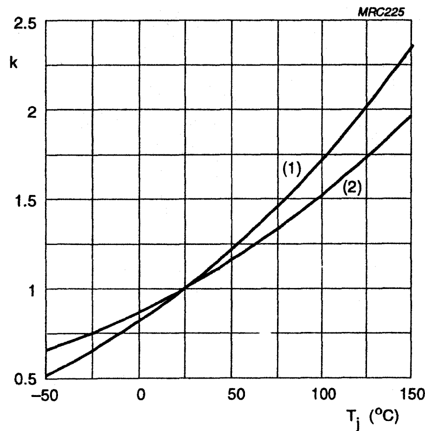
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



$\delta = 0.01$; $T_{amb} = 25$ °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



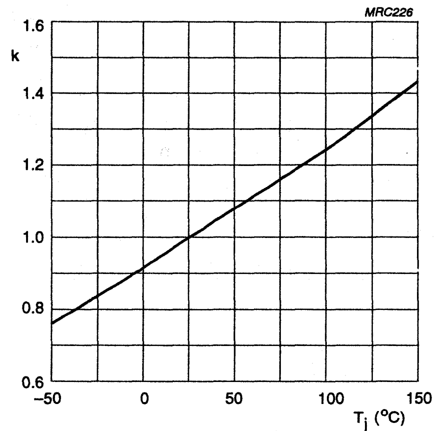
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 5 V.

(2) I_D = 20 mA; V_{GS} = 0.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}.$$

Typical $V_{GS(th)}$ at I_D = 1 mA; V_{DS} = 3 V.

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

MECHANICAL DATA

Dimensions in mm

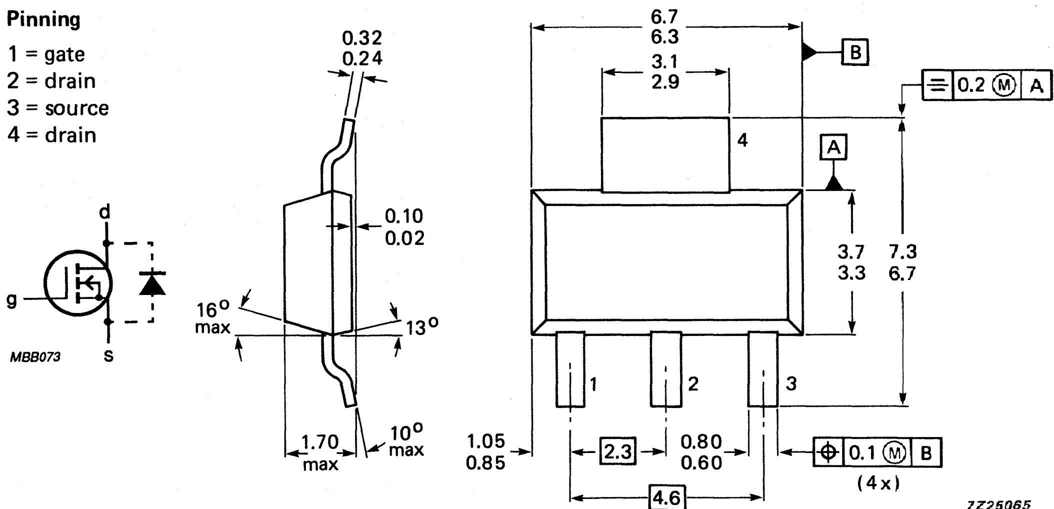
Fig.1 SOT223.

Marking code

BSP126

Pinning

1 = gate
2 = drain
3 = source
4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250	V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.0	V V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 7.0	Ω Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\|Y_{fs}\|$	min. typ.	200 400	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 90	pF pF
Output capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	5 15	pF pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V;
V_{GS} = 0 to 10 V

t_{on}	typ.	5	ns
	max.	10	ns
t_{off}	typ.	20	ns
	max.	30	ns

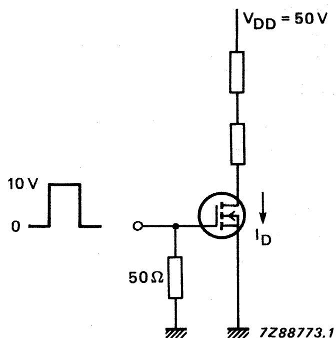


Fig.2 Switching time test circuit.

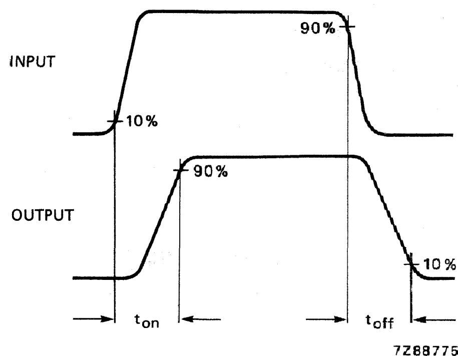


Fig.3 Input and output waveforms.

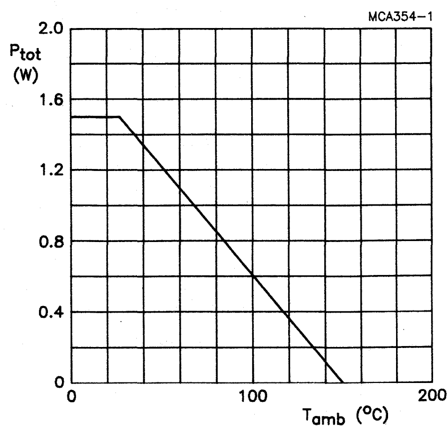


Fig.4 Power derating curve.

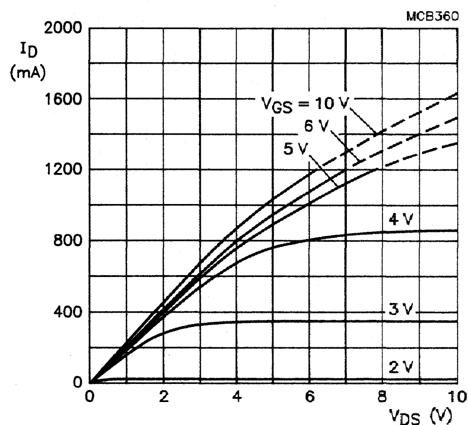


Fig.5 Output characteristics; T_j = 25 °C; typical values.

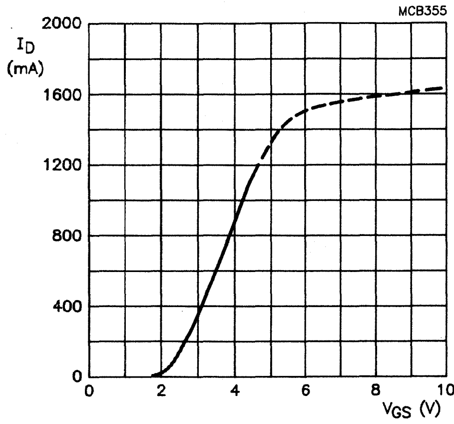


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

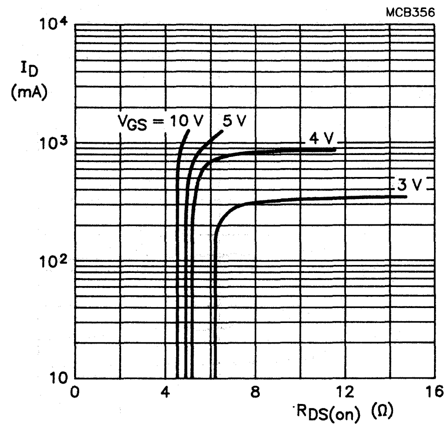


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

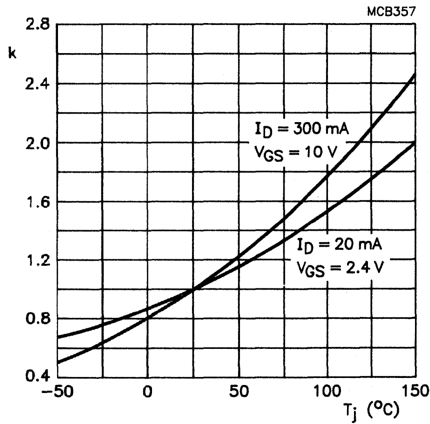


Fig.8 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^{o}C}$; typical values.

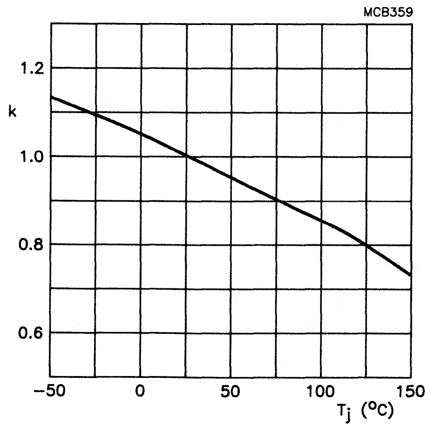


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

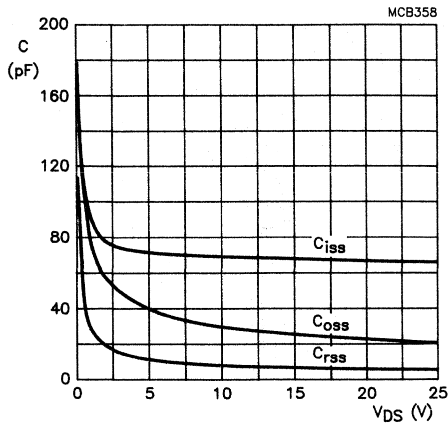


Fig.10 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP127

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
Code: BSP127	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

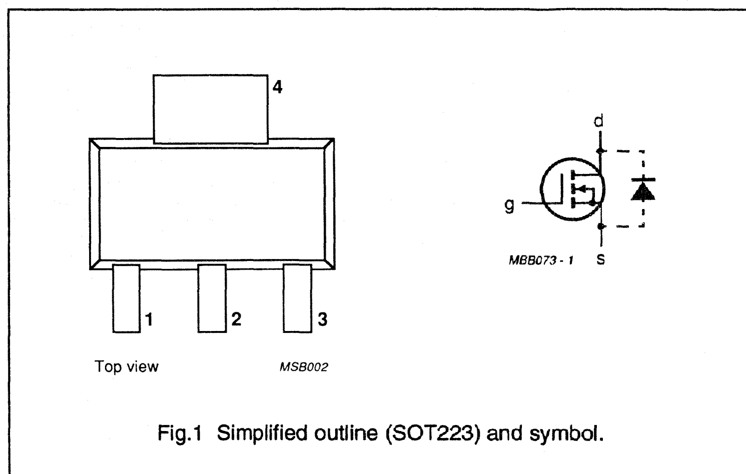


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

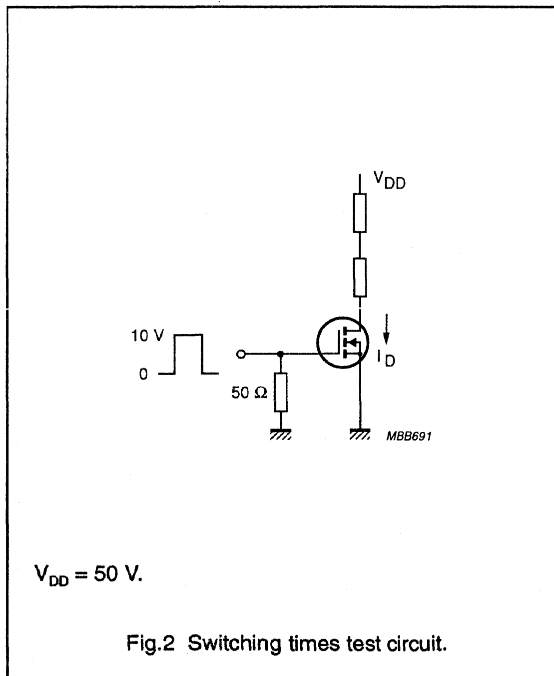
Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	270	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.5	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	9	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	55	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

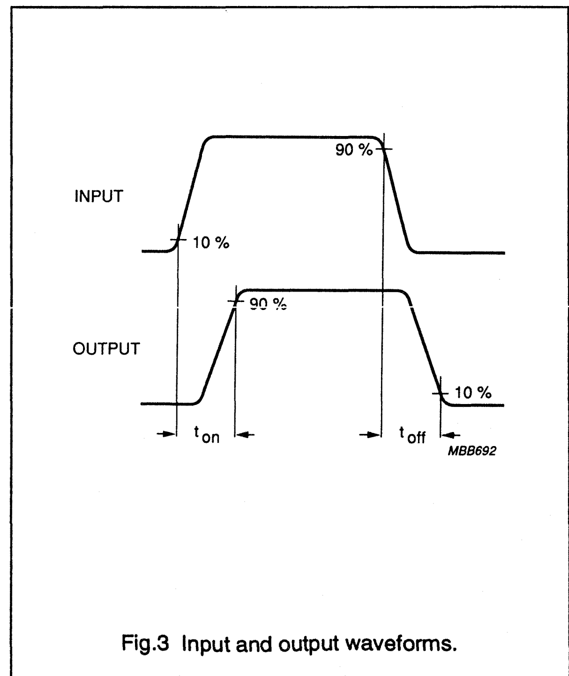


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP128

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
Code: BSP128	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

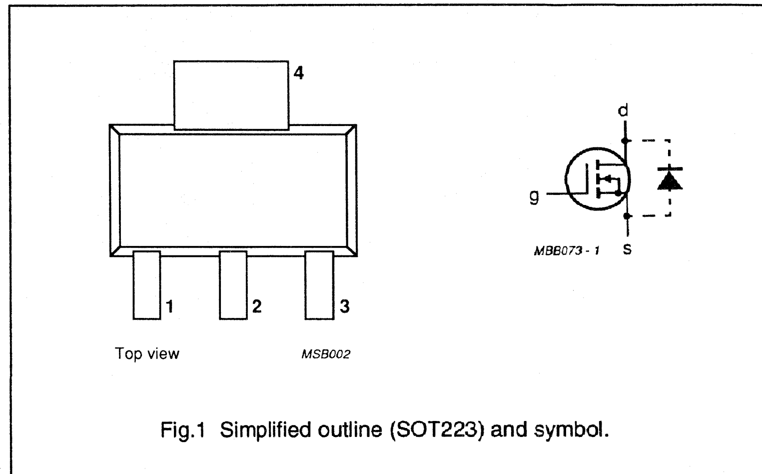


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

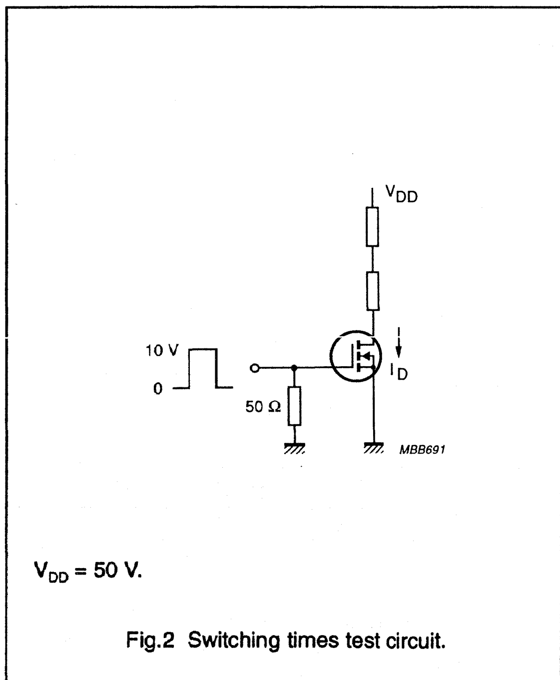
Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

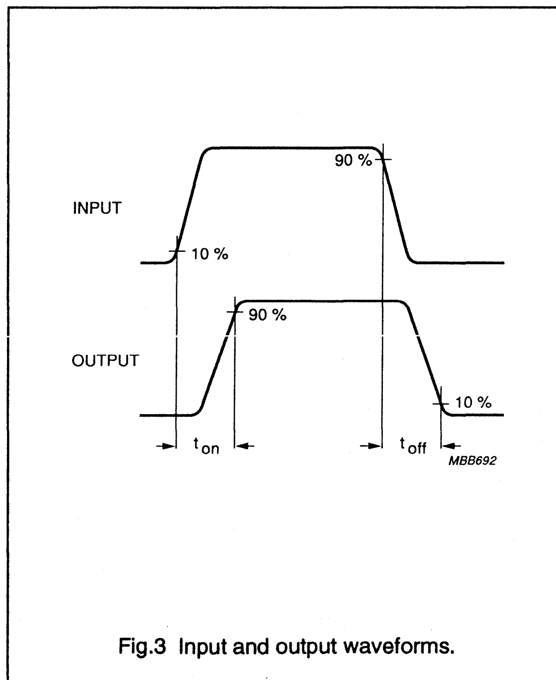


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP130

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

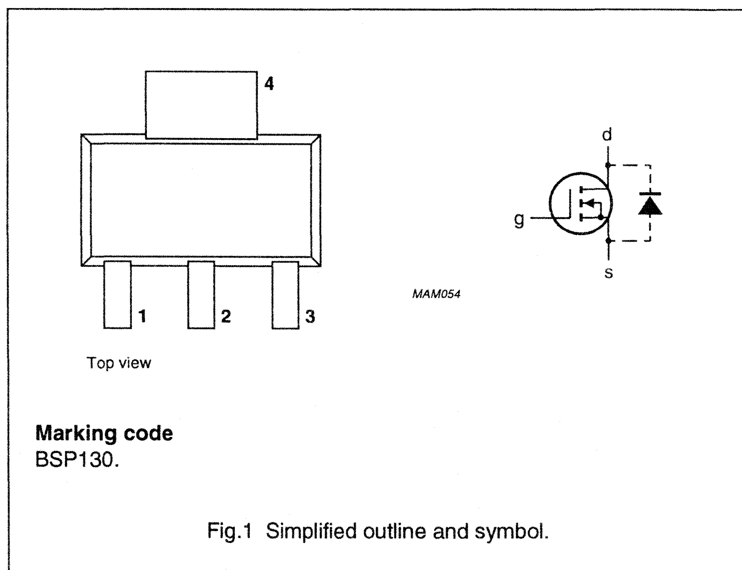
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	0.8	2	V



Marking code
BSP130.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	300	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
		I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

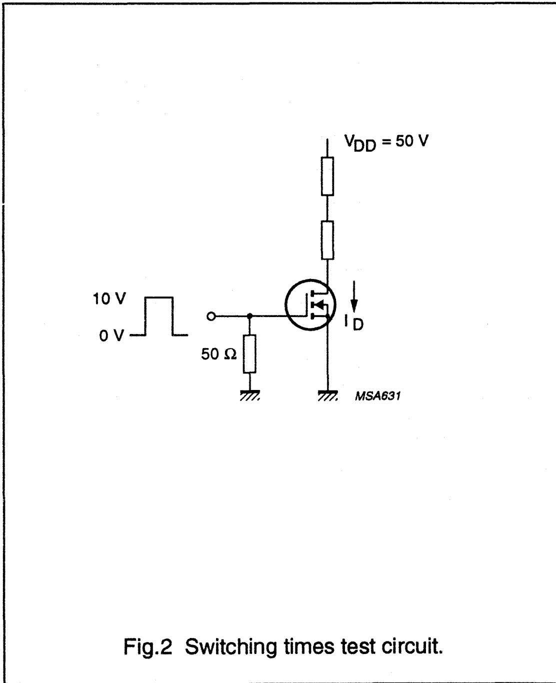


Fig.2 Switching times test circuit.

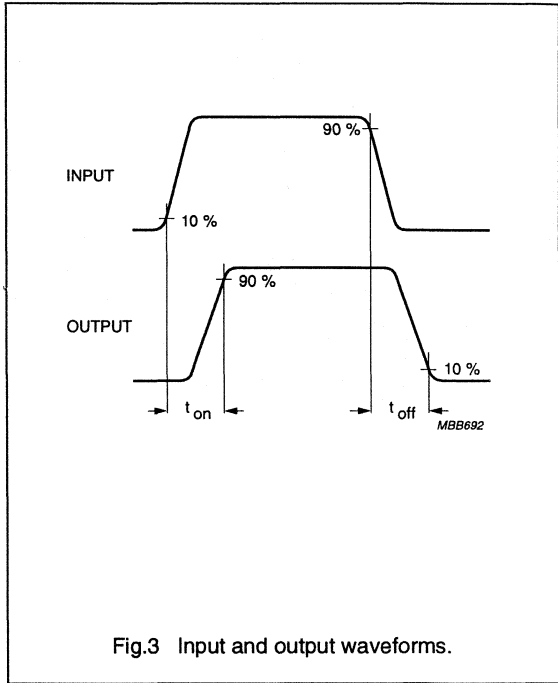


Fig.3 Input and output waveforms.

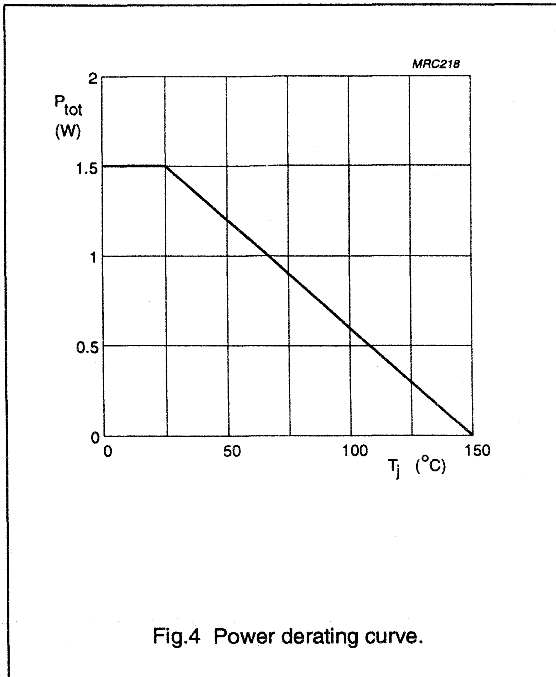
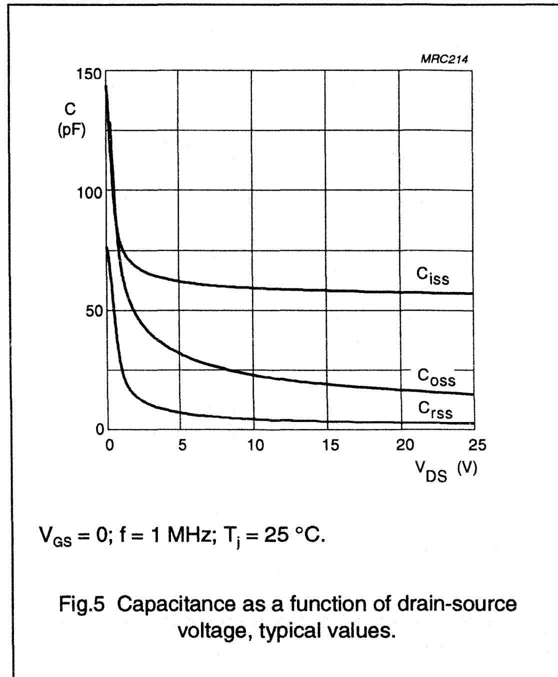
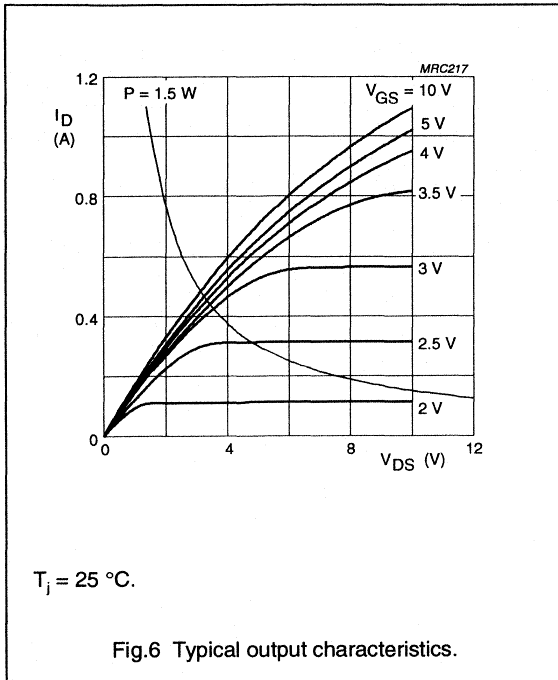


Fig.4 Power derating curve.



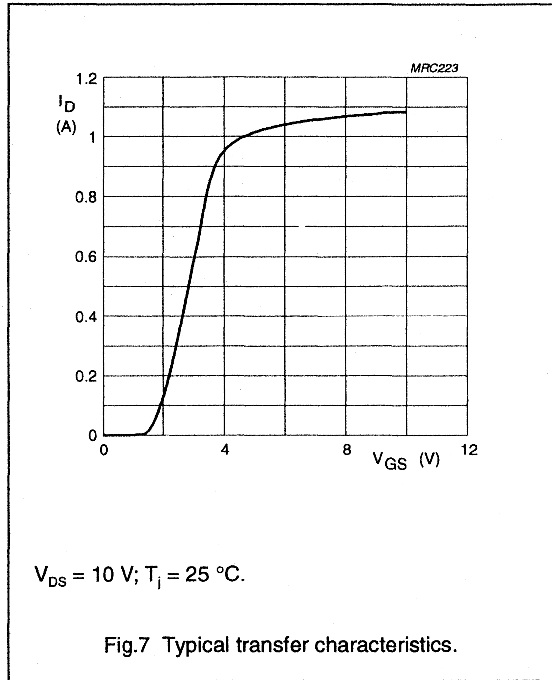
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



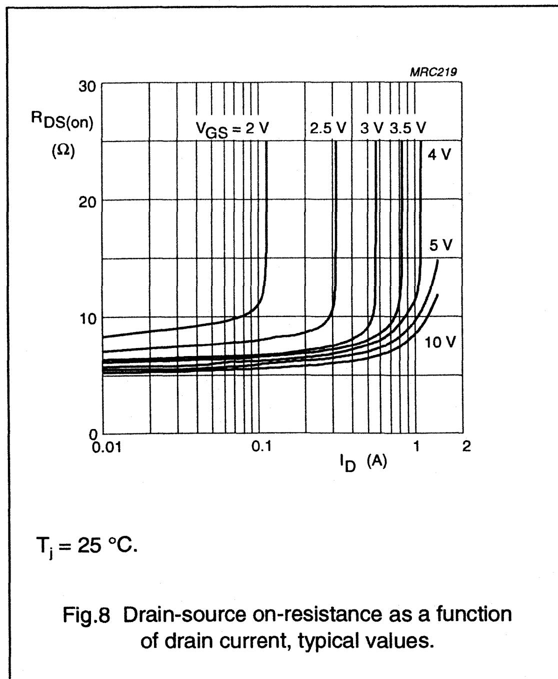
T_j = 25 °C.

Fig.6 Typical output characteristics.



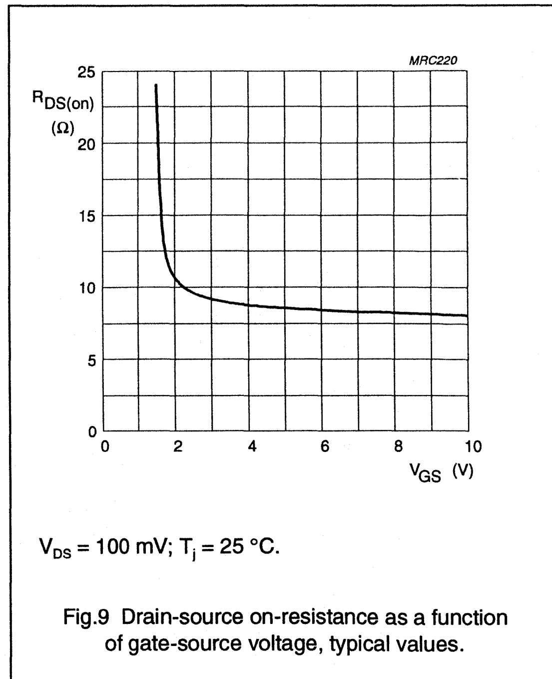
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

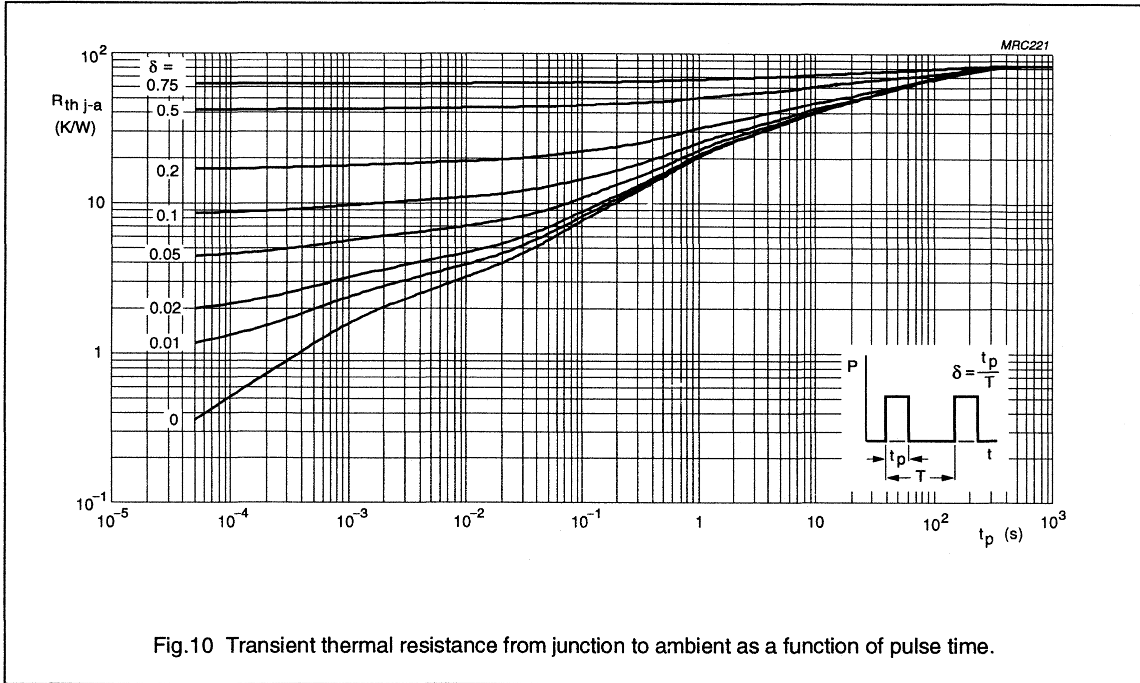
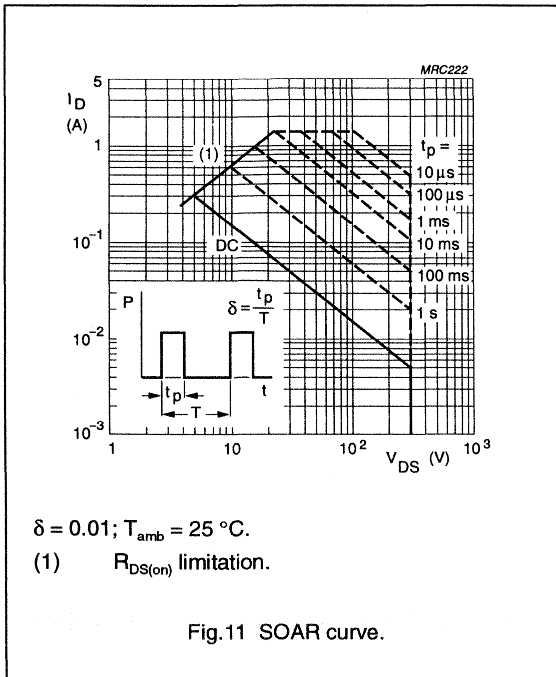


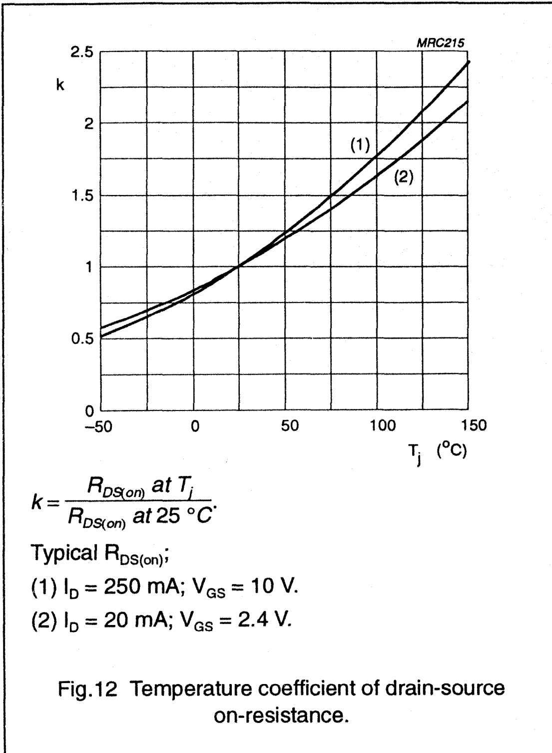
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



$\delta = 0.01$; $T_{amb} = 25$ °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



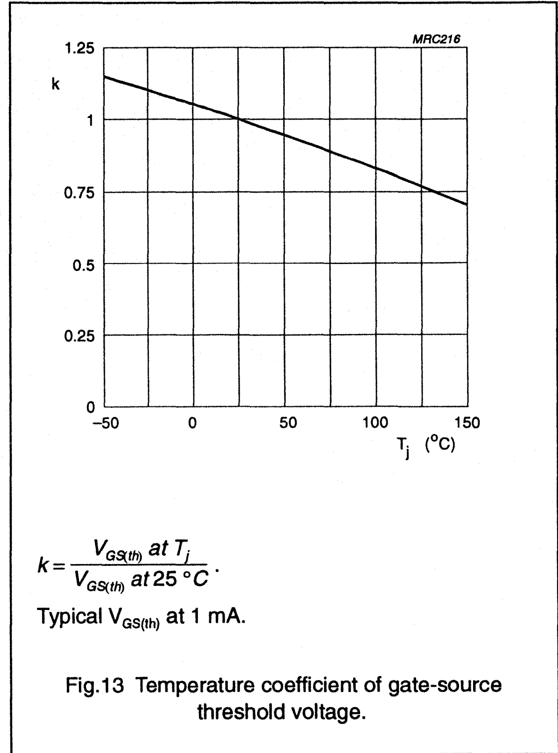
$$k = \frac{R_{DS(on)}\ at\ T_j}{R_{DS(on)}\ at\ 25\ °C}.$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 10 V.

(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)}\ at\ T_j}{V_{GS(th)}\ at\ 25\ °C}.$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSP152

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
I_D	DC drain current		–	550	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	2.5	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1.5	3.5	V

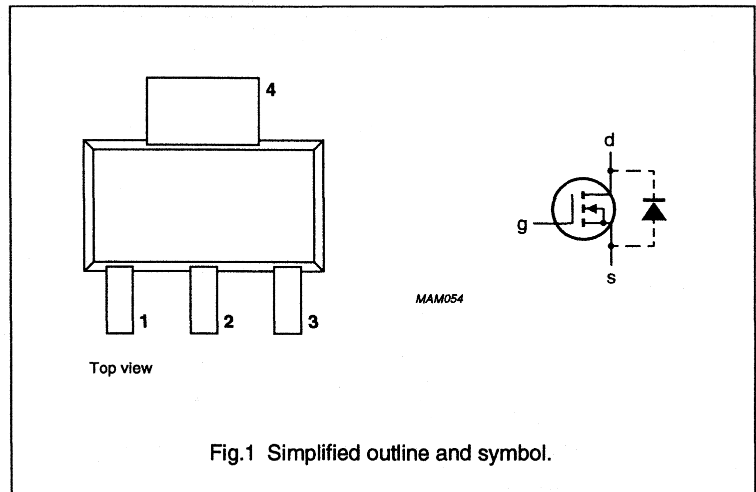


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	DC drain current		–	550	mA
I_{DM}	peak drain current		–	3	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	200	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 40 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1.5	–	3.5	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	–	2.5	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 750 mA; V_{DS} = 25 V	400	–	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	100	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	42	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	8	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	15	ns
t_{off}	turn-off time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	–	30	ns

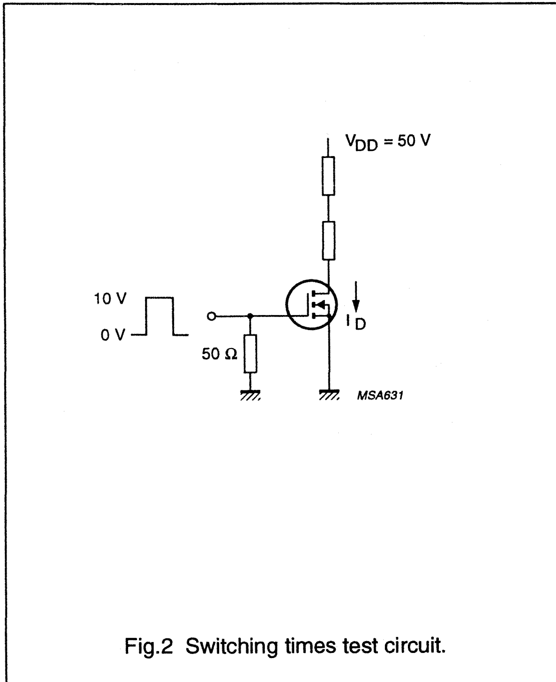


Fig.2 Switching times test circuit.

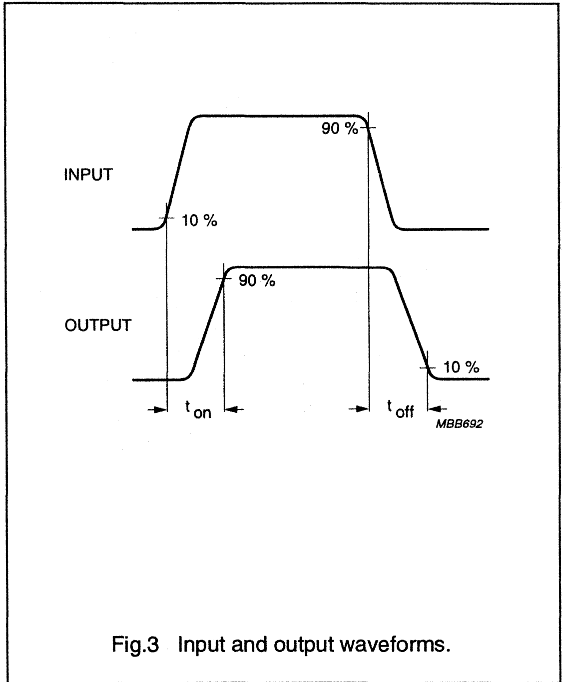


Fig.3 Input and output waveforms.

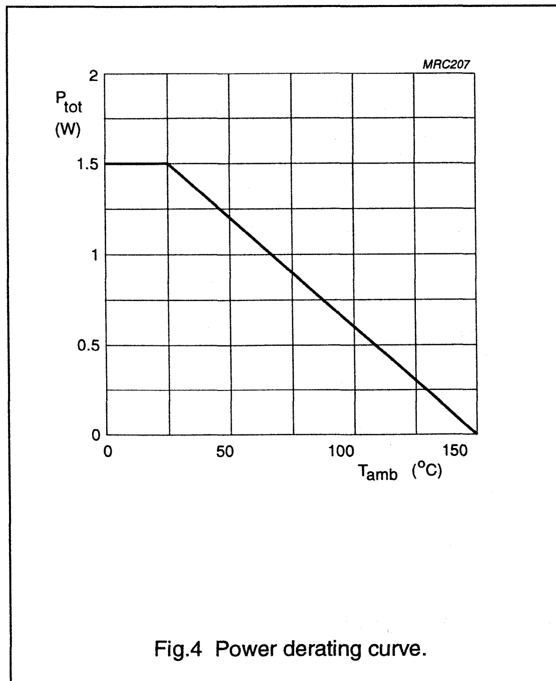
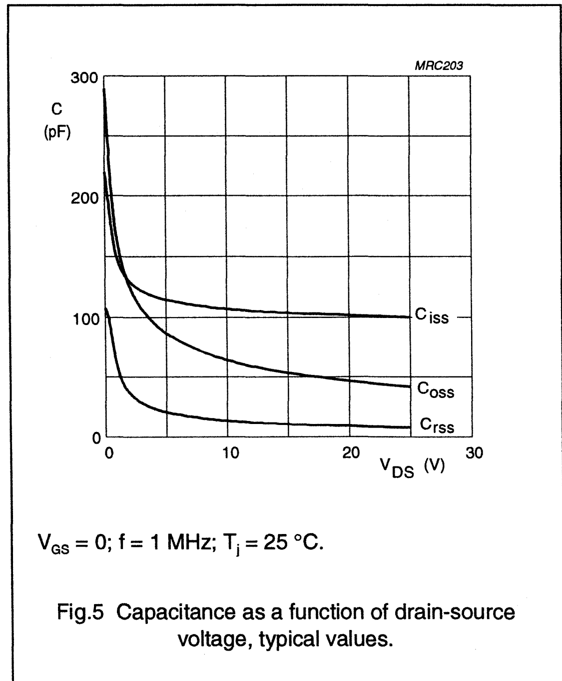
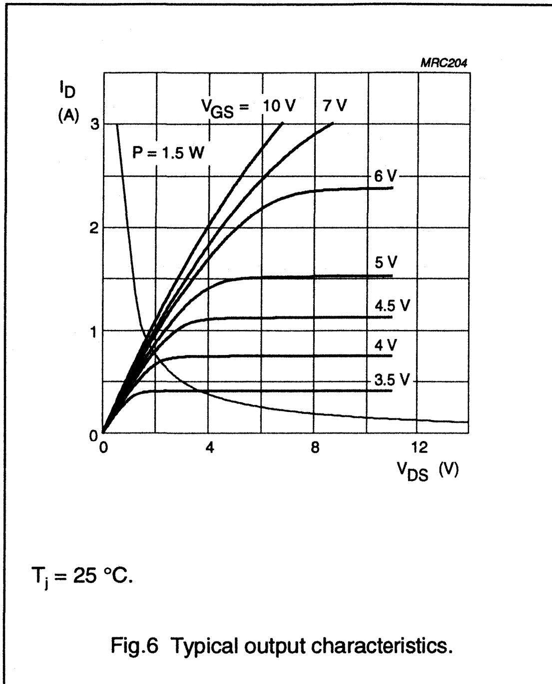


Fig.4 Power derating curve.



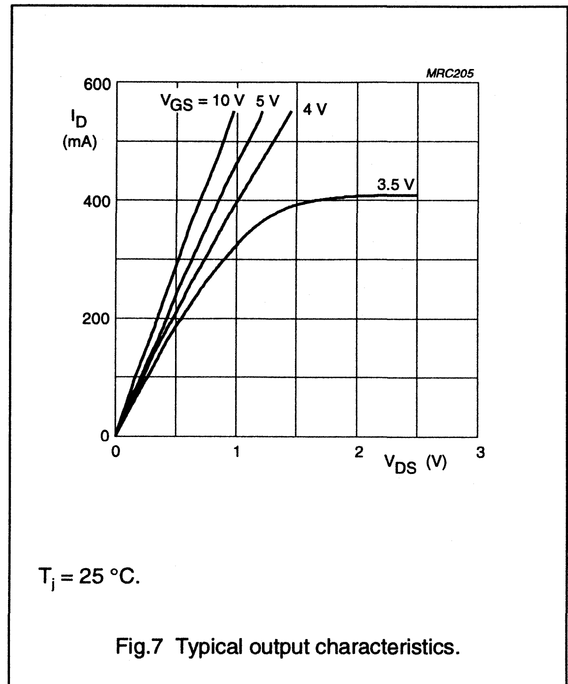
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



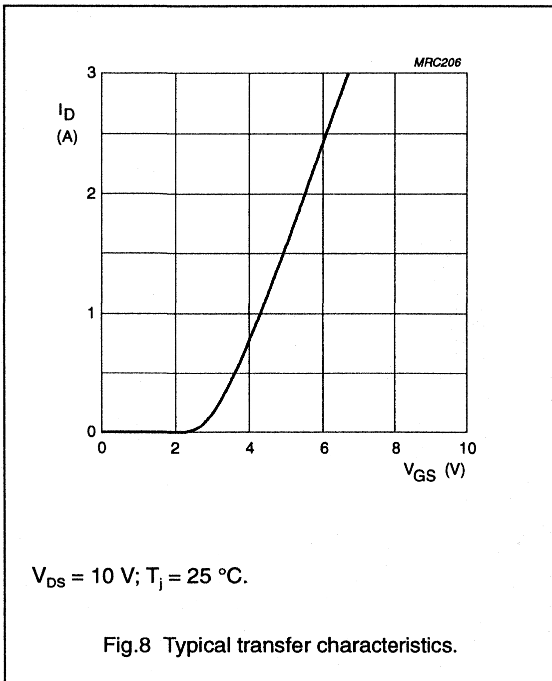
T_j = 25 °C.

Fig.6 Typical output characteristics.



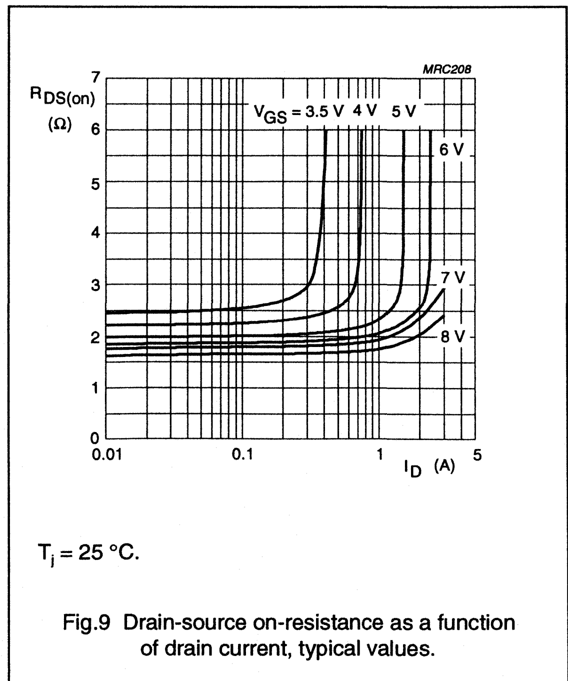
T_j = 25 °C.

Fig.7 Typical output characteristics.



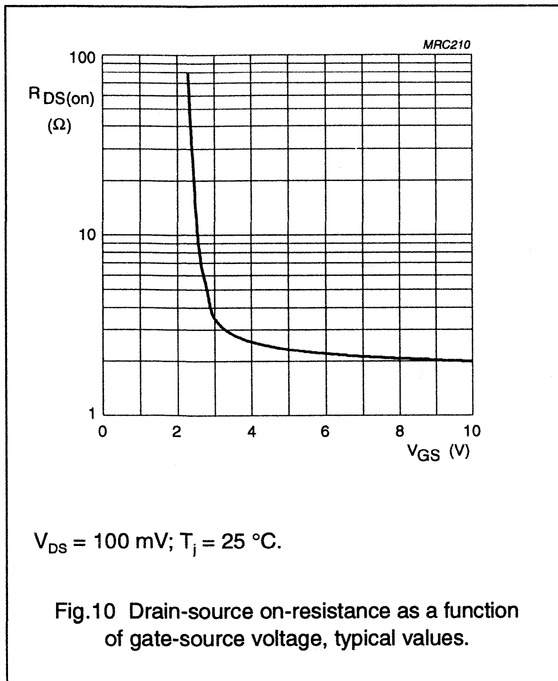
V_{DS} = 10 V; T_j = 25 °C.

Fig.8 Typical transfer characteristics.



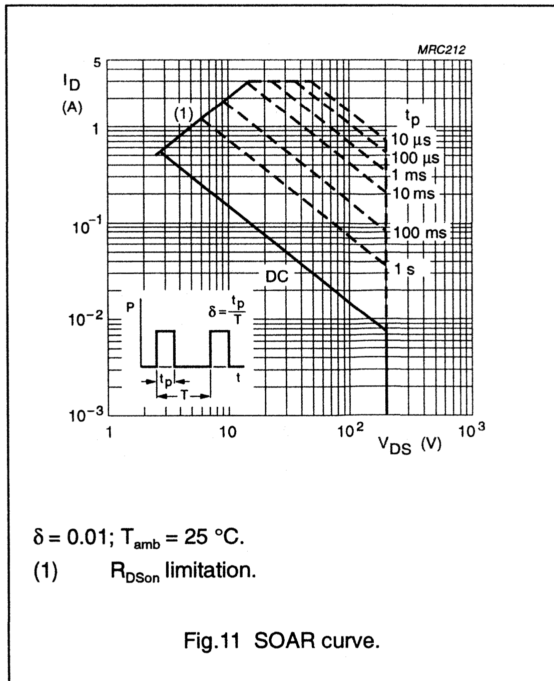
T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.10 Drain-source on-resistance as a function of gate-source voltage, typical values.



δ = 0.01; T_{amb} = 25 °C.

(1) R_{DSon} limitation.

Fig.11 SOAR curve.

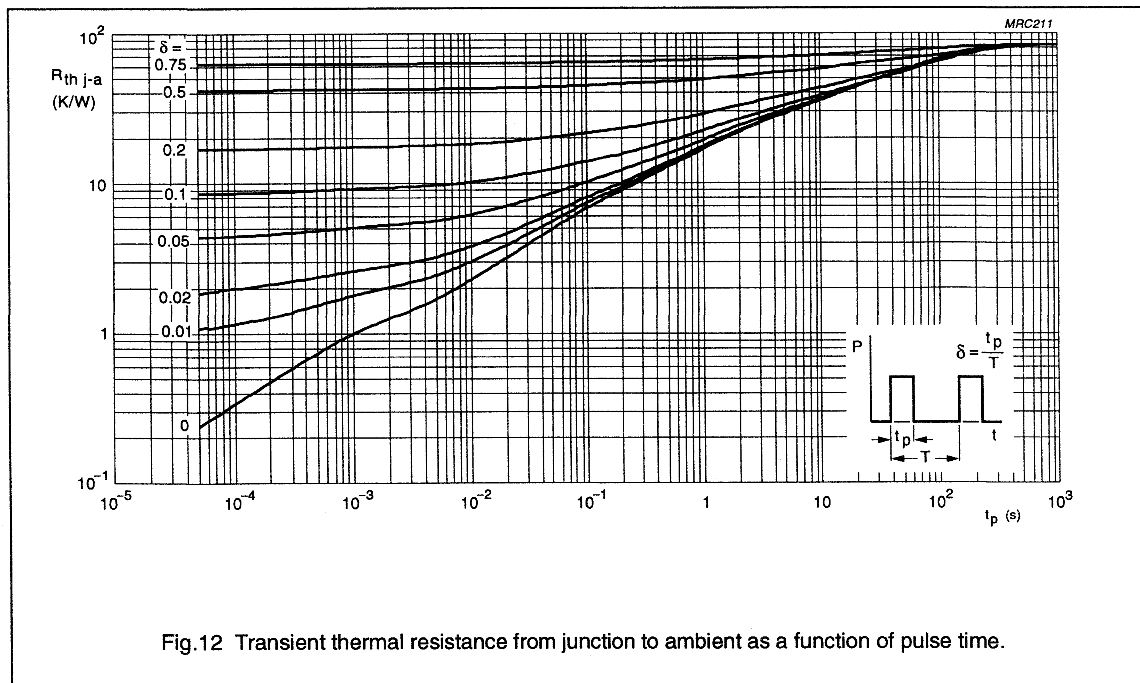
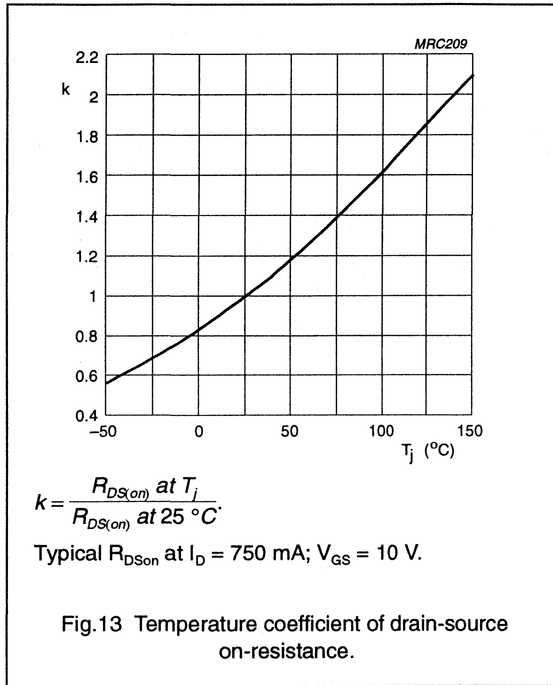


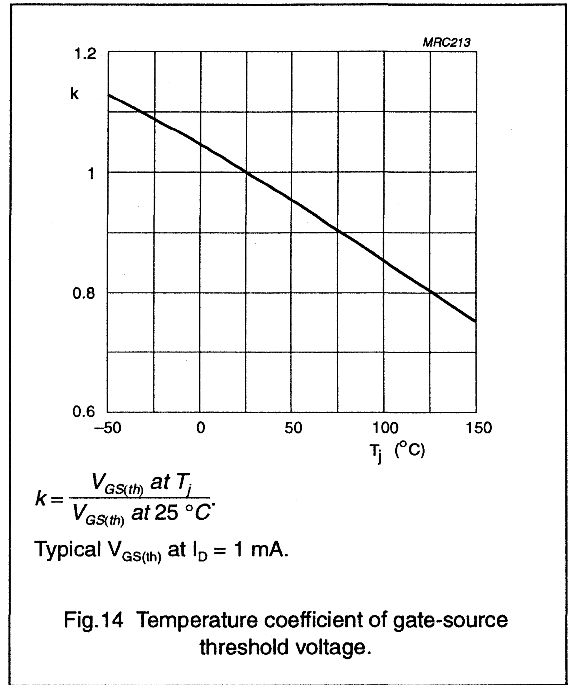
Fig.12 Transient thermal resistance from junction to ambient as a function of pulse time.



$$k = \frac{R_{DS(on)}\ at\ T_j}{R_{DS(on)}\ at\ 25\ °C}.$$

Typical R_{DSon} at I_D = 750 mA; V_{GS} = 10 V.

Fig.13 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)}\ at\ T_j}{V_{GS(th)}\ at\ 25\ °C}.$$

Typical $V_{GS(th)}$ at I_D = 1 mA.

Fig.14 Temperature coefficient of gate-source threshold voltage.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	November 1990

BSP204/BSP204A
P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant (BSP204)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP204A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200$ mA $-V_{GS} = 10$ V	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1$ mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

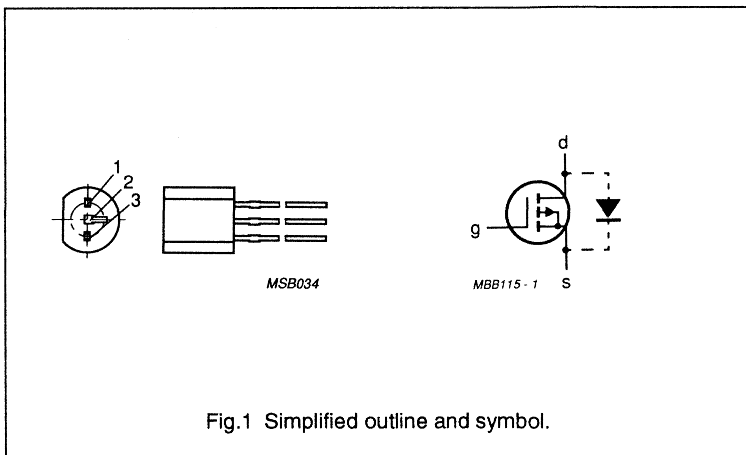


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
$-I_D$	drain current	DC value	–	250	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

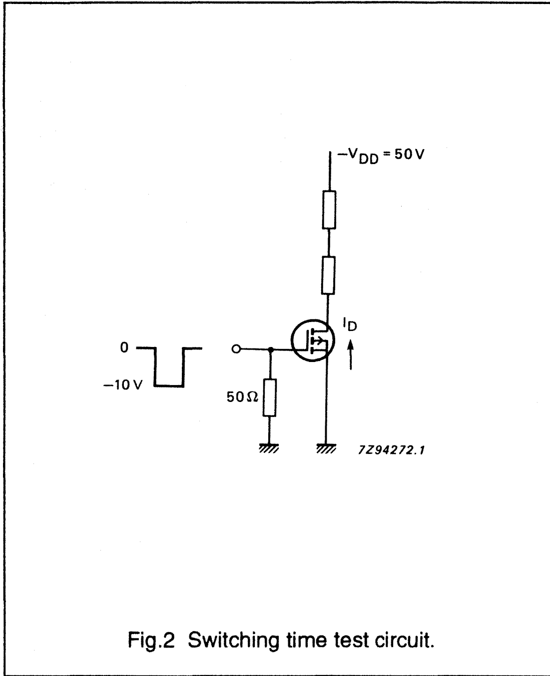


Fig.2 Switching time test circuit.

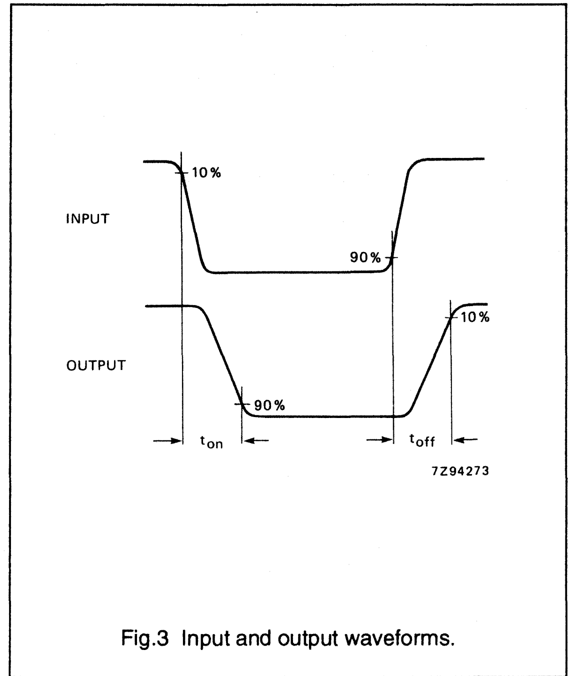


Fig.3 Input and output waveforms.

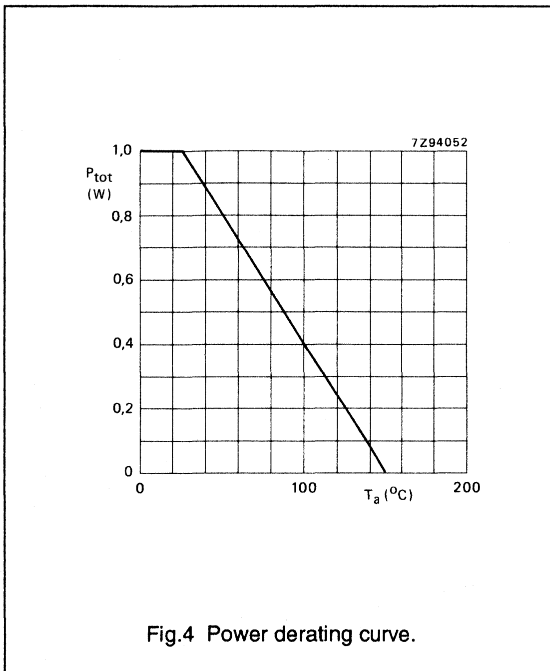


Fig.4 Power derating curve.

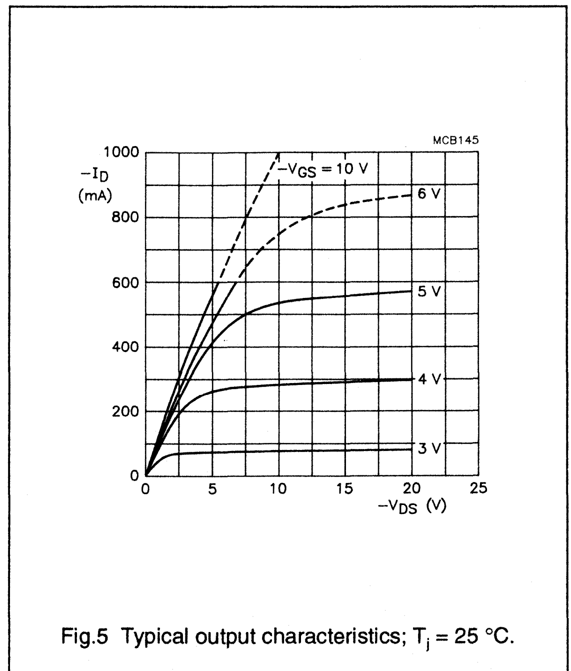


Fig.5 Typical output characteristics; T_j = 25 °C.

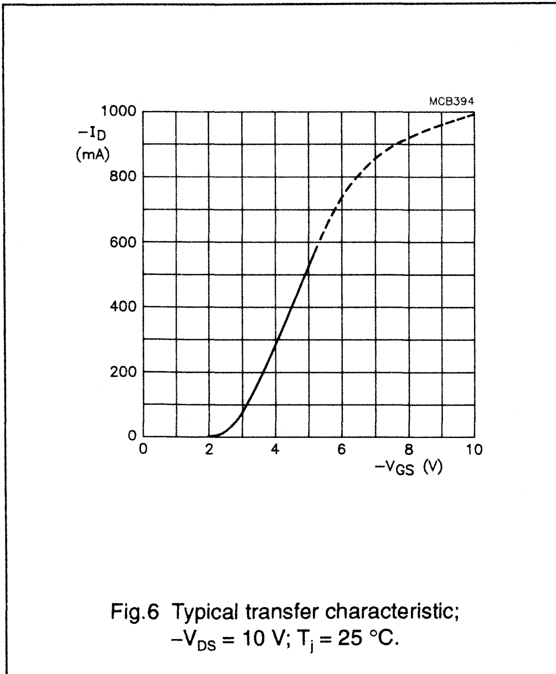


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

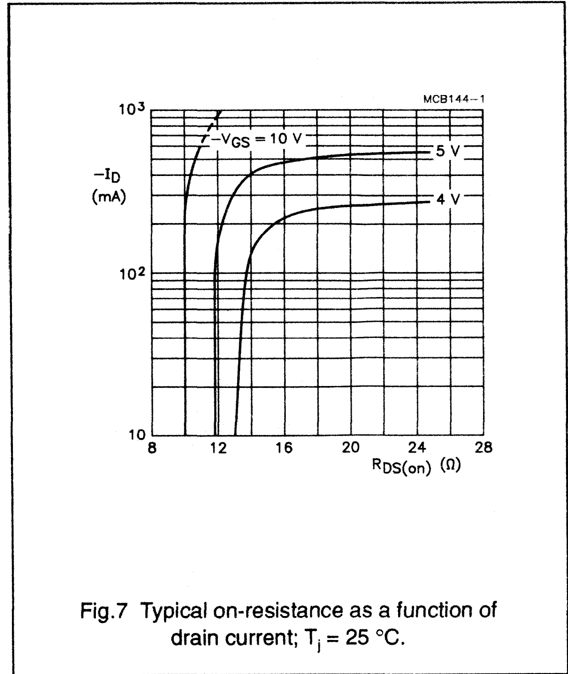


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

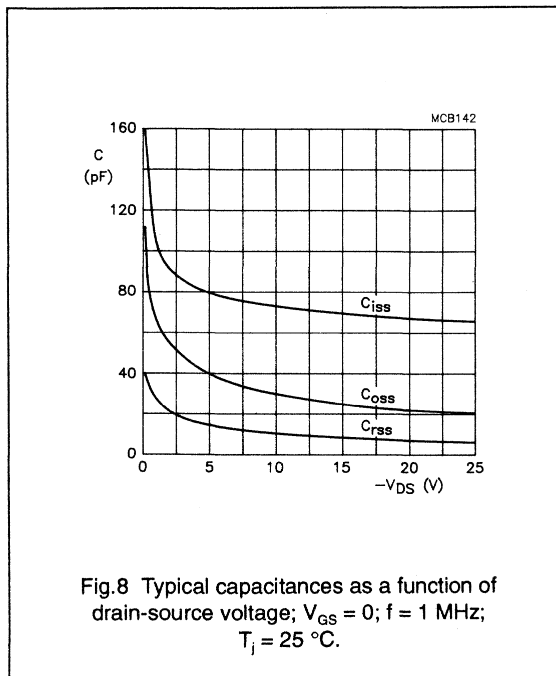


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

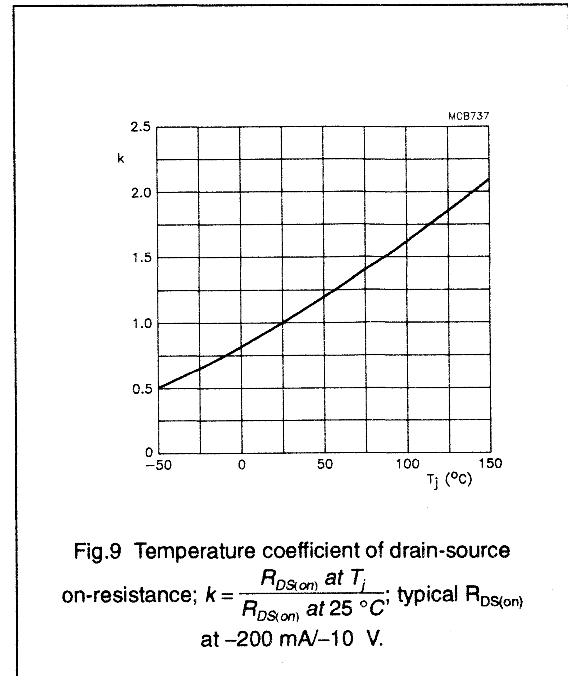


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

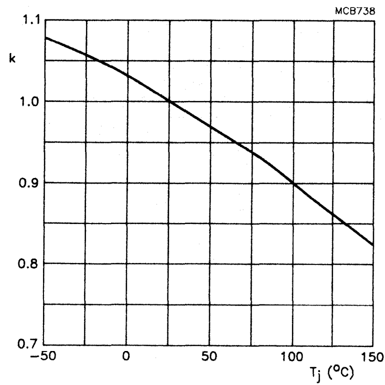


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)}\ at\ T_j}{-V_{GS(th)}\ at\ 25\ °C}$; typical $-V_{GS(th)}$ at −1 mA.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	275 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	max.	10 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA

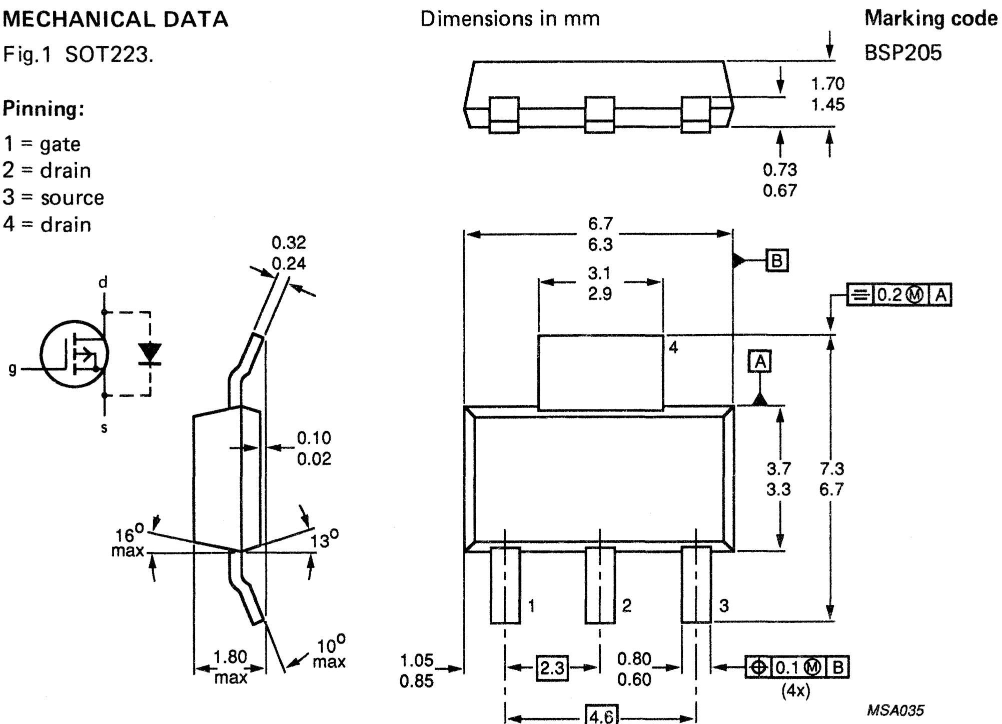
Dimensions in mm

Marking code
BSP205

Fig.1 SOT223.

Pinning:

1 = gate
2 = drain
3 = source
4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	275	mA
Drain current (peak)	$-I_{DM}$	max.	550	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D = 10\ \mu A$; $V_{GS} = 0$	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS} = 48$ V; $V_{GS} = 0$	$-I_{DSS}$	max.	1.0	μA
Gate-source leakage current $\pm V_{GS} = 20$ V; $V_{DS} = 0$	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D = 1$ mA; $V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D = 200$ mA; $-V_{GS} = 10$ V	$r_{DS(on)}$	typ. max.	7.5 10	Ω Ω
Transfer admittance $-I_D = 200$ mA; $-V_{DS} = 15$ V	$\|Y_{fs}\|$	min. typ.	60 125	mS mS
Input capacitance at f = 1 MHz; $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{iss}	typ. max.	30 45	pF pF
Output capacitance at f = 1 MHz; $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz; $-V_{DS} = 10$ V; $V_{GS} = 0$	C_{rss}	typ. max.	5 10	pF pF
Switching times (see Figs 2 and 3) $-I_D = 200$ mA; $-V_{DD} = 50$ V; $-V_{GS} = 0$ to 10 V	t_{on}	typ. max.	3 6	ns ns
	t_{off}	typ. max.	10 15	ns ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

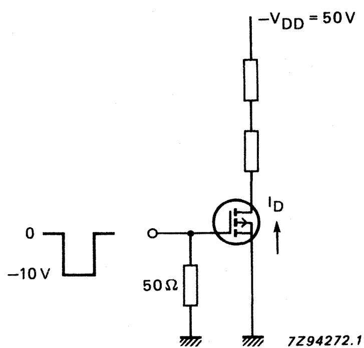


Fig.2 Switching time test circuit.

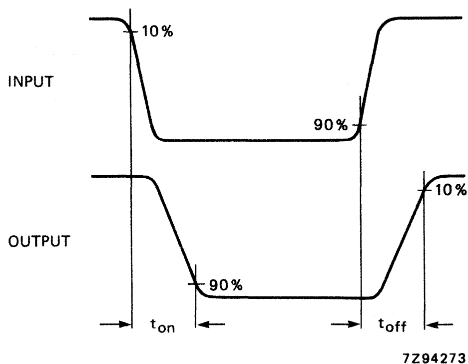


Fig.3 Input and output waveforms.

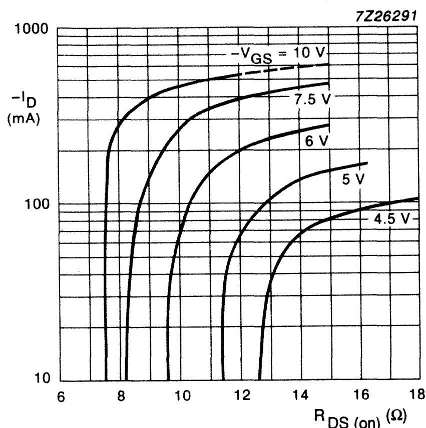


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

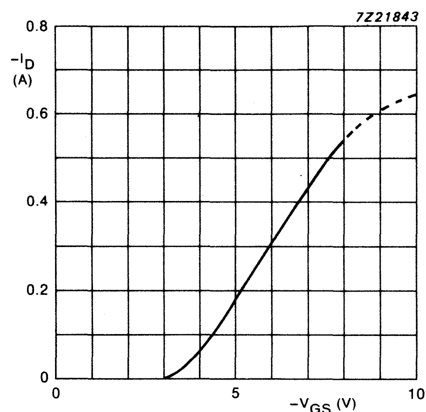


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

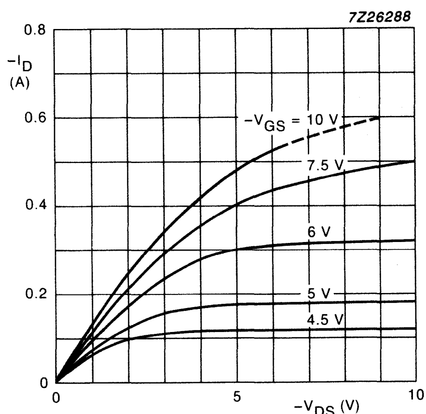


Fig.6 Output characteristics; T_j = 25 °C; typical values.

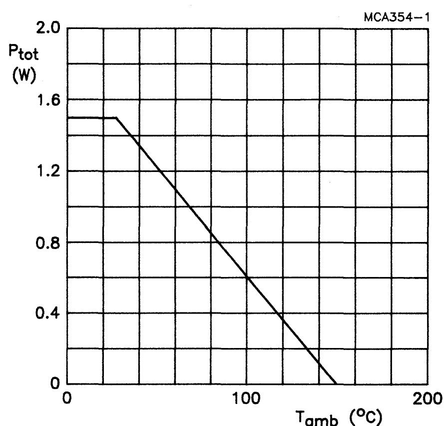


Fig.7 Power derating curve.

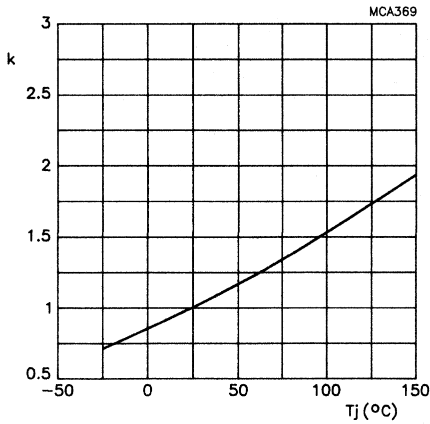


Fig.8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25\ ^oC}$; at −200 mA/−10 V; typical values.

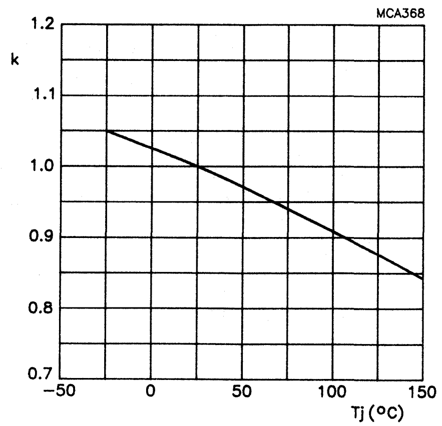


Fig.9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^oC}$; $-V_{GS(th)}$ at −1 mA; typical values.

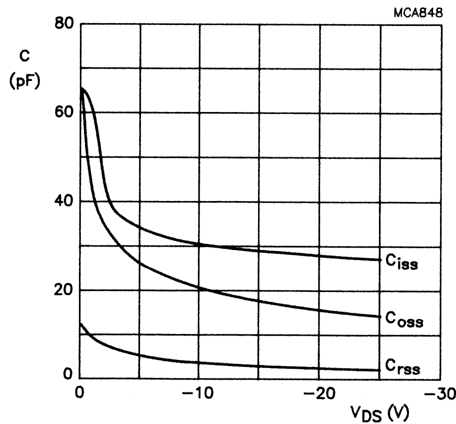


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	max.	6 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA

Dimensions in mm

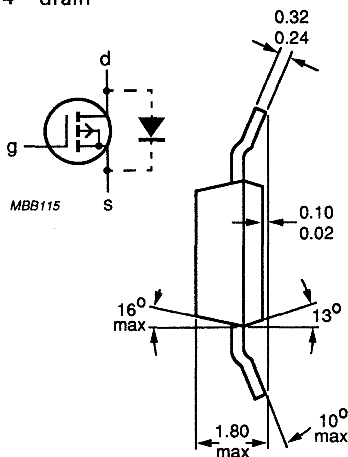
Marking code

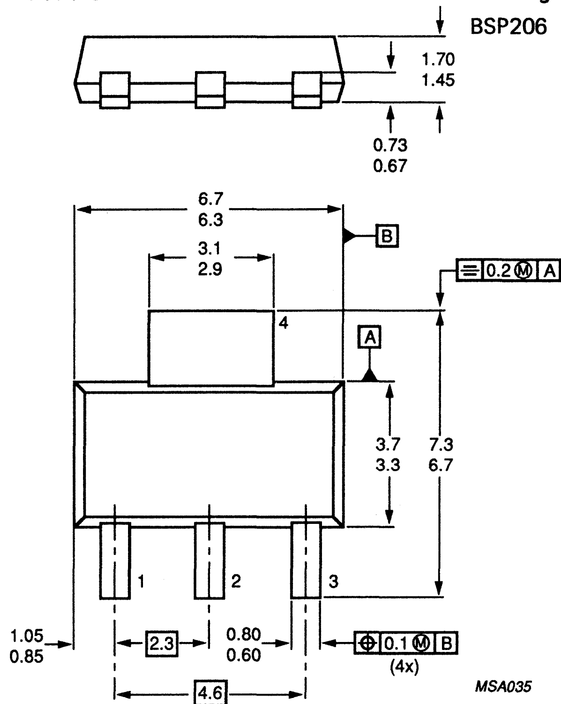
BSP206

Fig.1 SOT223.

Pinning:

1 = gate
2 = drain
3 = source
4 = drain





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	350	mA
Drain current (peak)	$-I_{DM}$	max.	700	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 10 µA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0	µA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	typ. max.	4.5 6	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	min. typ.	100 200	mS mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 70	pF pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	4 8	ns ns
	t_{off}	typ. max.	15 25	ns ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

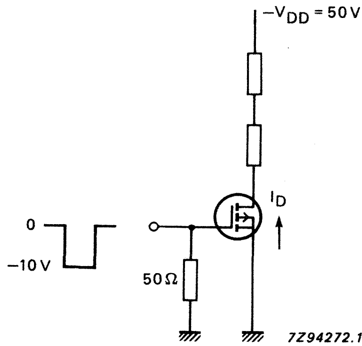


Fig.2 Switching time test circuit.

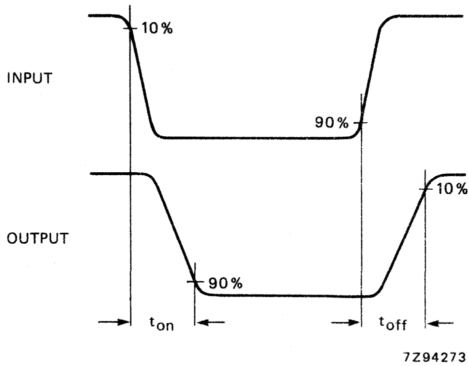


Fig.3 Input and output waveforms.

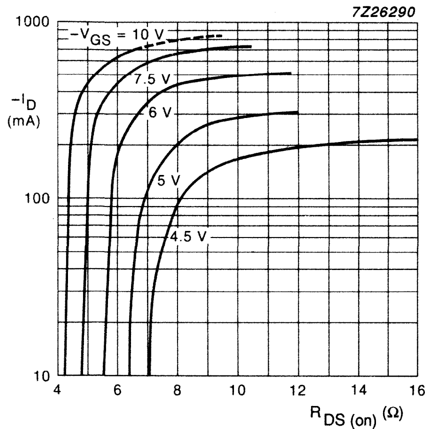


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

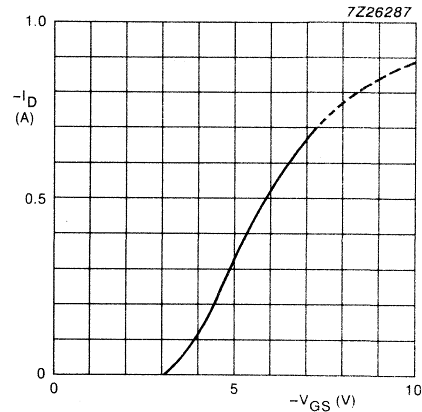


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

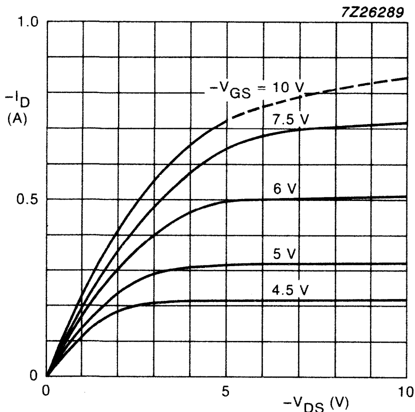


Fig.6 Output characteristics; T_j = 25 °C; typical values.

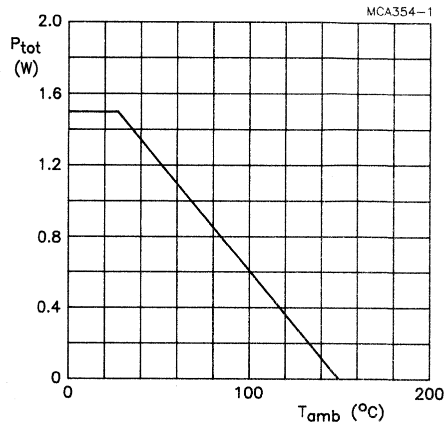


Fig.7 Power derating curve.

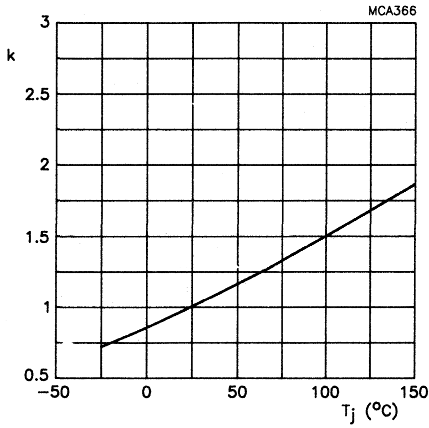


Fig.8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25\ ^oC}$; at −200 mA/−10V; typical values.

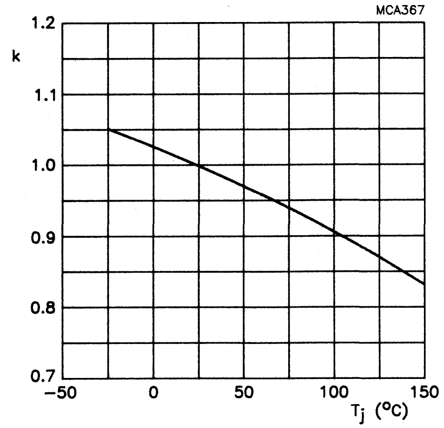


Fig.9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^oC}$; $-V_{GS(th)}$ at −1 mA; typical values.

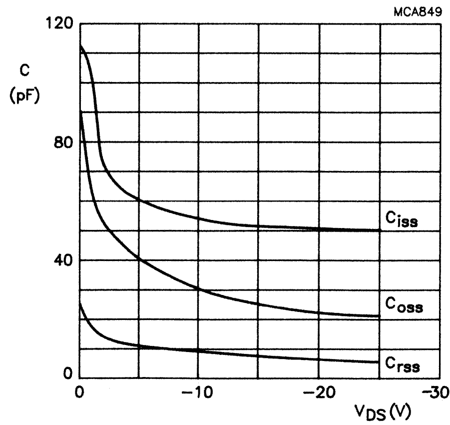


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1991

BSP220

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	12	Ω
$-V_{GS(th)}$	gate-source threshold voltage		2.8	V

PIN CONFIGURATION

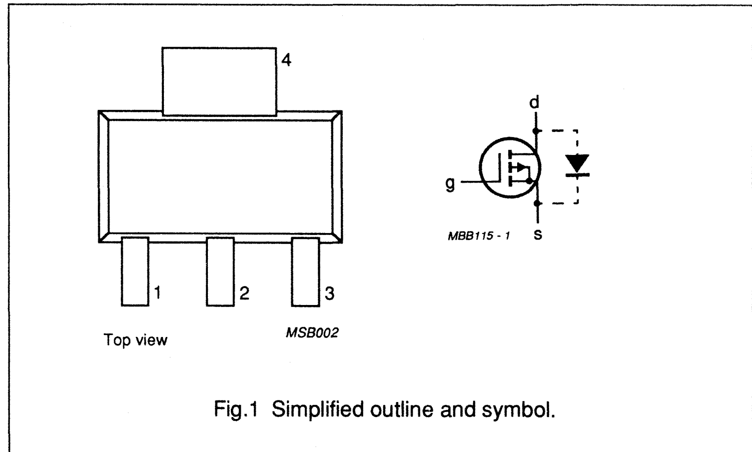


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP220

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	12	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	20	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

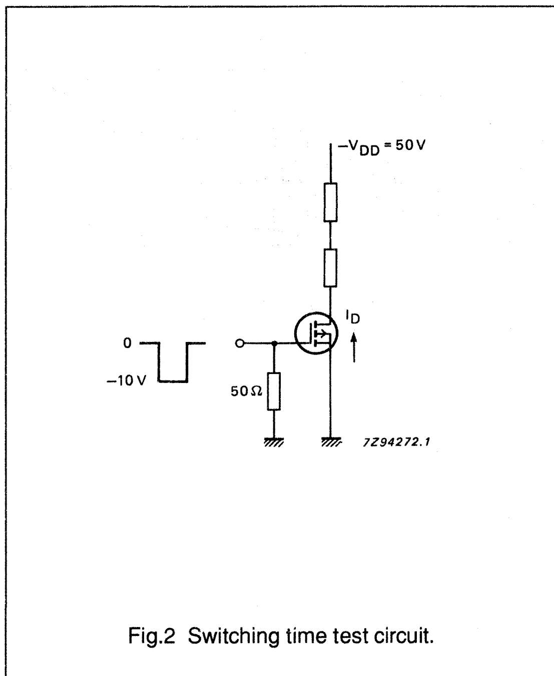


Fig.2 Switching time test circuit.

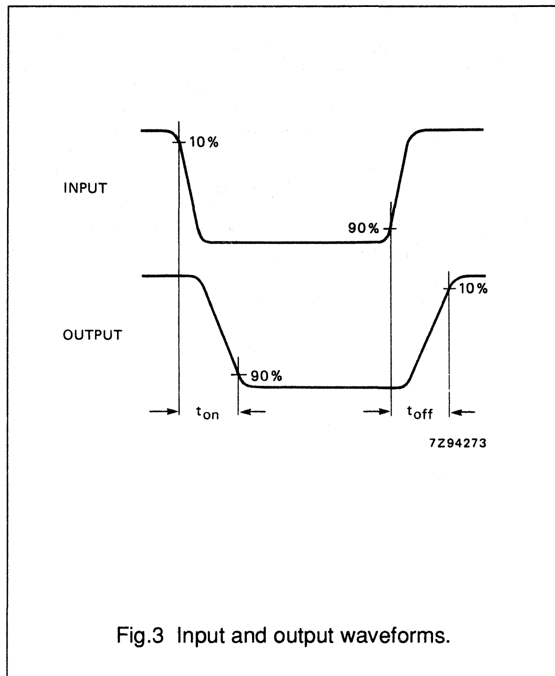


Fig.3 Input and output waveforms.

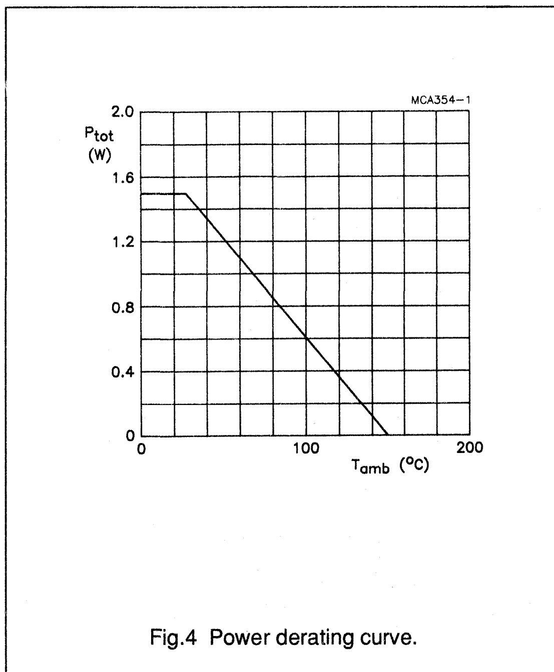


Fig.4 Power derating curve.

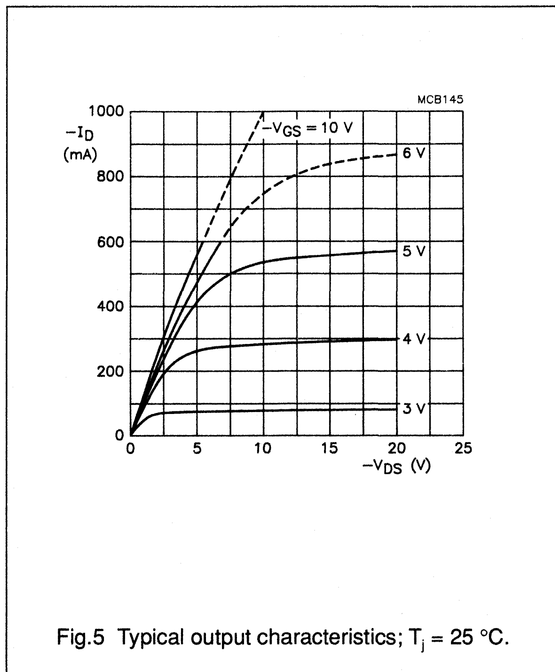


Fig.5 Typical output characteristics; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP220

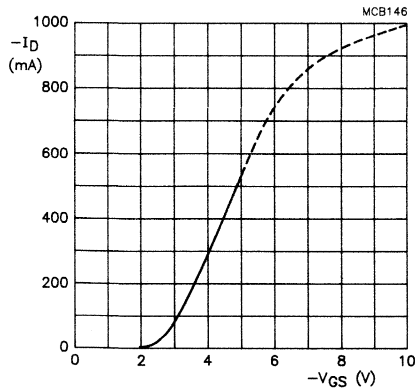


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

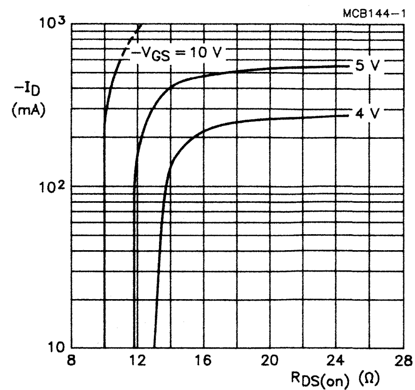


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

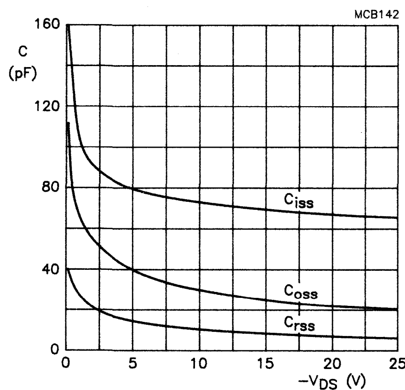


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

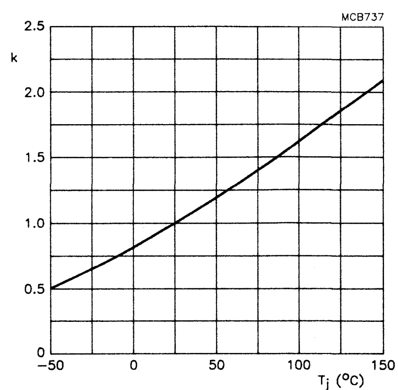


Fig.9 Temperature coefficent of drain-source on-resistance; $k = \frac{R_{DS(on)}\ at\ T_j}{R_{DS(on)}\ at\ 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

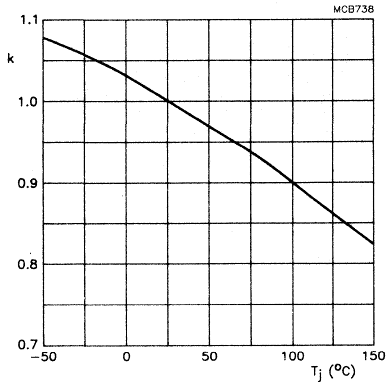


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $-V_{GS(th)}$ at −1 mA.

Data sheet	
status	Product specification
date of issue	November 1990

BSP225
P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200$ mA $-V_{GS} = 10$ V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1$ mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

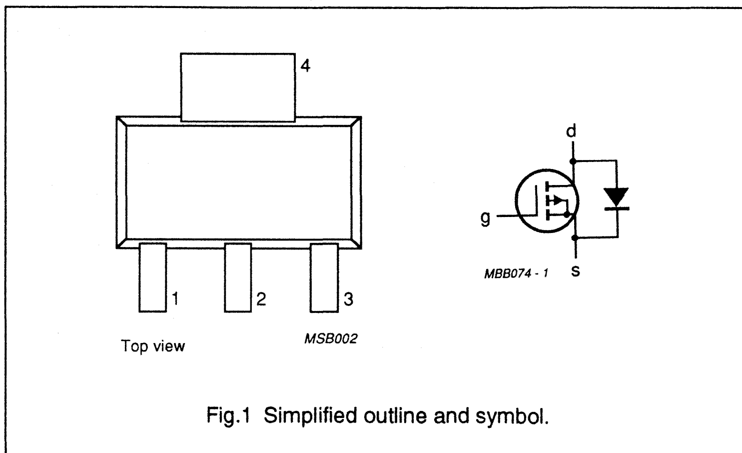


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 20 V	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

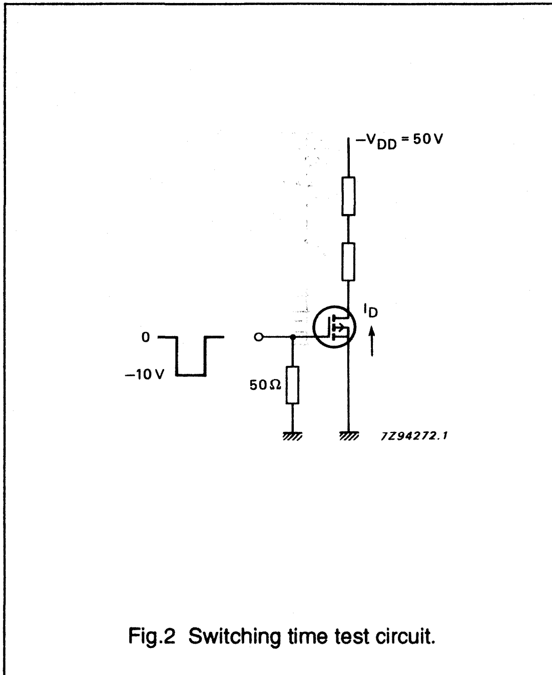


Fig.2 Switching time test circuit.

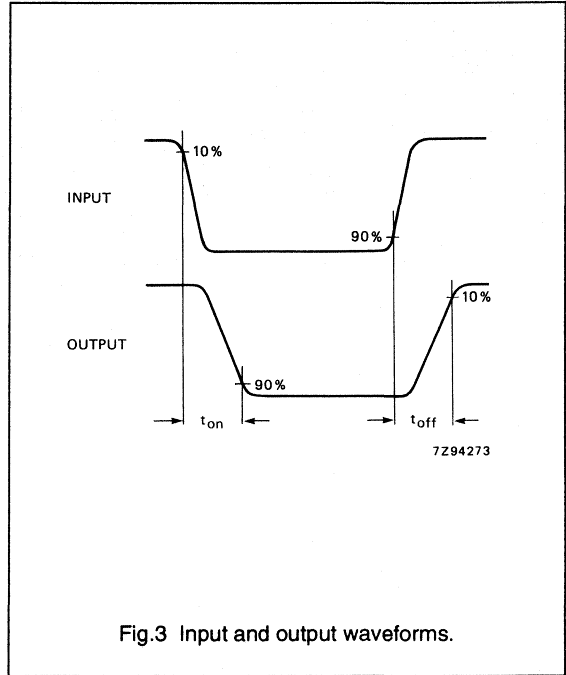


Fig.3 Input and output waveforms.

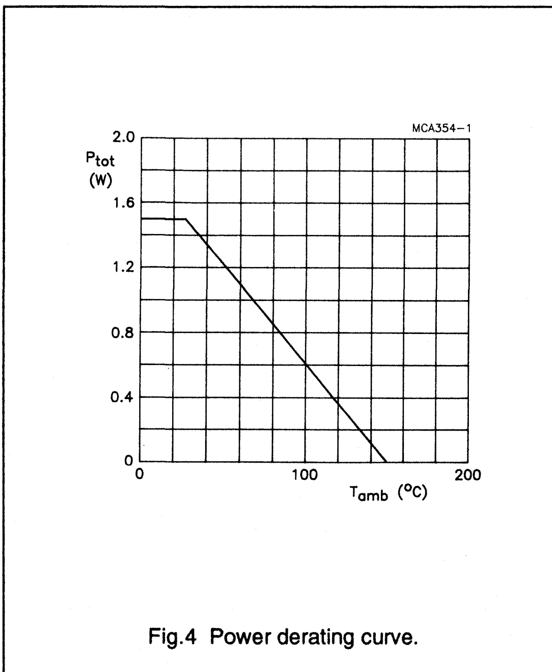


Fig.4 Power derating curve.

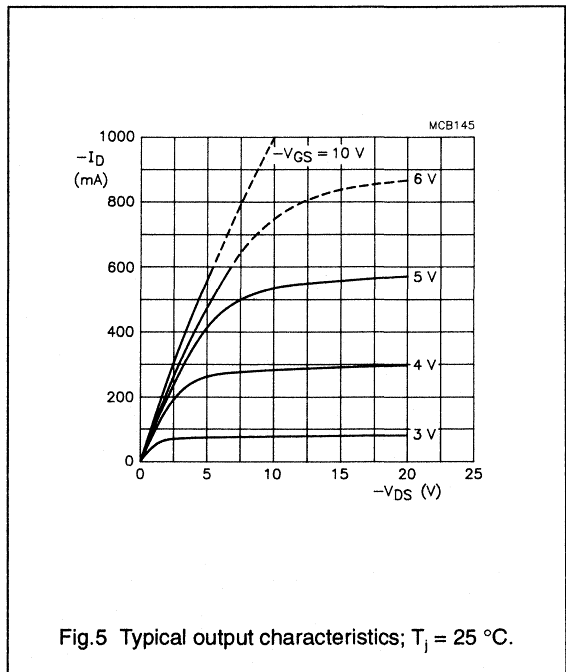


Fig.5 Typical output characteristics; T_j = 25 °C.

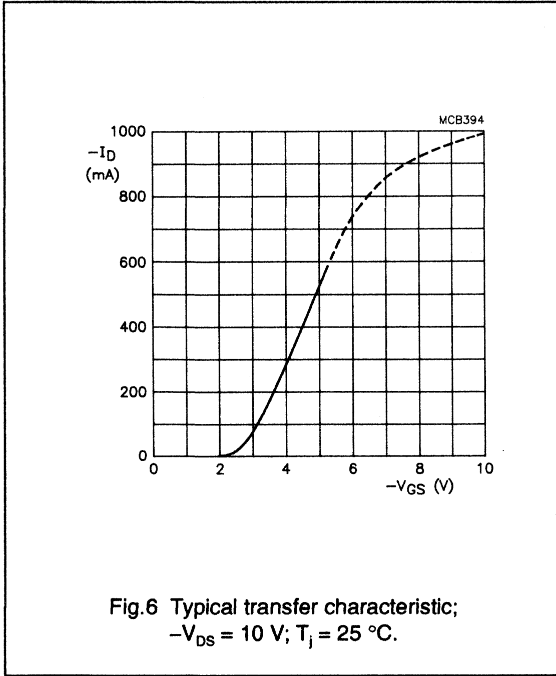


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

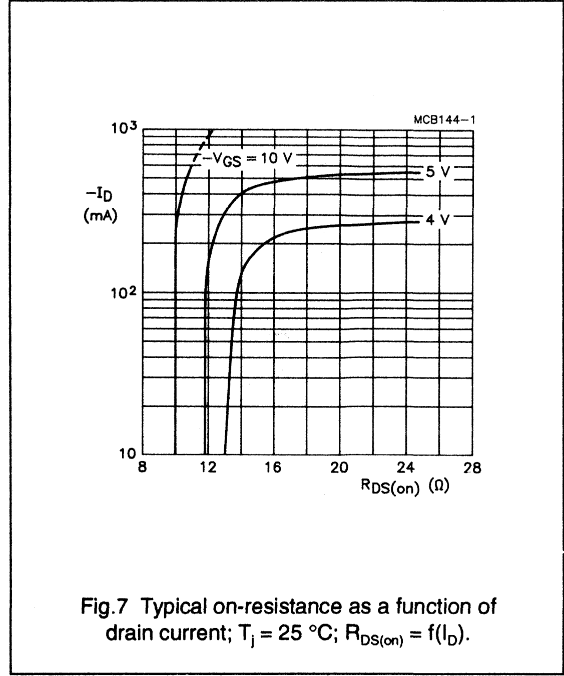


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C; $R_{DS(on)} = f(I_D)$.

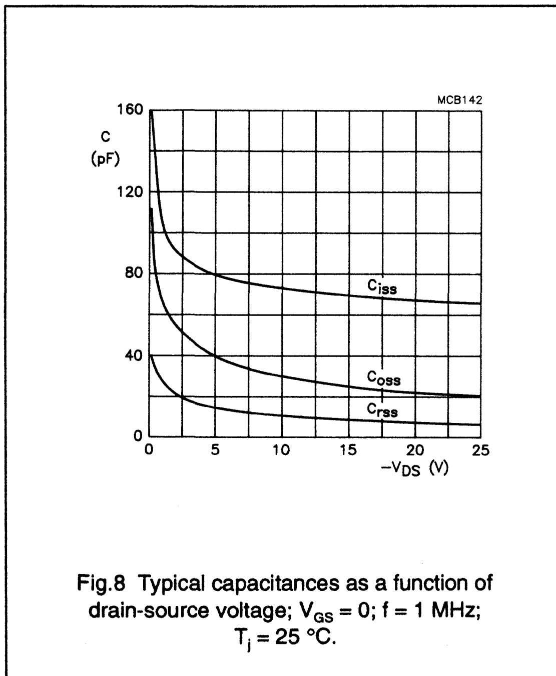


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

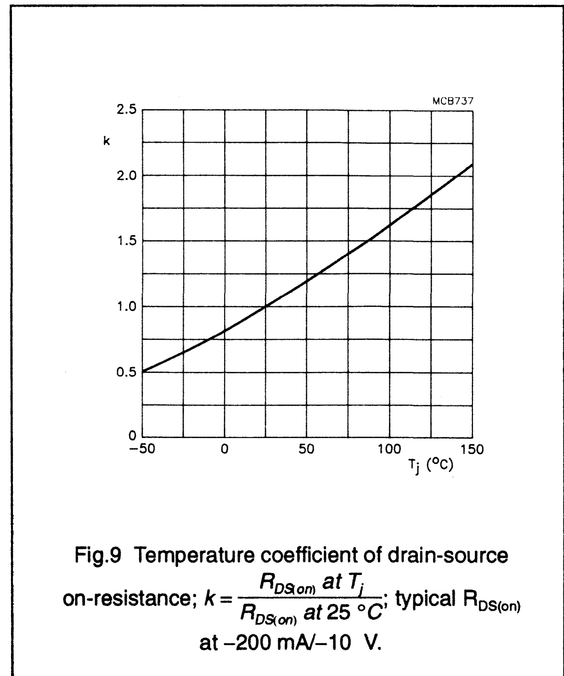


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

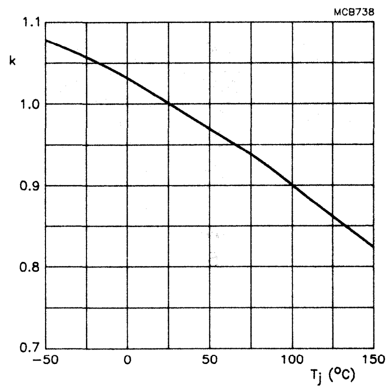


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

BSP254/BSP254A

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

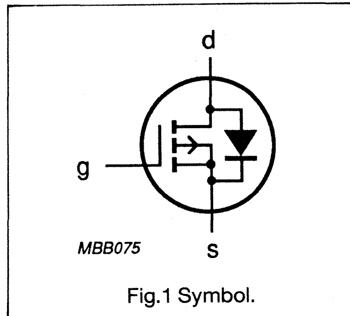


Fig.1 Symbol.

PINNING - TO-92 variant (BSP254)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP254A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	-	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	-	20	V
$-I_D$	drain-current	DC	-	-	0.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	-	1	W
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	15	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	-	mS

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
$-I_D$	drain current	DC	-	0.2	A
$-I_{DM}$	drain current	peak value	-	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
R_{thj-a}	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

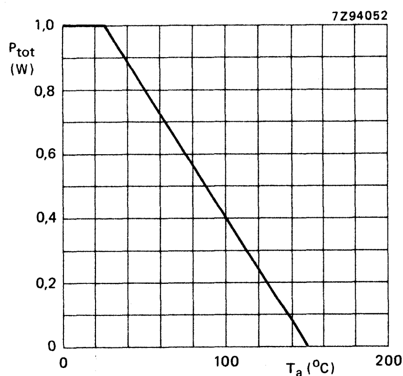


Fig.2 Power derating curve.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS} = 0$ $-I_D = 10\ \mu A$	250	-	-	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS} = 200\ V$ $V_{GS} = 0$	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\ V$ $V_{DS} = 0$	-	-	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$V_{GS} = V_{DS}$ $-I_D = 1\ mA$	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS} = 10\ V$ $-I_D = 200\ mA$	-	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-V_{DS} = 25\ V$ $-I_D = 200\ mA$	100	200	-	mS
C_{iss}	input capacitances	note 1	-	65	90	pF
C_{oss}	output capacitance	note 1	-	20	30	pF
C_{rss}	feedback capacitance	note 1	-	6	15	pF
t_{on}	turn-on time	note 2	-	5	10	ns
t_{off}	turn-off time	note 2	-	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

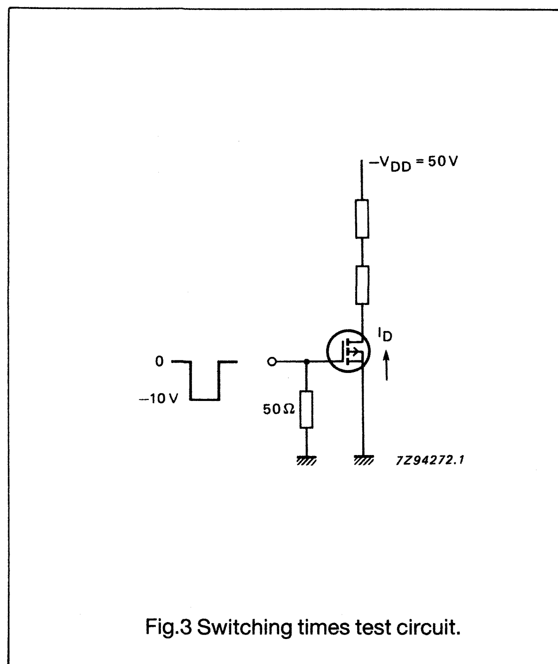


Fig.3 Switching times test circuit.

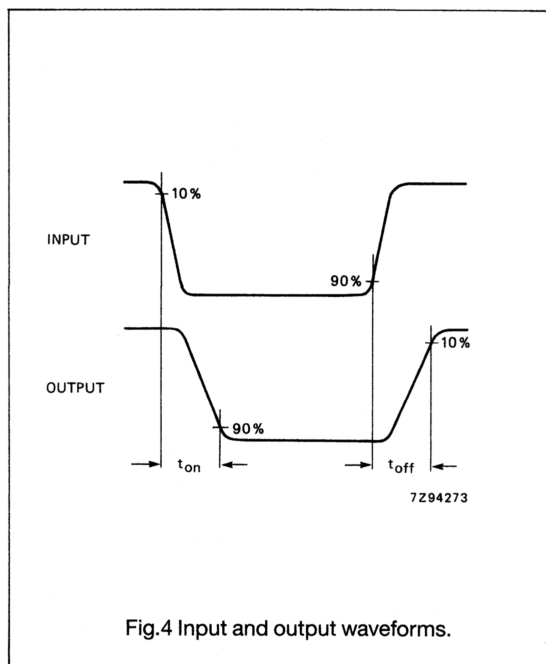


Fig.4 Input and output waveforms.

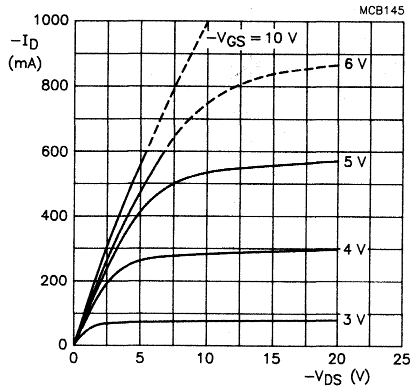


Fig.5 Typical output characteristics; T_j = 25 °C.

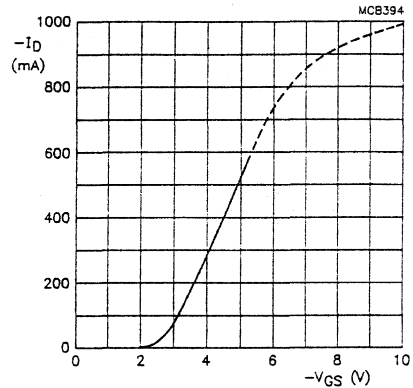


Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

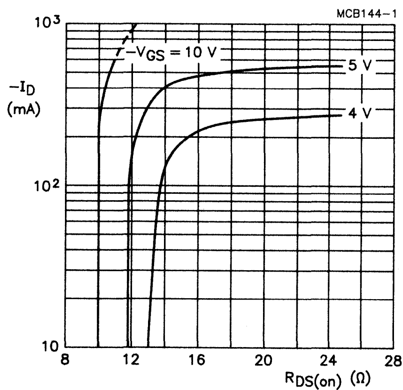


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

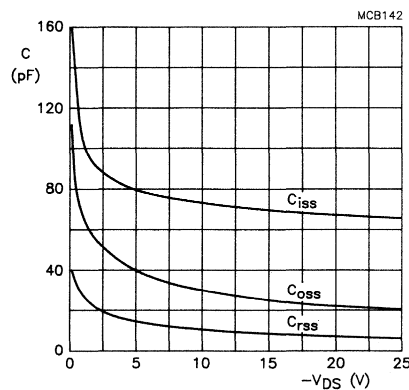


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

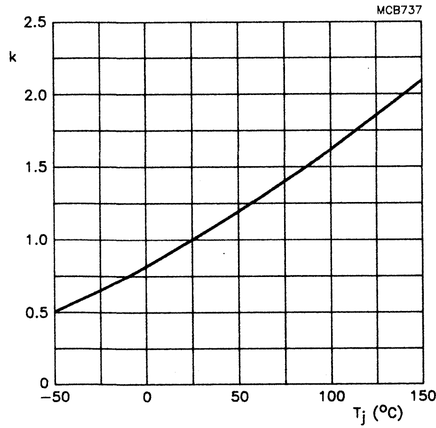


Fig.9 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V;

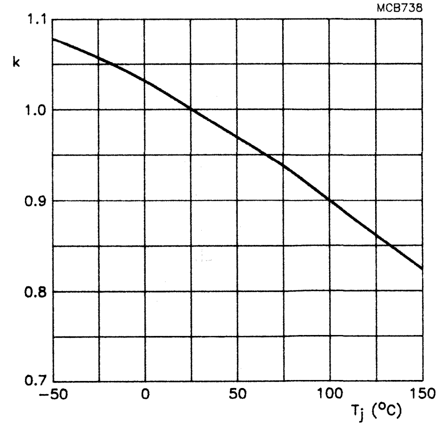


Fig.10 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

N-CHANNEL FETS

Symmetrical silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

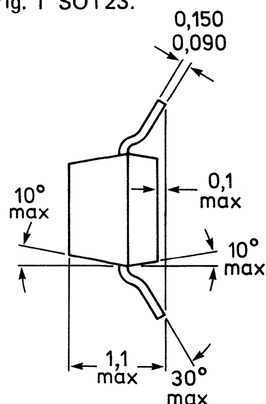
QUICK REFERENCE DATA

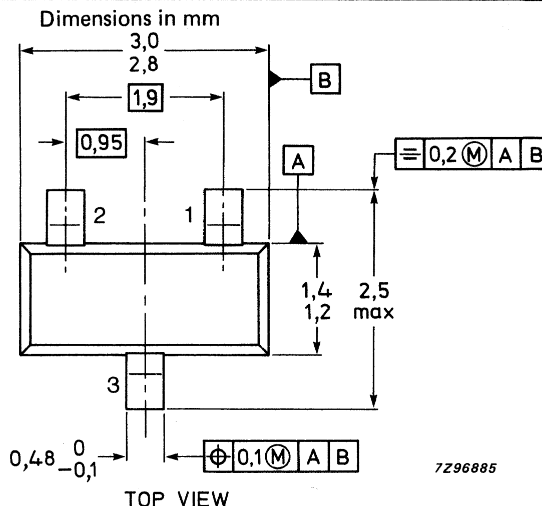
			BSR56	BSR57	BSR58	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	250	250	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source cut-off voltage V_{DS} = 15 V; I_D = 0.5 nA	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz $-V_{GS}$ = 10 V; V_{DS} = 0	C_{rs}	<	5	5	5	pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0						
I_D = 20 mA; $-V_{GSM}$ = 10 V	t_{off}	<	25	–	–	ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	t_{off}	<	–	50	–	ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	t_{off}	<	–	–	100	ns

MECHANICAL DATA

Fig. 1 SOT23.

Dimensions in mm



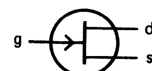


Marking code

BSR56 = M4p
BSR57 = M5p
BSR58 = M6p

Pinning

1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Drain-gate voltage	V_{DGO}	max.	40 V
Gate-source voltage	$-V_{GSO}$	max.	40 V
Forward gate current	I_{GF}	max.	50 mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source cut-off current V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	max.	1.0 nA
Drain cut-off current V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	max.	1.0 nA

			BSR56	BSR57	BSR58	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on) I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	750	–	–	mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	500	–	mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	400	mV
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0; T_a = 25 °C	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz $-V_{GS}$ = 10 V; V_{DS} = 0	C_{rss}	<	5	5	5	pF

Notes

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

			BSR56	BSR57	BSR58	
Switching times						
V_{DD} = 10 V; V_{GS} = 0						
Conditions I_D and $-V_{GSM}$	I_D	=	20	10	5	mA
	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

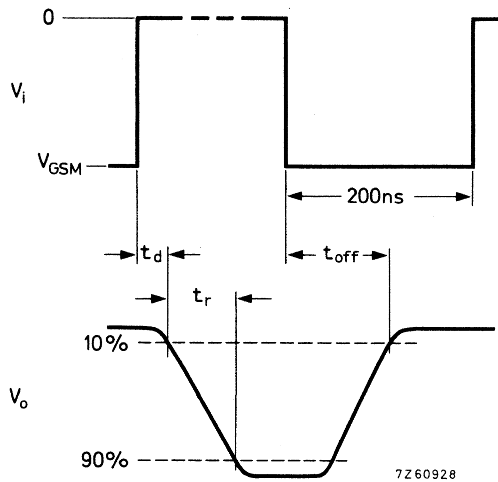


Fig. 2 Switching times waveforms.

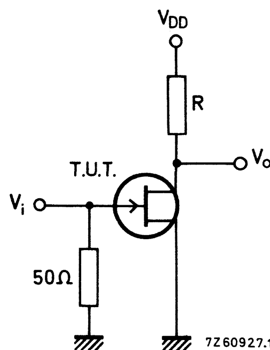


Fig. 3 Test circuit.

BSR56; R = 464 Ω
BSR57; R = 953 Ω
BSR58; R = 1910 Ω

Pulse generator

$t_r = t_f \leq 1$ ns
δ = 0.02
Z_o = 50 Ω

Oscilloscope

$t_r \leq 0.75$ ns
$R_i \geq$ 1 MΩ
$C_i \leq$ 2.5 pF

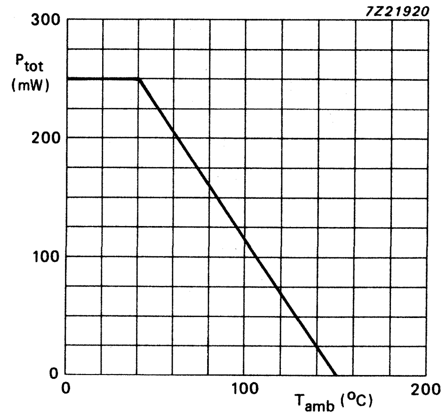


Fig.4 Power derating curve.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver

QUICK REFERENCE DATA

Parameter	Symbol		Value
Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (DC)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230 mW
Gate-source threshold voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu A$	$V_{GS(th)}$	$>$ $<$	0.1 V 2.0 V
Drain-source ON-resistance $V_{GS} = 10$ V; $V_{SB} = 0$; $I_D = 0.1$ mA	R_{DSon}	$<$	45 Ω
Feed-back capacitance $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V; f = 1 MHz	C_{rss}	typ.	0.6 pF

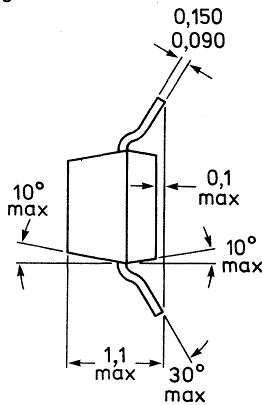
MECHANICAL DATA

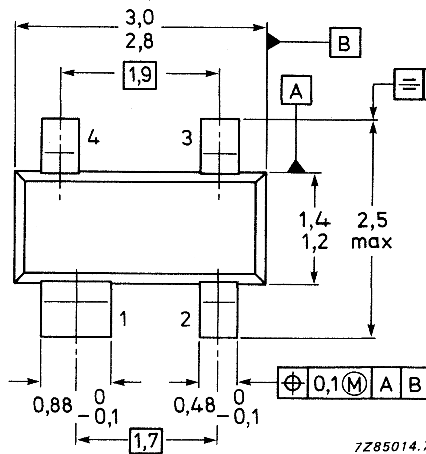
SOT143 (see Fig. 1).

See also *Soldering recommendations*.

Fig. 1 SOT143.

Dimensions in mm

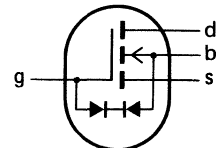




TOP VIEW

Marking code:
BSS83 = M74

Pinning;
1 = substrate (b)
2 = source
3 = drain
4 = gate



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (DC)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

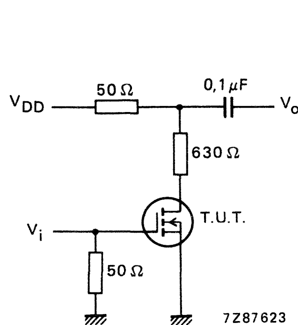
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_D = 10 nA	$V_{(BR)DSX}$	>	10 V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10 V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15 V
Source-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open drain	$V_{(BR)SBO}$	>	15 V
Drain-source leakage current $V_{GS} = V_{BS} = -2$ V; V_{DS} = 6,6 V	I_{DSoff}	<	10 nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Source-drain leakage current $V_{GD} = V_{BD} = -2$ V; $V_{SD} = 6,6$ V	I_{SDoff}	<	10 nA
Forward transconductance at f = 1 kHz $V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	> typ.	10 mS 15 mS
Gate-source threshold voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu$A	$V_{GS(th)}$	> <	0,1 V 2,0 V
Drain-source ON-resistance $I_D = 0,1$ mA;			
$V_{GS} = 5$ V; $V_{SB} = 0$	R_{DSon}	<	70 Ω
$V_{GS} = 10$ V; $V_{SB} = 0$	R_{DSon}	<	45 Ω
$V_{GS} = 3,2$ V; $V_{SB} = 6,8$ V (see Fig. 4)	R_{DSon}	typ. <	80 Ω 120 Ω
Gate-substrate zener voltages $V_{DB} = V_{SB} = 0$; $-I_G = 10\ \mu$A	$V_{Z(1)}$	>	12,5 V
$V_{DB} = V_{SB} = 0$; $+I_G = 10\ \mu$A	$V_{Z(2)}$	>	12,5 V
Capacitances at f = 1 MHz $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig. 2) $V_{DD} = 10$ V; $V_i = 5$ V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

Pulse generator:

R_i = 50 Ω
t_r < 0,5 ns
t_f < 1,0 ns
t_p = 20 ns
δ < 0,01



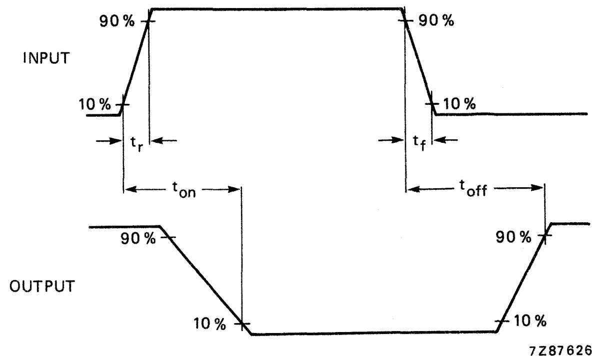


Fig. 2 Switching times test circuit and input and output waveforms.

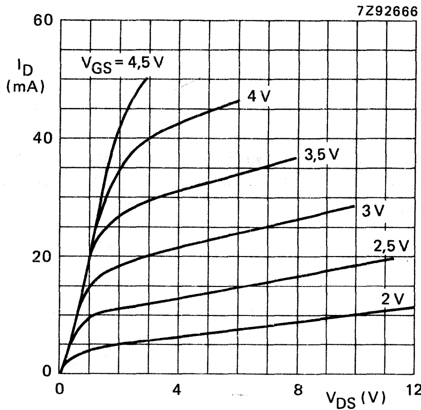


Fig. 3 $V_{SB} = 0$; typical values.

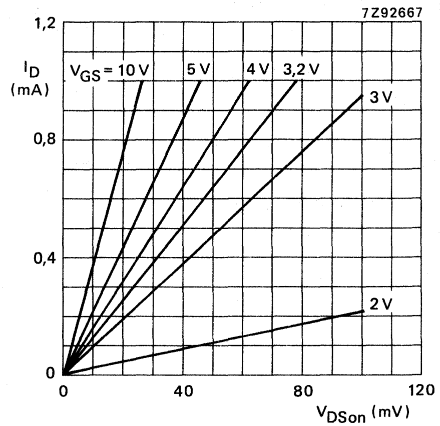


Fig. 4 $V_{SB} = 6{,}8$ V; typical values.

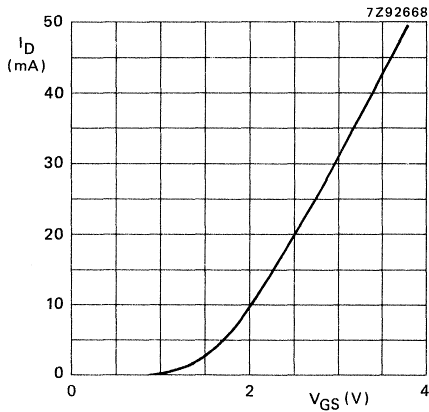


Fig. 5 $V_{DS} = 10$ V; $V_{BS} = 0$; typical values.

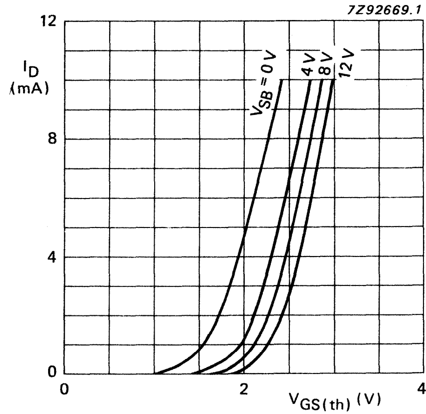


Fig. 6 $V_{DS} = V_{GS} = V_{GS(th)}$.

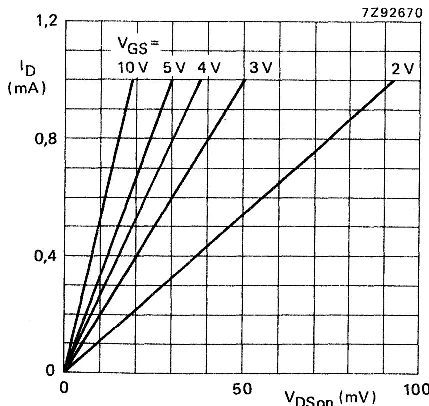


Fig. 7 $V_{SB} = 0$; typical values.

Conditions for Figs 3, 4, 5, 6 and 7:
$T_j = 25$ °C.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

BSS84
P-channel enhancement mode vertical D-MOS FET

DESCRIPTION

Silicon p-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

PIN CONFIGURATION

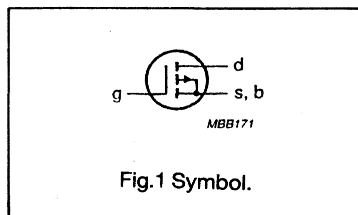


Fig.1 Symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	50	V
$-I_D$	drain current	130	mA
$R_{DS(on)}$	drain-source on resistance	10	Ω
$-V_{GS(th)}$	gate-source threshold voltage	2	V

P-channel enhancement mode vertical D-MOS FET

BSS84

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	50	V
$-V_{GSO}$	gate-source voltage	open drain $I_D = 0$	-	20	V
$-I_D$	drain current	average value	-	130	mA
$-I_{DM}$	drain current	peak value	-	520	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		−55	150	°C
T_j	junction temperature		-	150	°C

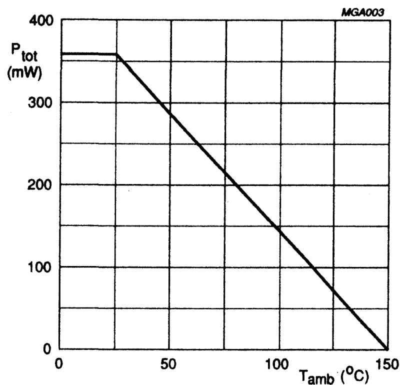


Fig.2 Total power dissipation as a function of ambient temperature.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

P-channel enhancement mode vertical D-MOS FET

BSS84

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 $-I_D$ = 250 µA	50	-	-	V
$-I_{DSS}$	drain-source leakage current	V_{GS} = 0 $-V_{DS}$ = 25 V	-	-	0.1	µA
		V_{GS} = 0 $-V_{DS}$ = 50 V	-	-	15	µA
		V_{GS} = 0 $-V_{DS}$ = 50 V T_j = 125 °C	-	-	60	µA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 20 V	-	-	60	µA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{DS} = V_{GS}	0.8	-	2	V
$R_{DS(on)}$	drain-source on resistance	$-V_{GS}$ = 5 V $-I_D$ = 100 mA	-	6	10	Ω
$\|y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 100 mA f = 1 kHz	50	70	-	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	-	40	-	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	-	15	-	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	-	6	-	pF
t_{on}	turn-on time	$-V_{CC}$ = 30 V $-I_D$ = 0.27 A $-V_{GS}$ = 0/5 V	-	20	-	ns
t_{off}	turn-off time	$-V_{CC}$ = 30 V $-I_D$ = 0.27 A $-V_{GS}$ = 0/5 V	-	43	-	ns

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in a SOT89 envelope.
Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS\ (on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ.	350	mS
		min.	140	mS

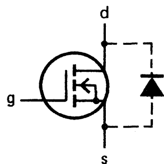
MECHANICAL DATA

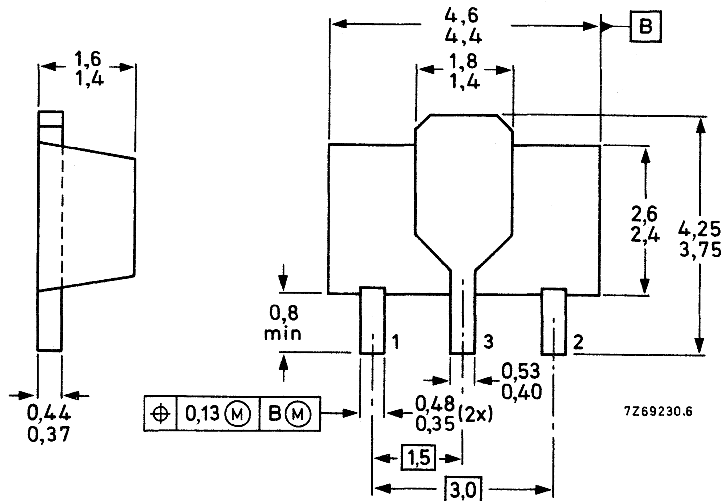
Dimensions in mm

Fig. 1 SOT89.

Pinning

1 = source
2 = gate
3 = drain





marking: KA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Drain current (peak)	I_{DM}	max.	1.1	A
Total power dissipation up to T_{amb} = 25 °C *	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient *	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	60	μA
		typ.	100	nA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	typ.	350	mS
		min.	140	mS
Input capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max.	60	pF
		typ.	45	pF
Output capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max.	25	pF
		typ.	15	pF
Feedback capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	10	pF
		typ.	3.5	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10	t_{on}	typ.	5	ns
		max.	10	ns
	t_{off}	typ.	15	ns
		max.	25	ns

* Transistor mounted on ceramic substrate area 2.5 cm², thickness 0.7 mm.

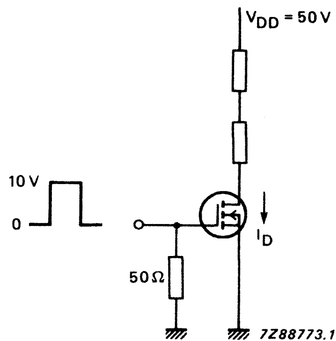


Fig. 2 Switching times test circuit.

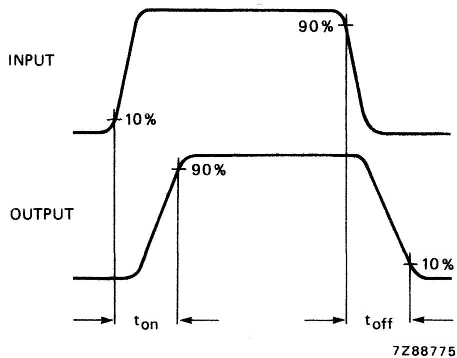


Fig. 3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS88

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	230	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.2	V

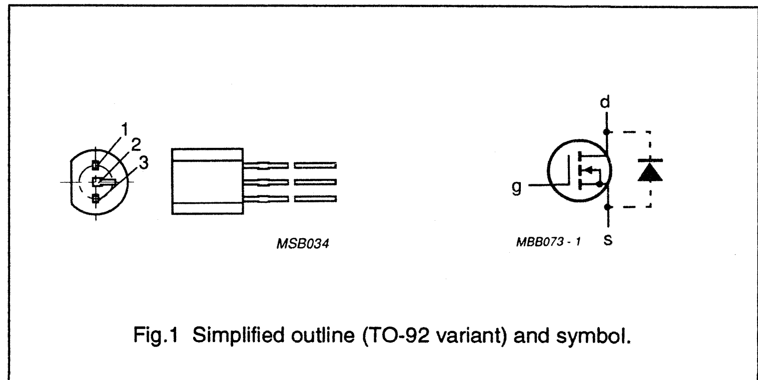


Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	230	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

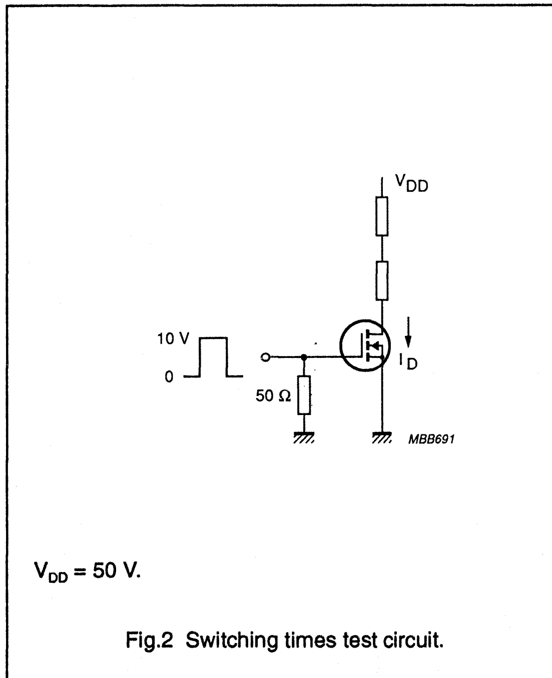
Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	230	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0	–	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; $V_{GS} = V_{DS}$	0.4	–	1.2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 14 mA; V_{GS} = 1.8 V	–	6	15	Ω
		I_D = 150 mA; V_{GS} = 5 V	–	5	8	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 150 mA; V_{DS} = 25 V	140	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

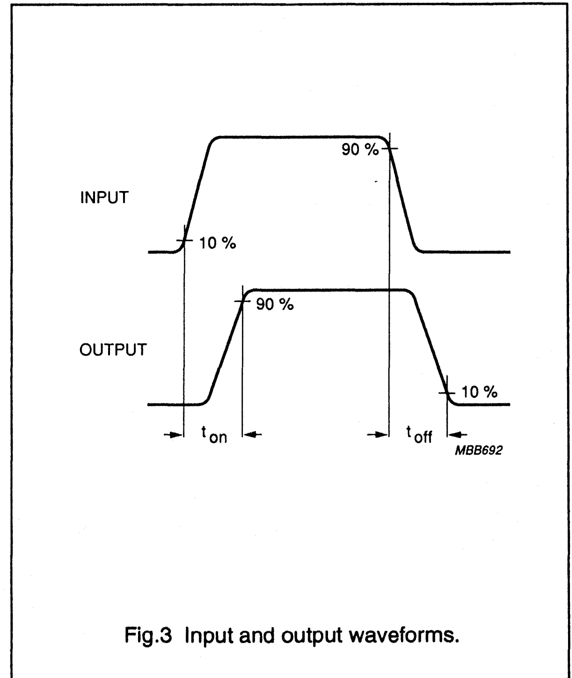


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and highspeed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

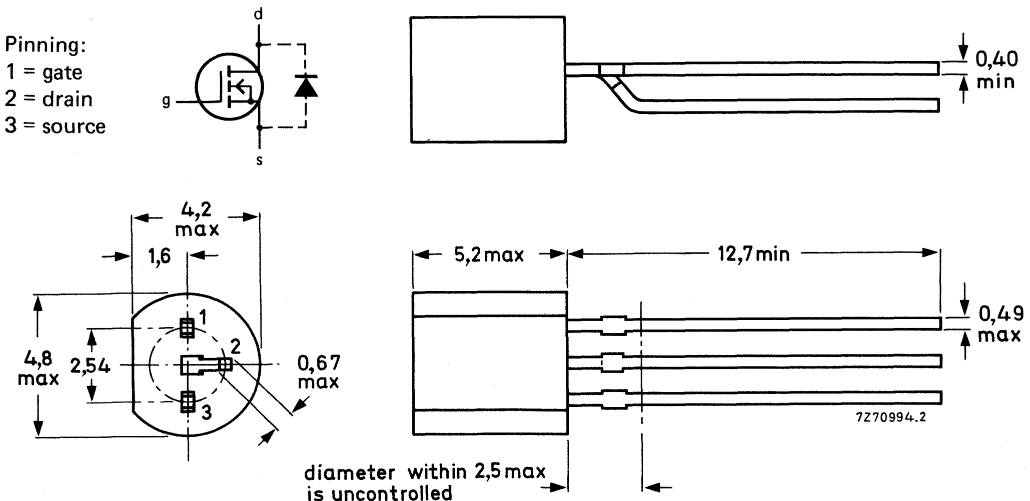
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5	Ω
		max.	6	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min.	140	mS
		typ.	350	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−55 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ. max.	100 60	nA μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 6	Ω Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	140 350	mS mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15	pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 15	ns ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

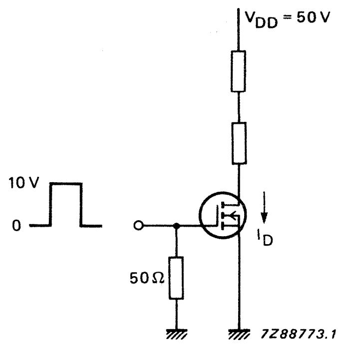


Fig. 2 Switching time test circuit.

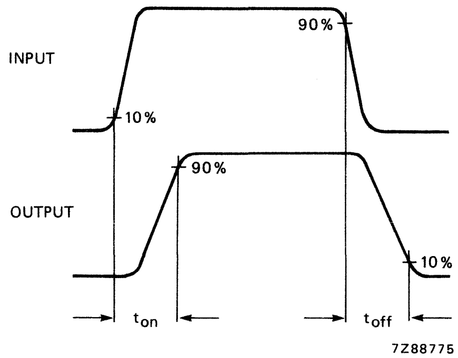


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-18 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5	Ω
		max.	6.0	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min.	140	mS
		typ.	350	mS

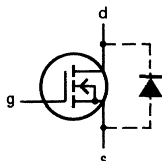
MECHANICAL DATA

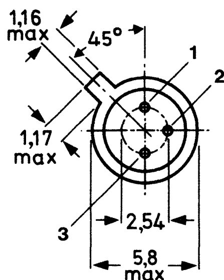
Dimensions in mm

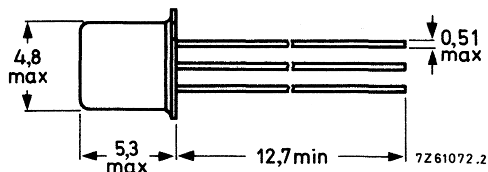
Fig. 1 TO-18.

Pinning

1 = source
2 = gate
3 = drain







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.4	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.4	W
T_{case} = 25 °C	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient	$R_{th\ j\text{-}a}$	=	310	K/W
From junction to case	$R_{th\ j\text{-}c}$	=	83	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ.	100	nA
		max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5	Ω
		max.	6.0	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	140	mS
		typ.	350	mS
Input capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45	pF
		max.	60	pF
Output capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15	pF
		max.	25	pF
Feedback capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5	pF
		max.	10	pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5	ns
		max.	15	ns
	t_{off}	typ.	15	ns
		max.	25	ns

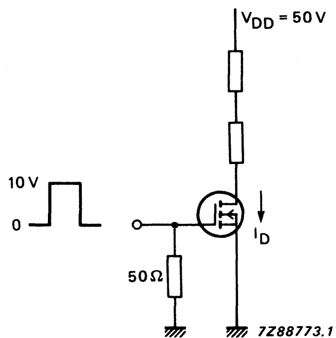


Fig. 2 Switching time test circuit.

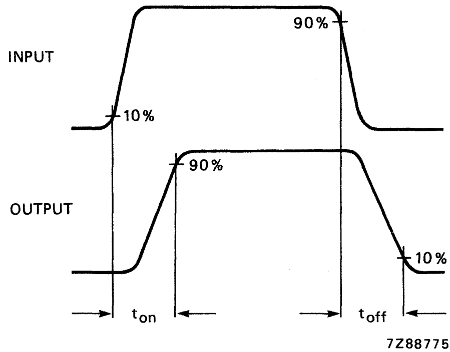


Fig. 3 Input and output waveforms.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers, and as a line current interruptor in telephony applications.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

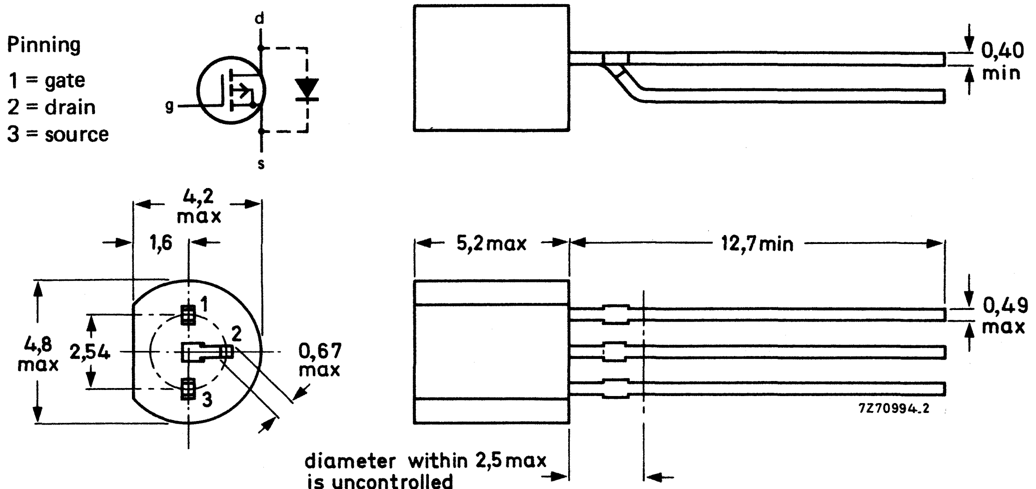
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.15	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ.	10	Ω
		max.	20	Ω
Transfer admittance				
$-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min.	60	mS
		typ.	200	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.15	A
Drain current (peak)	$-I_{DM}$	max.	0.6	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 250 μA; $-V_{GS}$ = 0	$-V_{(BR)DS}$	min.	200	V
Drain-source leakage current $-V_{DS}$ = 60 V; $-V_{GS}$ = 0	$-I_{DSS}$	max.	0.2	μA
$-V_{DS}$ = 200 V; $-V_{GS}$ = 0	$-I_{DSS}$	max.	60	μA
Gate-source leakage current $-V_{GS}$ = 20 V; $-V_{DS}$ = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 20	Ω Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\|y_{fs}\|$	min. typ.	60 200	mS mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{iss}	typ.	65	pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{oss}	typ.	20	pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{rss}	typ.	6	pF
Switching times (see Figs 2 and 3) $-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 20	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

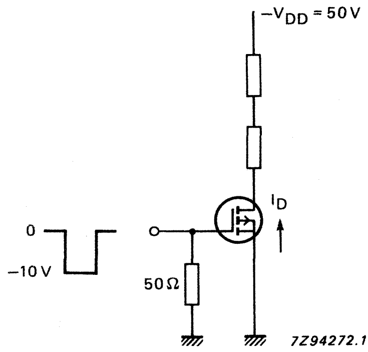


Fig. 2 Switching time test circuit.

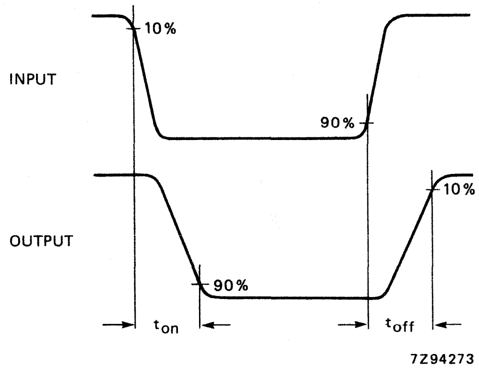


Fig. 3 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	November 1990

BSS100
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interrupter in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION

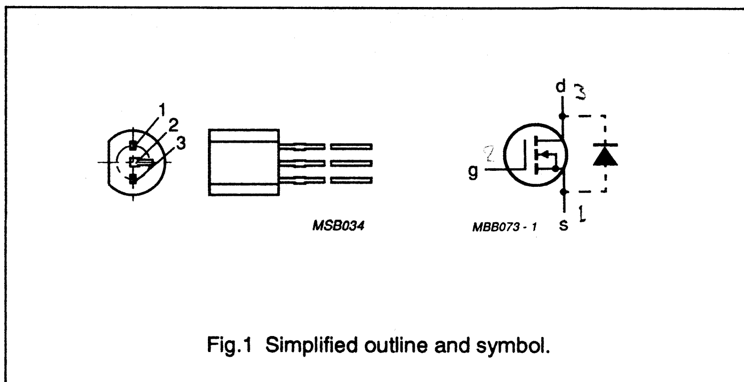


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSS100

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	250	mA
I_{DM}	drain current	peak value	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150	K/W

Note

1. Transistor mounted on a printed circuit board, maximum lead length 4 mm, mounting pad for the drain lead 10 mm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSS100

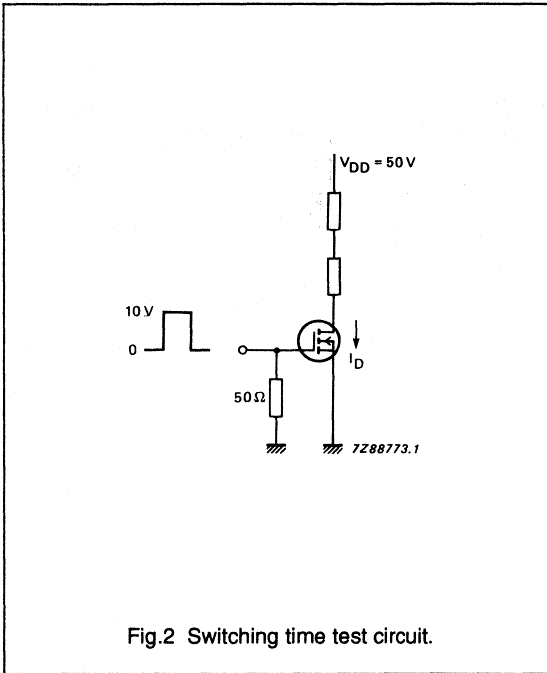


Fig.2 Switching time test circuit.

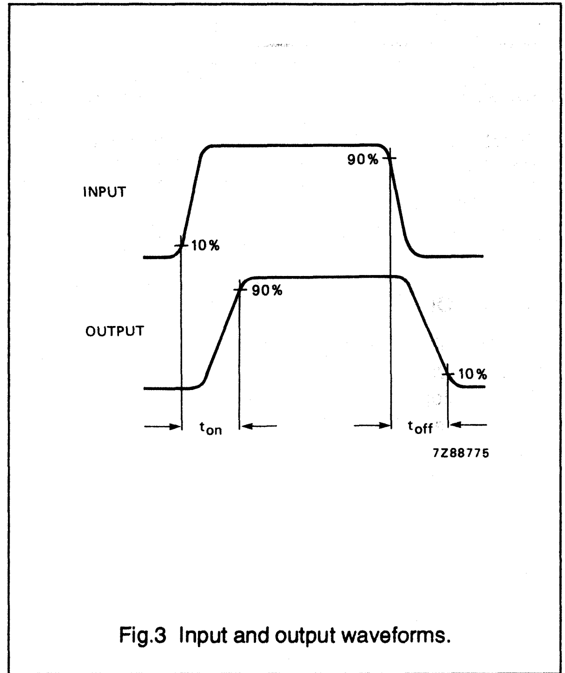


Fig.3 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

BSS123
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

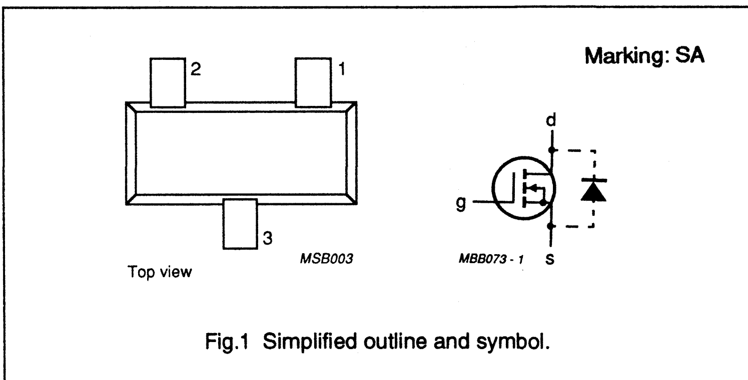


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	150	mA
I_{DM}	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on a FR4 printboard.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

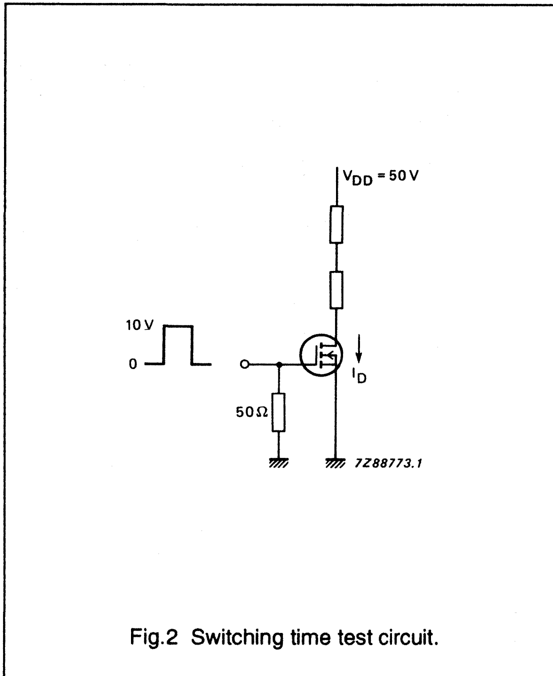


Fig.2 Switching time test circuit.

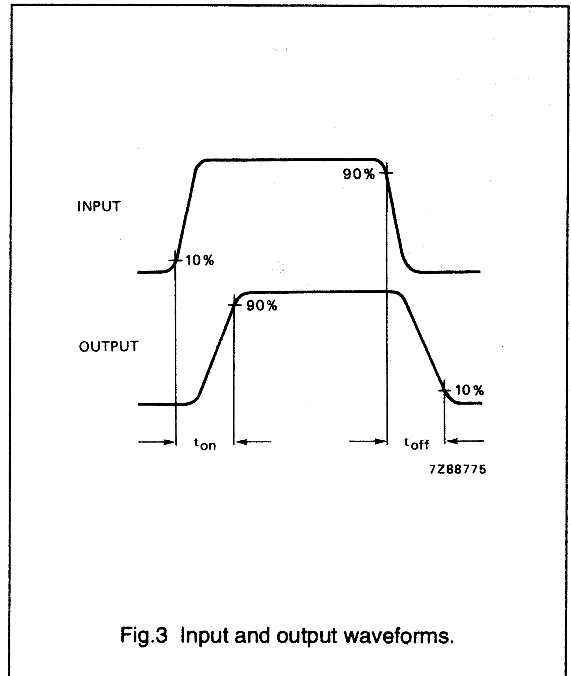


Fig.3 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

BSS131

N-channel enhancement mode vertical D-MOS FET

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	100	mA
$R_{DS(on)}$	drain-source on resistance	16	Ω
$-V_{GS(th)}$	gate-source threshold voltage	2.8	V

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

PIN CONFIGURATION

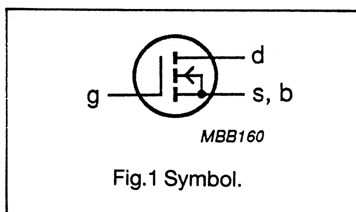


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
V_{GSO}	gate-source voltage	open drain $I_D = 0$	-	20	V
I_D	drain current	average value	-	100	mA
I_{DM}	drain current	peak value	-	400	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		−55	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient	350	K/W

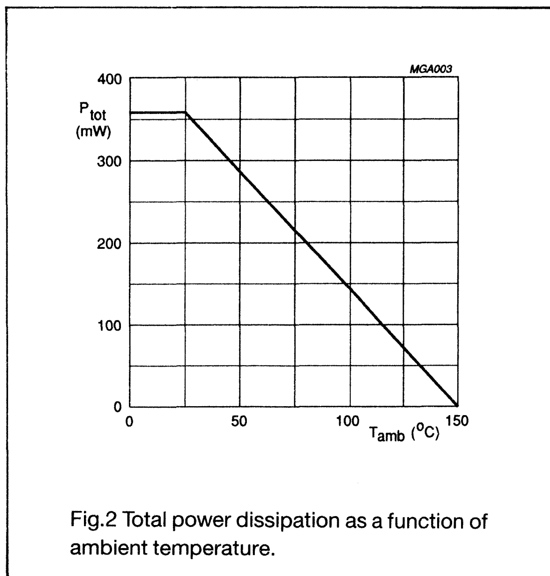


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 250 μA	240	-	-	V
I_{DSS}	drain-source leakage current	V_{GS} = 0 V_{DS} = 130 V	-	-	30	nA
		V_{GS} = 0 V_{DS} = 240 V	-	-	15	μA
		V_{GS} = 0 V_{DS} = 240 V T_j = 125 °C	-	-	60	μA
I_{GSS}	gate-source leakage current	V_{DS} = 0 V_{GS} = 20 V	-	-	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 10 V I_D = 100 mA	-	-	16	Ω
$\|Y_{fs}\|$	transfer admittance	V_{DS} = 25 V I_D = 100 mA f = 1 kHz	60	100	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	20	-	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	6	-	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	2.5	-	pF
t_{on}	turn-on time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0-5 V	-	20	-	ns
t_{off}	turn-off time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0-5 V	-	40	-	ns

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	September 1990

BSS138

N-channel enhancement mode vertical D-MOS FET

FEATURES

- Low threshold voltage
- CMOS compatible
- Low on-resistance.

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

PIN CONFIGURATION

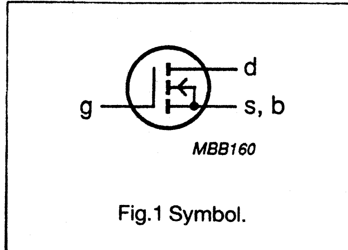


Fig.1 Symbol.

PINNING - SOT223

PIN	DESCRIPTION
1	source, substrate (b)
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	drain current	200	mA
$R_{DS(on)}$	drain-source on resistance	3.5	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.5	V

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	50	V
V_{GSO}	gate-source voltage	open drain $I_D = 0$	-	20	V
I_D	drain current	average value	-	200	mA
I_{DM}	drain current	peak value	-	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

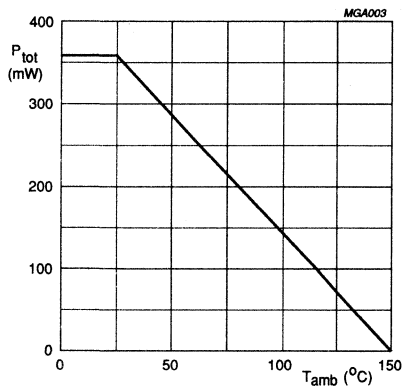


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 250 μA	50	-	-	V
I_{DSS}	drain-source leakage current	V_{GS} = 0 V_{DS} = 25 V	-	-	0.1	μA
		V_{GS} = 0 V_{DS} = 50 V	-	-	0.5	μA
		V_{GS} = 0 V_{DS} = 50 V T_j = 125 °C	-	-	5	μA
I_{GSS}	gate-source leakage current	V_{DS} = 0 V_{GS} = 20 V	-	-	0.1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.5	-	1.5	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 5 V I_D = 200 mA	-	2	3.5	Ω
$\|Y_{fs}\|$	transfer admittance	V_{DS} = 25 V I_D = 200 mA f = 1 kHz	100	200	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	40	-	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	12	-	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	5	-	pF
t_{on}	turn-on time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0/5 V	-	16	-	ns
t_{off}	turn-off time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0/5 V	-	40	-	ns

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

BSS192
P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT89 envelope, intended for use in relay, high-speed and line transformer drivers, and as a line current interruptor in telephony applications.

PINNING - SOT89

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 100$ mA $-V_{GS} = 10$ V	20	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1$ mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

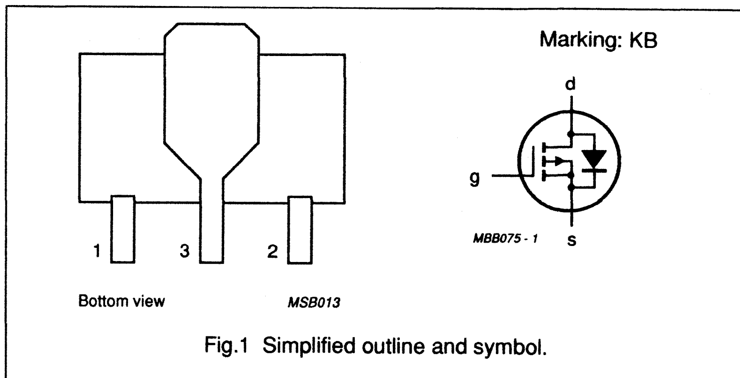


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSS192

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	150	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Transistor mounted on a ceramic substrate, area 2.5 cm^2, thickness 0.7 mm.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on a ceramic substrate, area 2.5 cm^2, thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 60 V V_{GS} = 0	–	–	0.2	μA
		$-V_{DS}$ = 200 V $-V_{GS}$ = 0.2 V	–	0.1	60	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 100 mA $-V_{GS}$ = 10 V	–	10	20	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	60	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	55	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

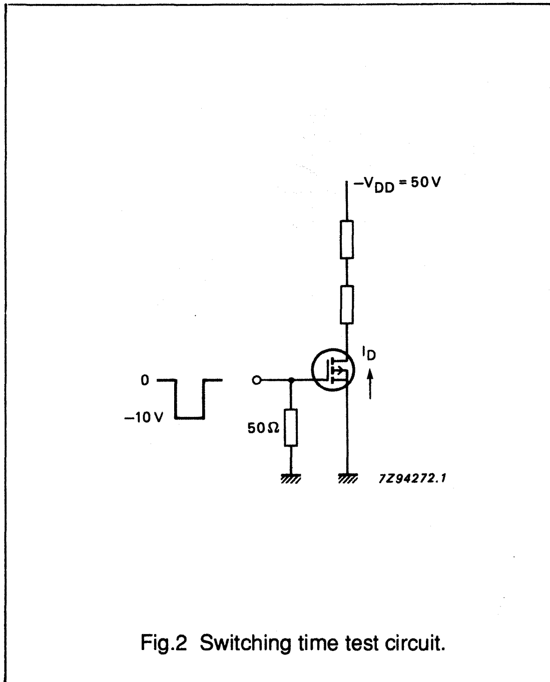


Fig.2 Switching time test circuit.

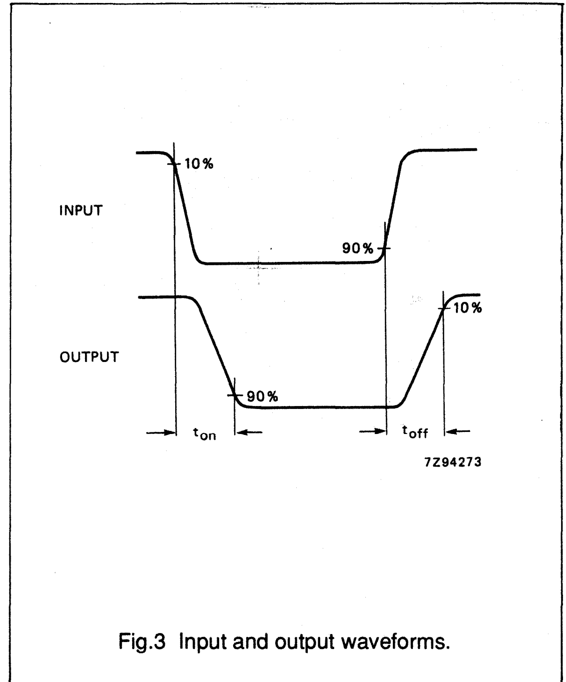


Fig.3 Input and output waveforms.

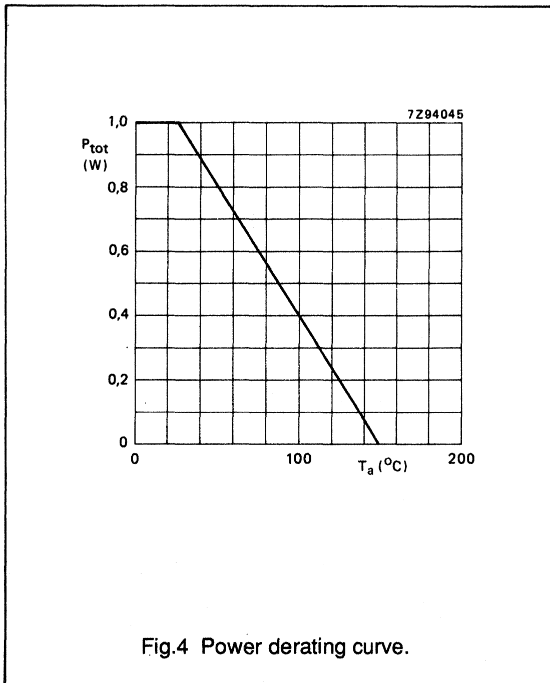


Fig.4 Power derating curve.

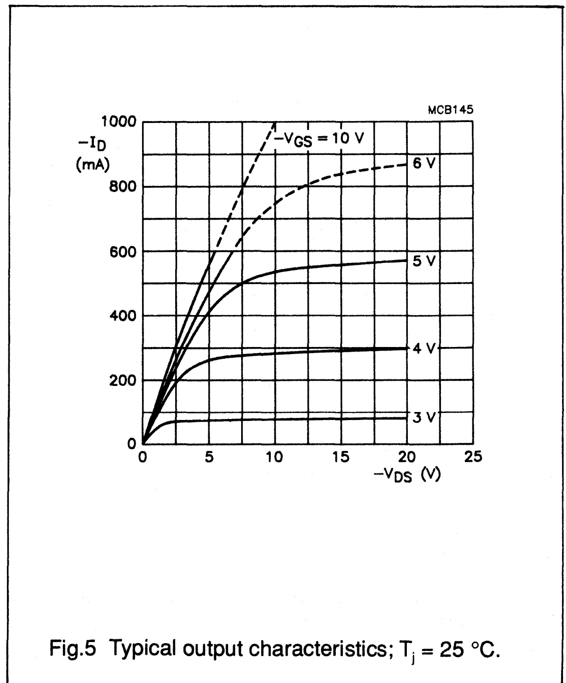


Fig.5 Typical output characteristics; T_j = 25 °C.

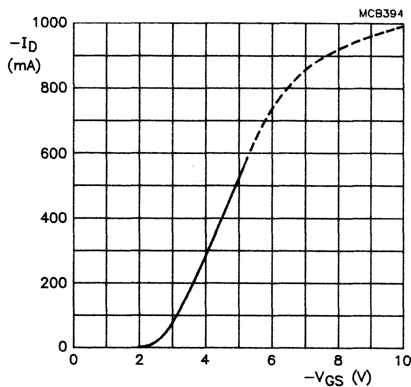


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

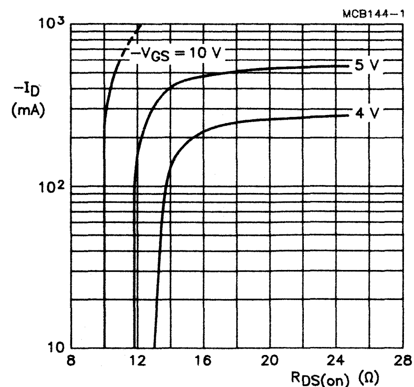


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

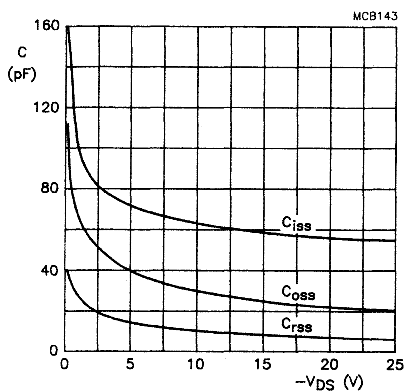


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

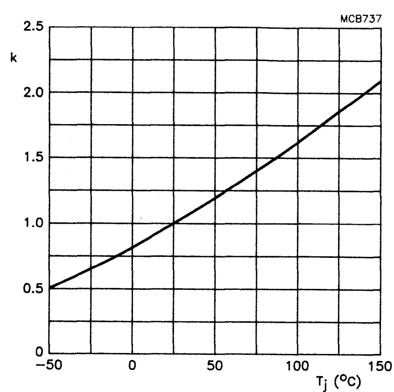


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

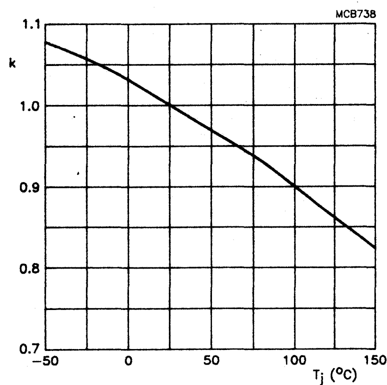


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2 4	Ω Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	typ.	300	mS

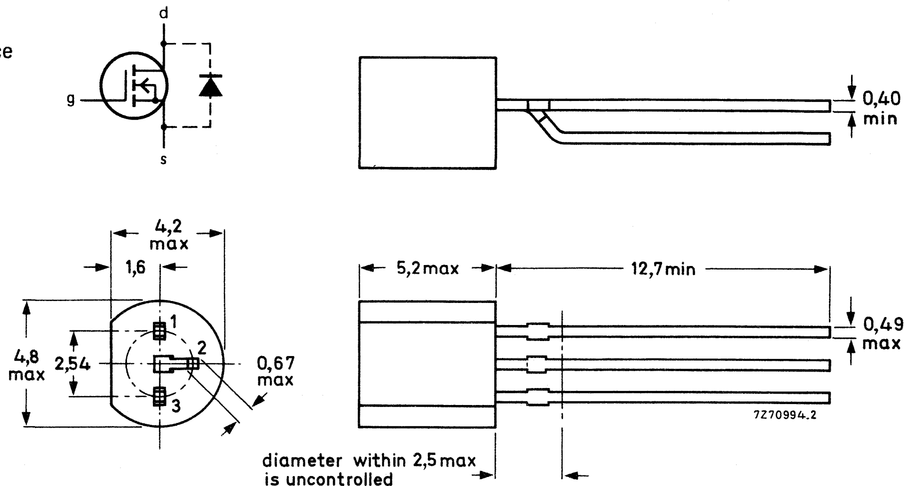
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Drain current (peak)	I_{DM}	max.	1.0	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 µA; V_{GS} = 0	$V_{(BR)DS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1	µA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance (see Fig. 4) I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 3.0	Ω Ω
Transfer admittance at f = 1 kHz I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs}\rvert$	typ.	300	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. max.	45 60	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 15	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

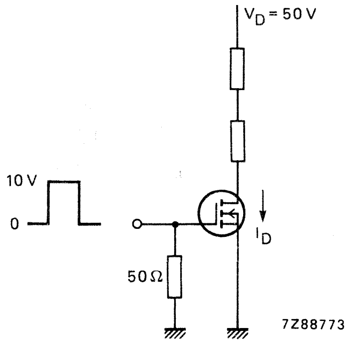


Fig. 2 Switching times test circuit.

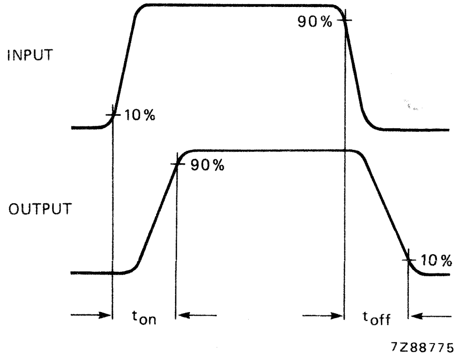


Fig. 3 Input and output waveforms.

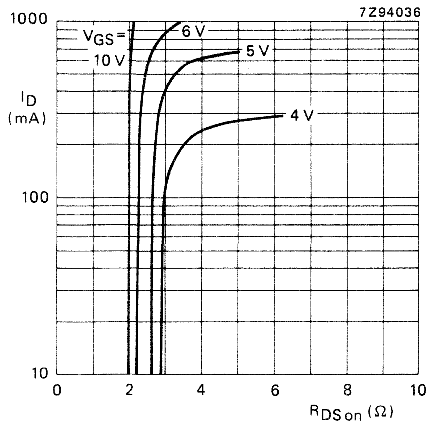


Fig. 4 T_j = 25 °C; typical values.

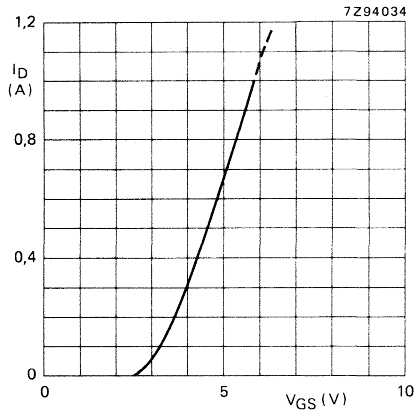


Fig. 5 T_j = 25 °C; typical values at V_{DS} = 10 V.

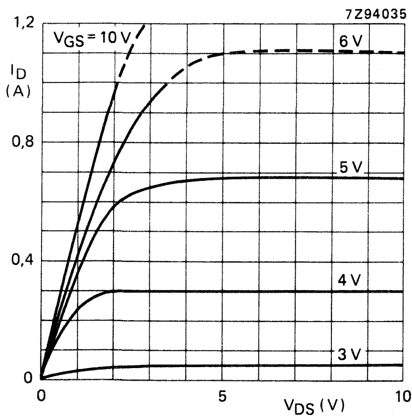


Fig. 6 T_j = 25 °C; typical values.

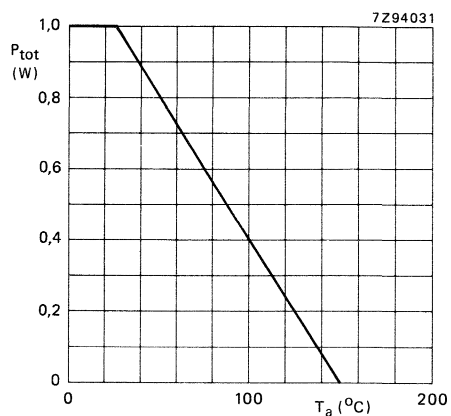


Fig. 7 Power derating curve.

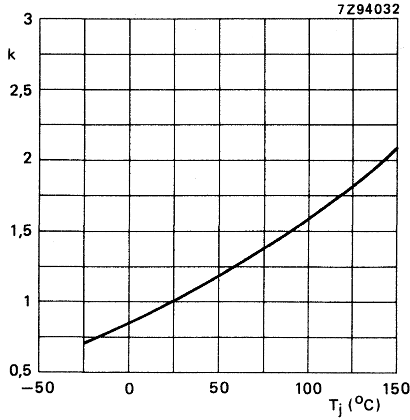


Fig. 8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{\circ}C}$; typ. values at 500 mA/10 V.

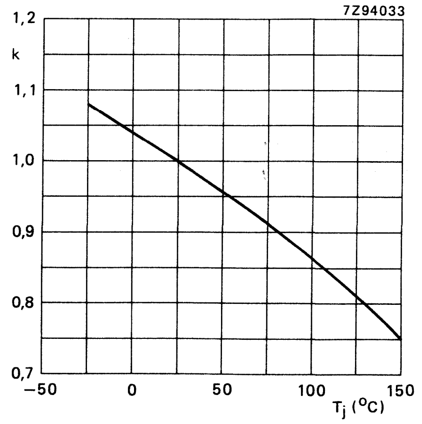


Fig. 9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{\circ}C}$; $V_{GS(th)}$ at 1 mA; typical values.

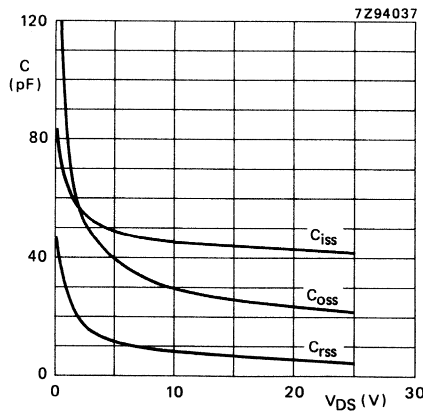


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	0.83	W
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ.	7	Ω
		max.	10	Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	150	mS

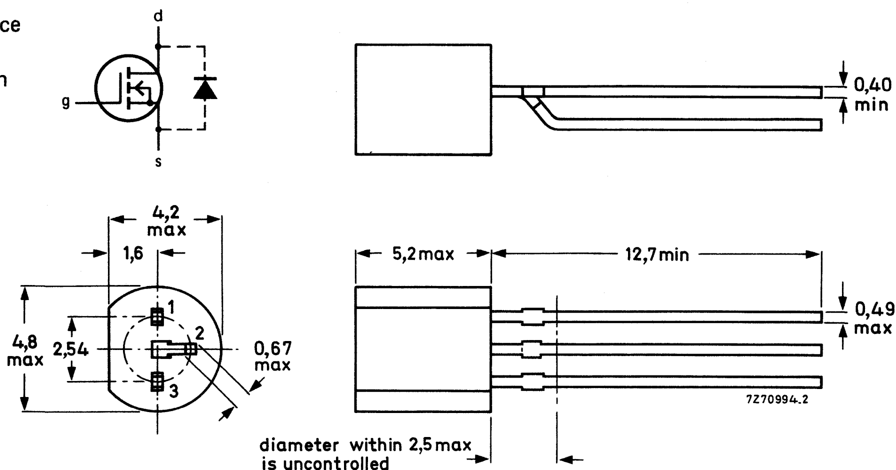
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $I_D = 10\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	min.	80	V
Drain-source leakage current $V_{DS} = 60$ V; $V_{GS} = 0$	I_{DSS}	max.	1.0	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	max.	100	nA
Gate threshold voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance (see Fig. 4) $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance at f = 1 kHz $I_D = 200$ mA; $V_{DS} = 5$ V	$\lvert y_{fs} \rvert$	typ.	150	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. max.	15 30	pF pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. max.	13 20	pF pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. max.	3 6	pF pF
Switching times (see Figs 2 and 3) $I_D = 200$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	4 10	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

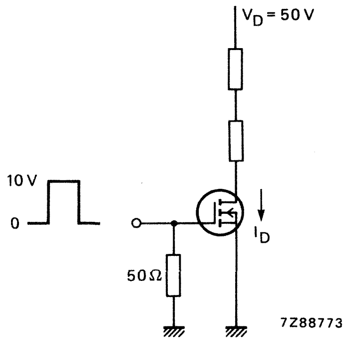


Fig. 2 Switching times test circuit.

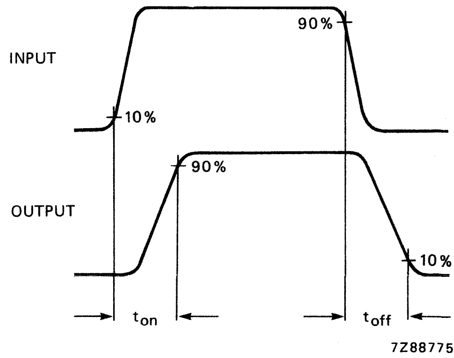


Fig. 3 Input and output waveforms.

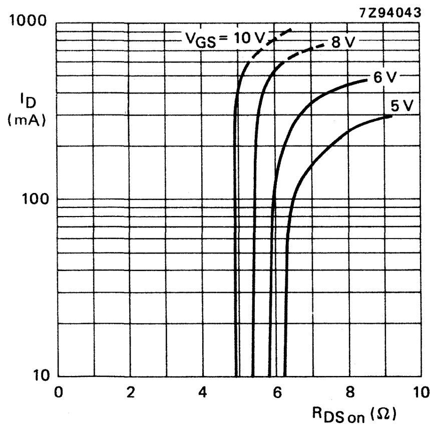


Fig. 4 T_j = 25 °C; typical values.

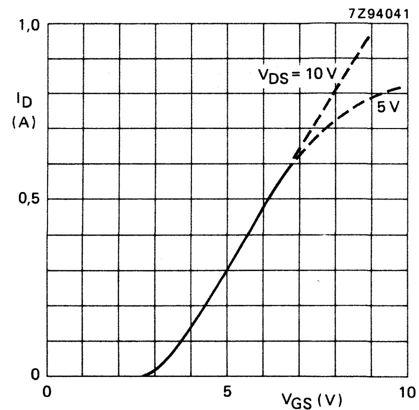


Fig. 5 T_j = 25 °C; typical values.

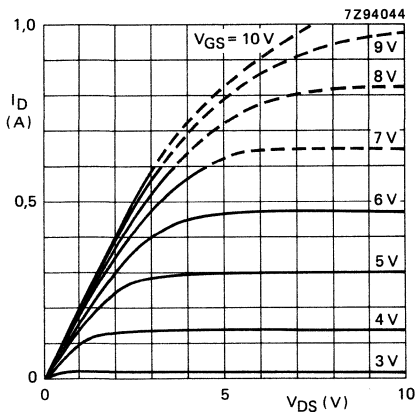


Fig. 6 T_j = 25 °C; typical values.

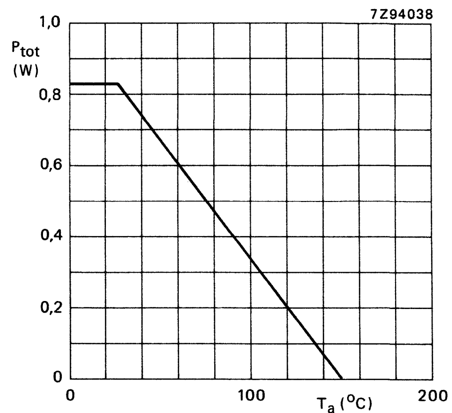


Fig. 7 Power derating curve.

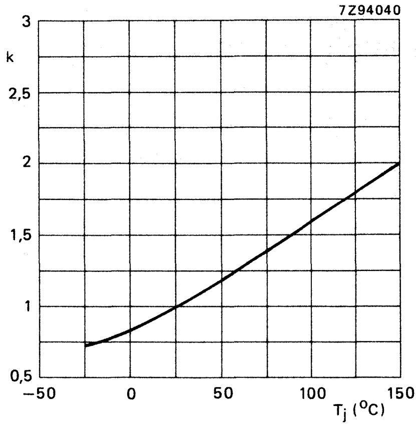


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typ. values at 150 mA/5 V.

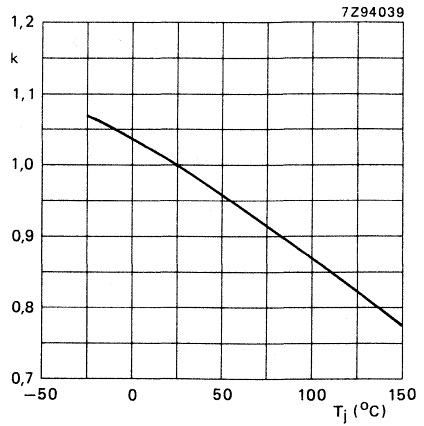


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

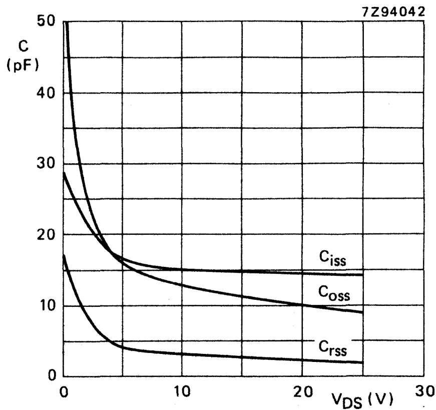


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	typ.	250 mS

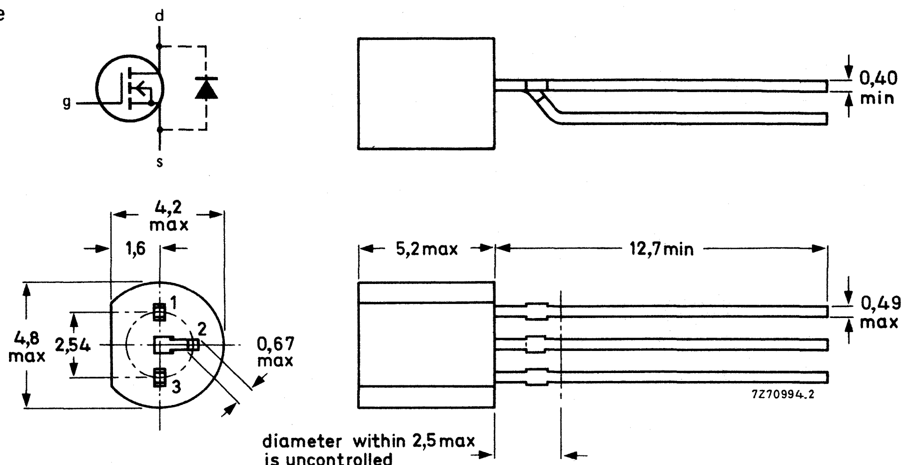
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

Parameter	Symbol		Value
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value
Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance (see Fig. 4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance at f = 1 kHz I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. max.	70 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 10 ns
	t_{off}	typ. max.	15 ns 25 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

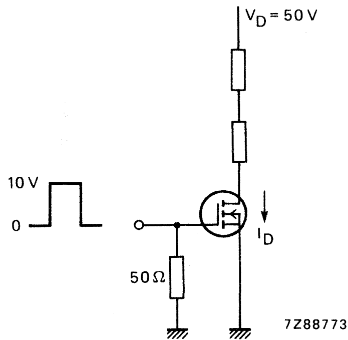


Fig. 2 Switching times test circuit.

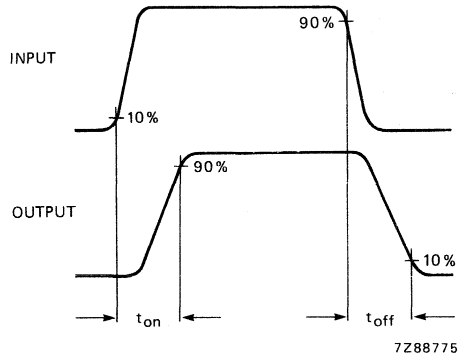


Fig. 3 Input and output waveforms.

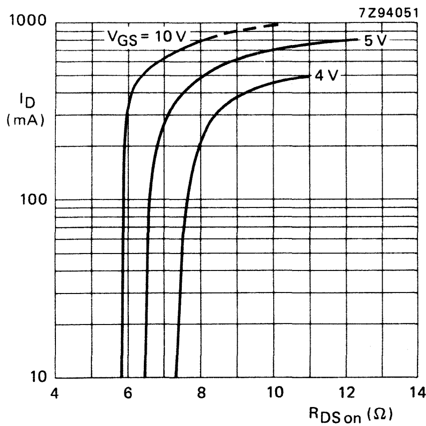


Fig. 4 T_j = 25 °C; typical values.

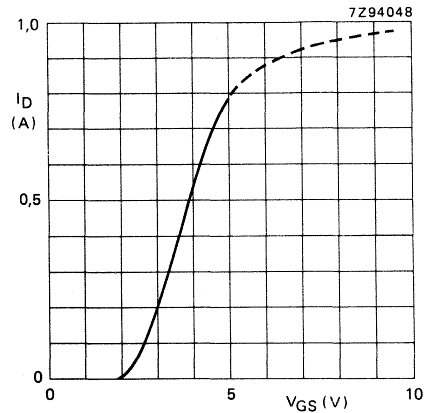


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

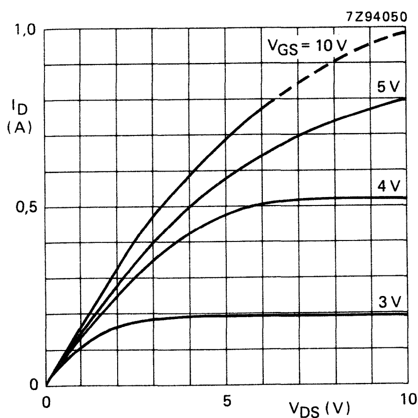


Fig. 6 T_j = 25 °C; typical values.

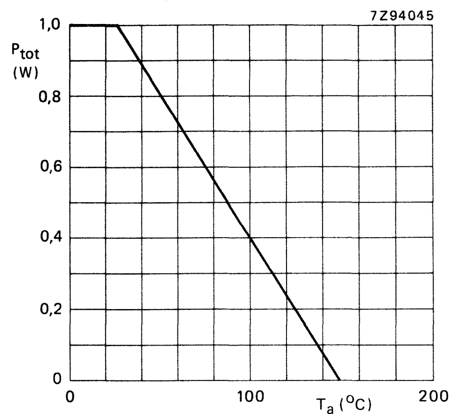


Fig. 7 Power derating curve.

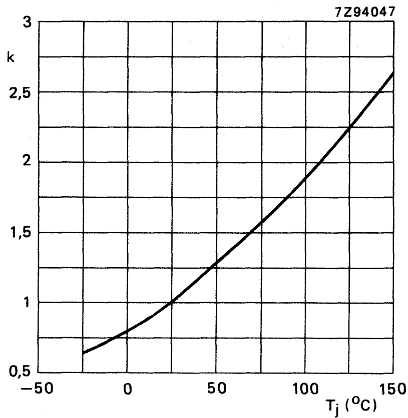


Fig. 8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^oC}$; at 400 mA/10 V; typical values.

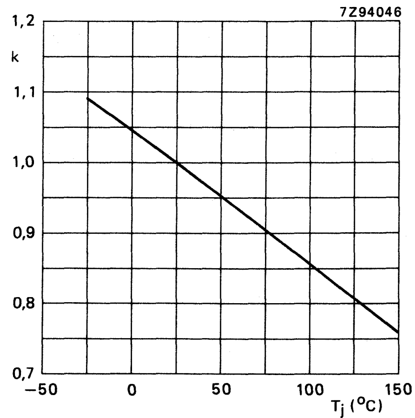


Fig. 9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

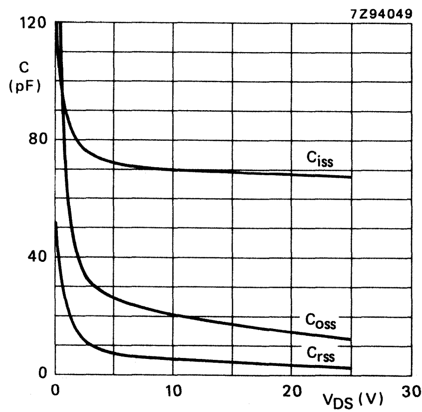


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ.	7 Ω
		max.	10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	250 mS

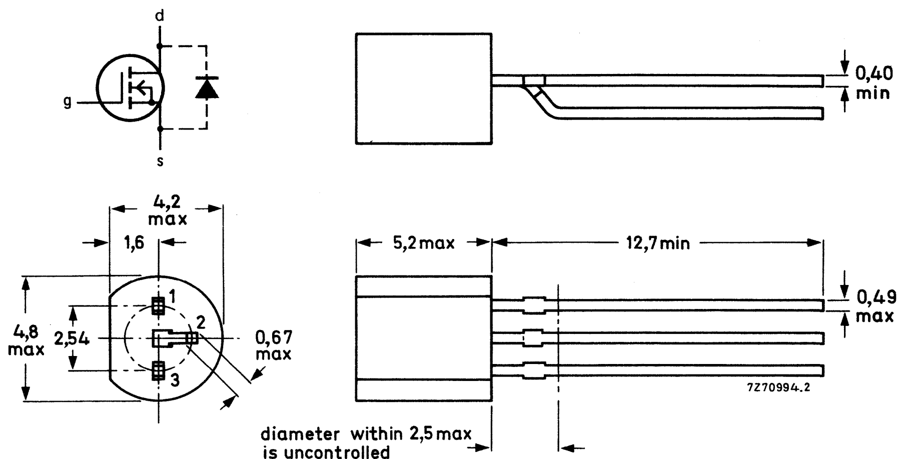
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	180	V
Drain-source leakage current V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.7 2.4	V V
Drain-source ON-resistance (see Fig. 4) I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 10	Ω Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6	Ω
Transfer admittance at f = 1 kHz I_D = 300 mA; V_{DS} = 15 V	$\|y_{fs}\|$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. max.	50 65	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. max.	6 10	pF pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 15	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

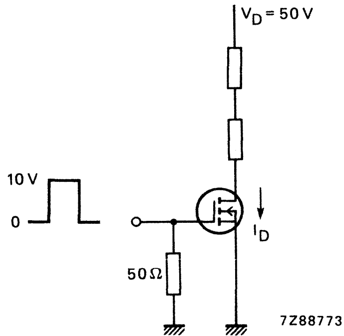


Fig. 2 Switching times test circuit.

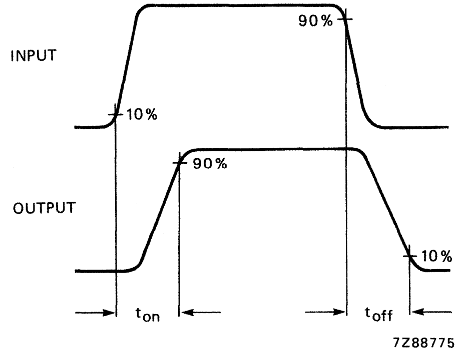


Fig. 3 Input and output waveforms.

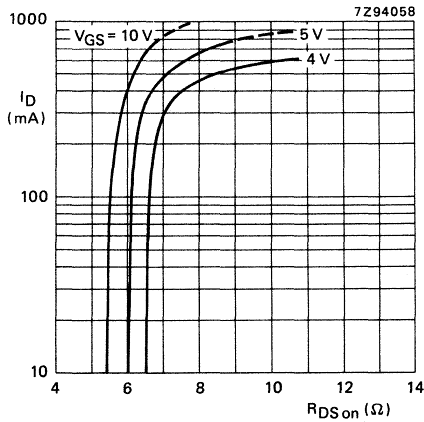


Fig. 4 $T_j = 25\,^oC$; typical values.

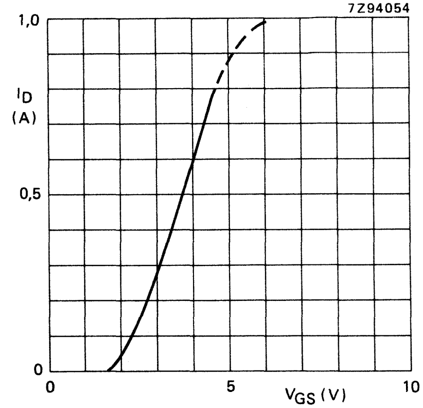


Fig. 5 $T_j = 25\,^oC$; $V_{DS} = 10\,V$; typ. values.

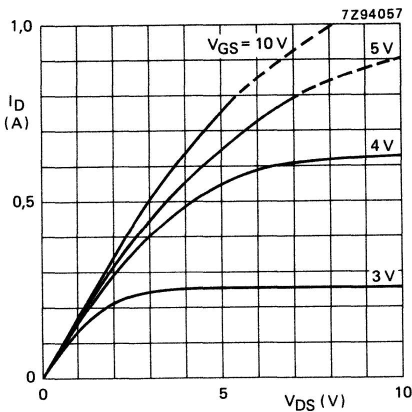


Fig. 6 $T_j = 25\,^oC$; typical values.

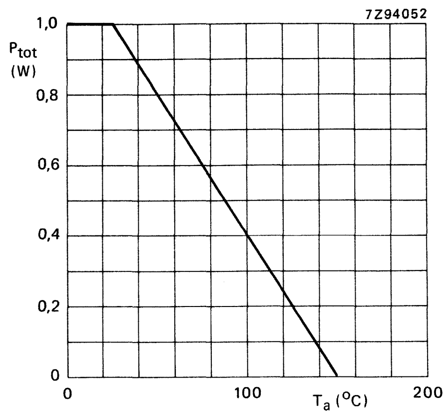


Fig. 7 Power derating curve.

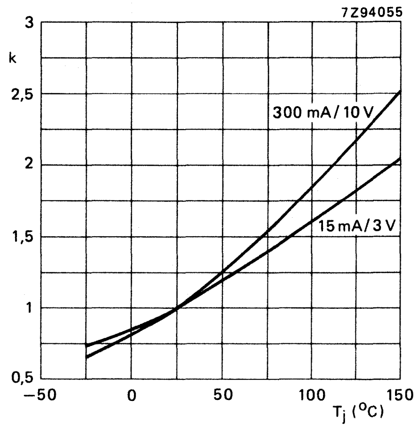


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typical values.

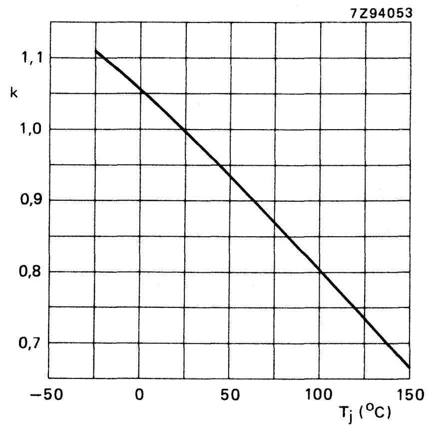


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 0,1 mA; typical values.

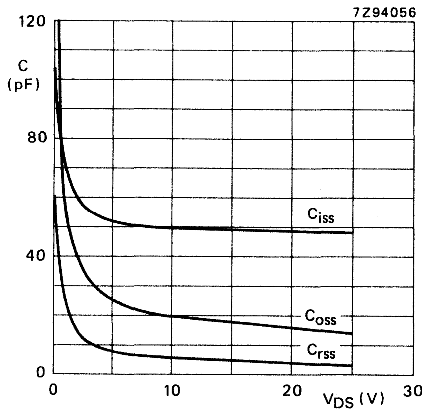


Fig. 10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

HIGH-VOLTAGE N-CHANNEL VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	450	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,75	A
Total power dissipation up to T_{mb} = 75 °C	P_{tot}	max.	15	W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ.	15	Ω
Transfer admittance I_D = 250 mA; V_{DS} = 20 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	400	mS

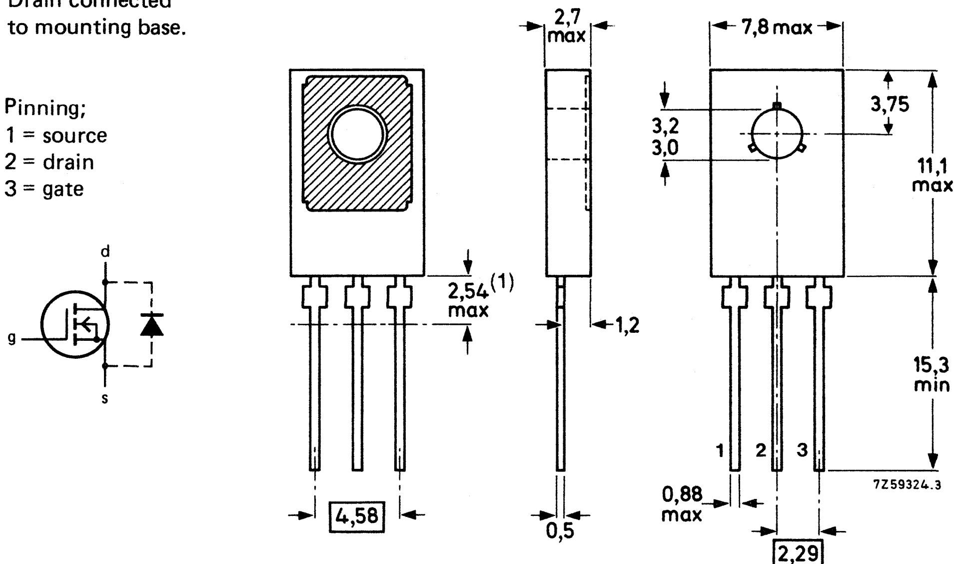
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126.

Drain connected to mounting base.

Pinning;
1 = source
2 = drain
3 = gate



(1) Lead dimensions uncontrolled under this zone

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	450	V
Drain-source voltage (non-repetitive peak; $t_p \leq 50\ \mu s$)	$V_{DS(SM)}$	max.	525	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,75	A
Drain current (peak)	I_{DM}	max.	1,5	A
Total power dissipation up to T_{mb} = 75 °C	P_{tot}	max.	15	W
Storage temperature	T_{stg}	−65 to	+150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
From junction to ambient	$R_{th\ j\text{-}a}$	100	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	450	V
Drain-source leakage current V_{DS} = 350 V; V_{GS} = 0	I_{DSS}	<	25	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100	nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	>	2,0	V
		<	4,0	V
Drain-source ON-resistance (see Fig. 4) I_D = 100 mA; V_{GS} = 10 V	R_{DSon}	typ.	10	Ω
		<	14	Ω
I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ.	15	Ω
Transfer admittance at f = 1 kHz I_D = 250 mA; V_{DS} = 20 V	$\lvert y_{fs} \rvert$	typ.	400	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ.	75	pF
		<	100	pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ.	25	pF
		<	35	pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	3	pF
		<	5	pF
Switching times (see Figs 2 and 3) I_D = 100 mA; V_{DS} = 200 V; V_{GS} = 0 to 10 V	t_{on}	<	10	ns
	t_{off}	<	100	ns

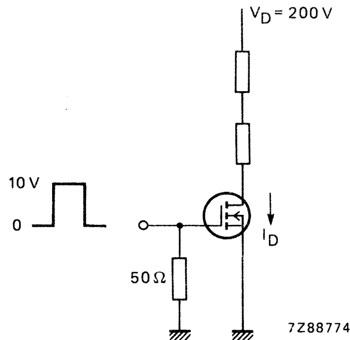


Fig. 2 Switching times test circuit.

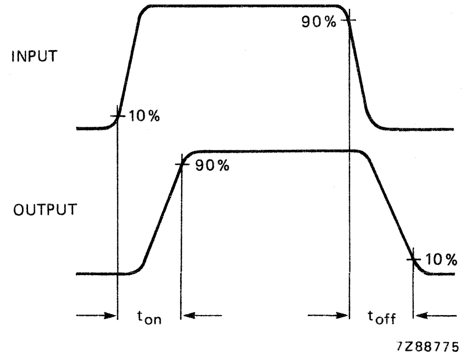


Fig. 3 Input and output waveforms.

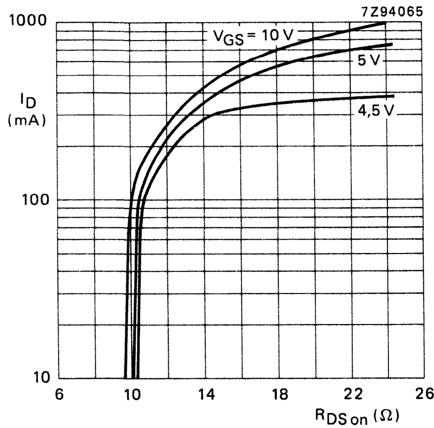


Fig. 4 T_j = 25 °C; typical values.

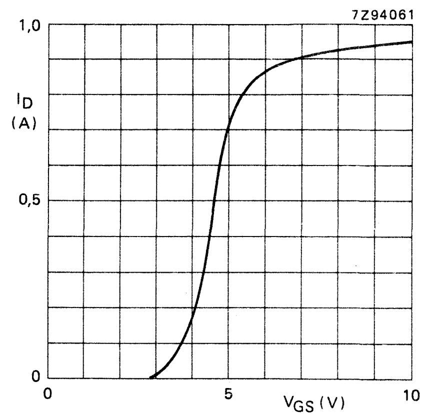


Fig. 5 T_j = 25 °C; V_{DS} = 20 V; typical values.

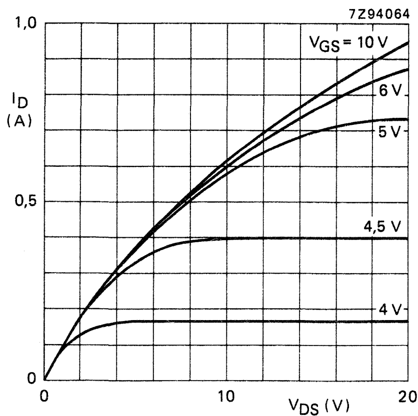


Fig. 6 T_j = 25 °C; typical values.

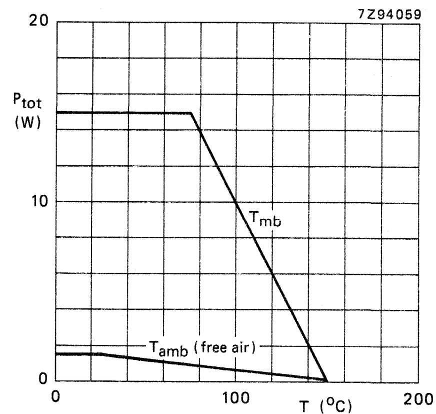


Fig. 7 Power derating curve.

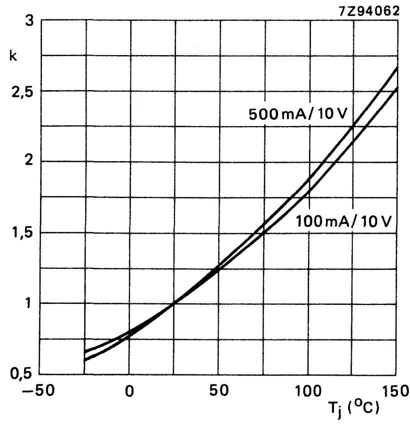


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typical values.

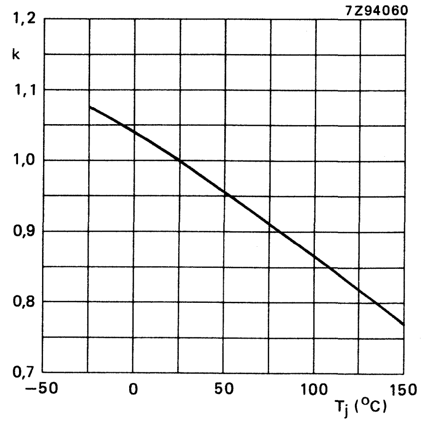


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

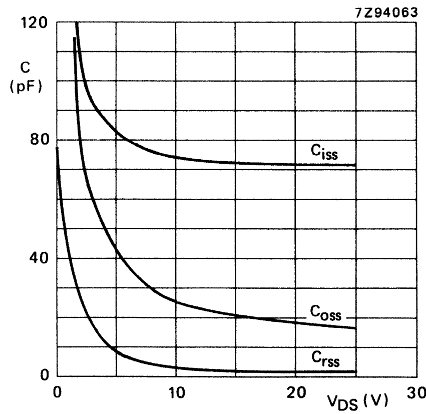


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Low $R_{DS\,on}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ.	2.0	Ω
		max.	4.0	Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300	mS

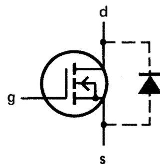
MECHANICAL DATA

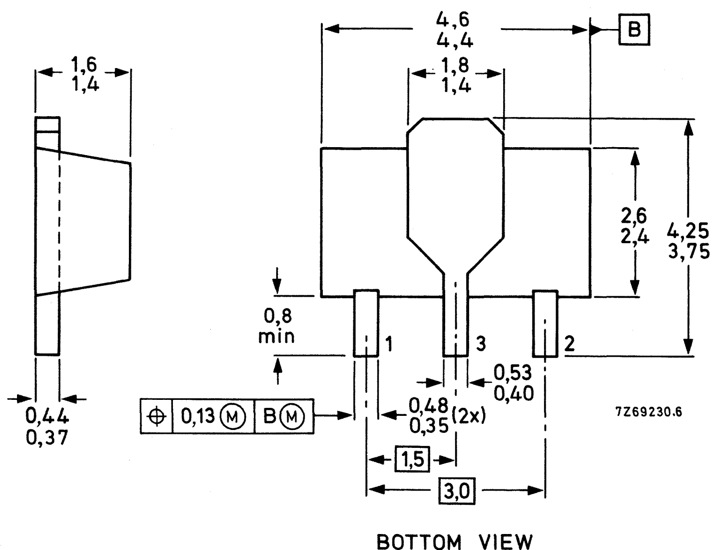
Dimensions in mm

Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain





Marking: KM

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Drain current (peak)	I_{DM}	max.	1.0	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to	+ 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 µA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1	µA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 3.0	Ω Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 60	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD}= 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 15	ns ns

Note

1. Transistors mounted on a substrate with surface area of 2.5 cm^2 and thickness of 0.7 mm.

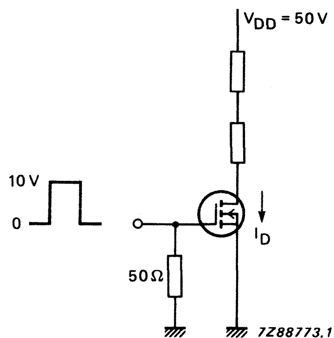


Fig.2 Switching times test circuit.

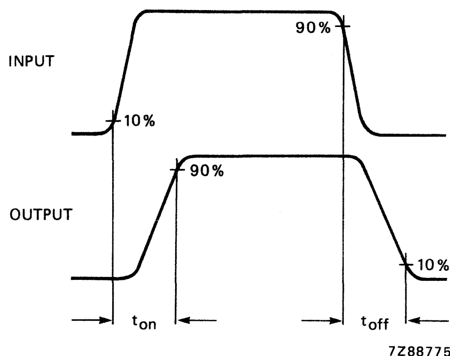


Fig.3 Input and output waveforms.

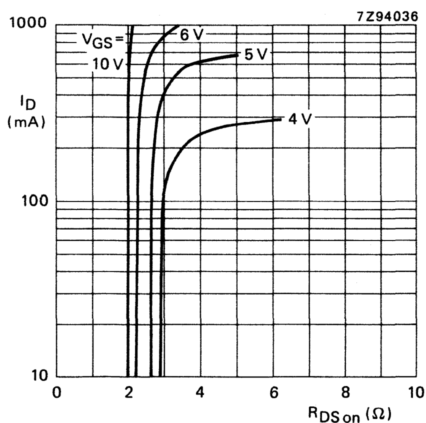


Fig.4 T_j = 25 °C; typical values.

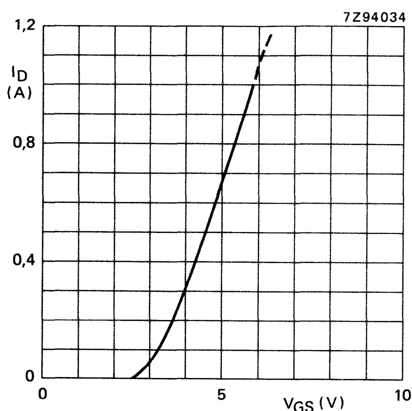


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

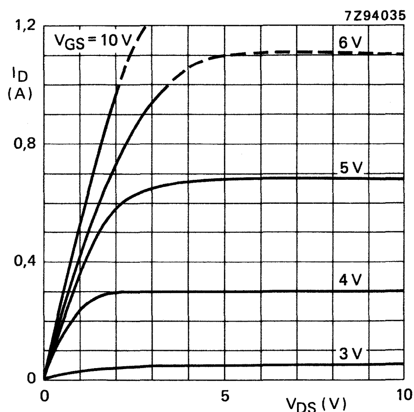


Fig.6 T_j = 25 °C; typical values.

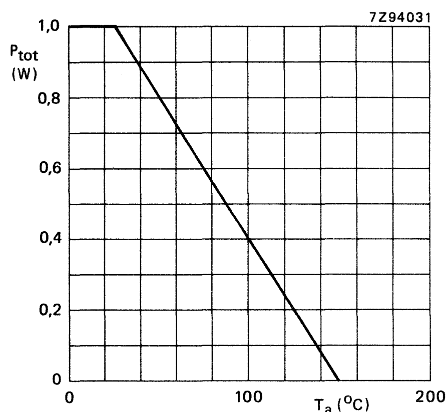


Fig.7 Power derating curve.

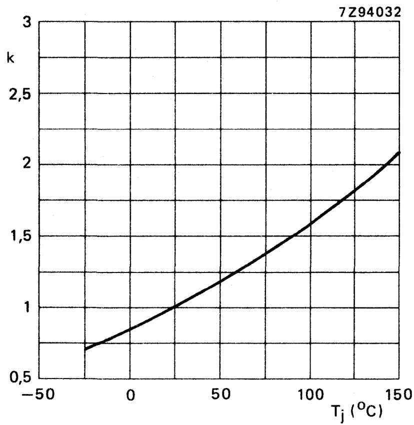


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{o}C}$; typ. values.
at 500 mA/10 V.

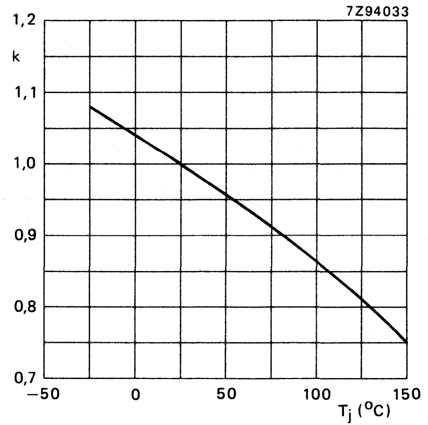


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

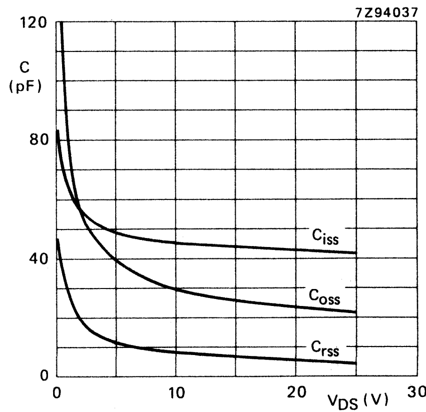


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ.	7	Ω
		max.	10	Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\|y_{fs}\|$	typ.	150	mS

MECHANICAL DATA

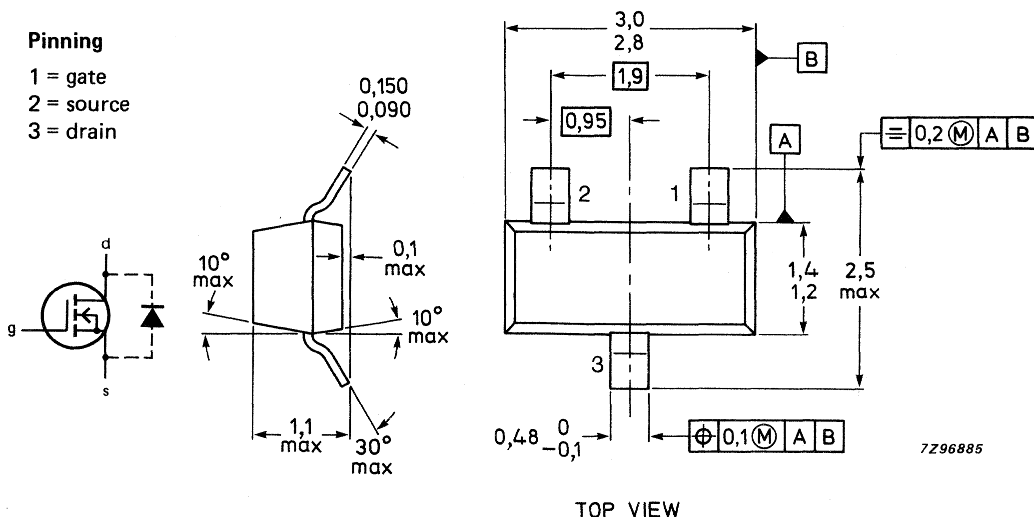
Dimensions in mm

Fig.1 SOT23.

Marking: 02p

Pinning

1 = gate
2 = source
3 = drain



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to	+ 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\|y_{fs}\|$	typ.	150	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 30	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 20	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 6	pF pF
Switching times (see Figs 2 and 3) I_D = 175 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	4 10	ns ns

Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

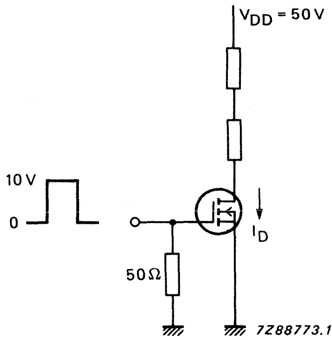


Fig.2 Switching times test circuit.

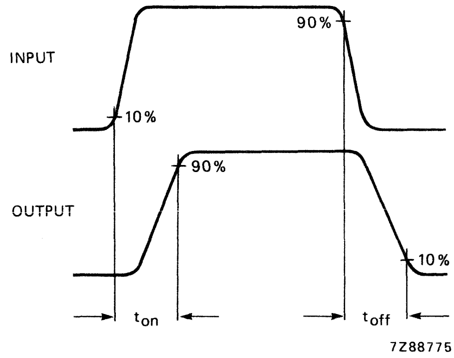


Fig.3 Input and output waveforms.

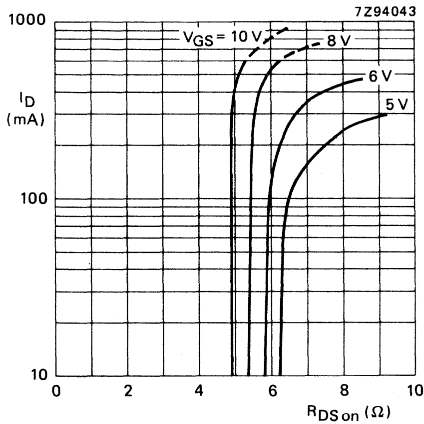


Fig.4 T_j = 25 °C; typical values.

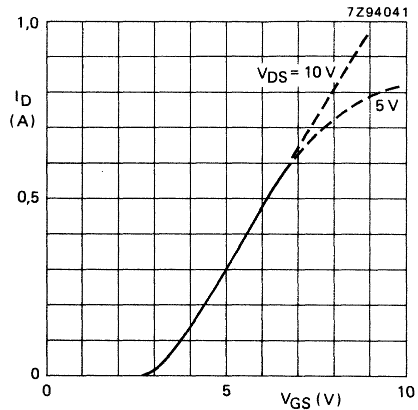


Fig.5 T_j = 25 °C; typical values.

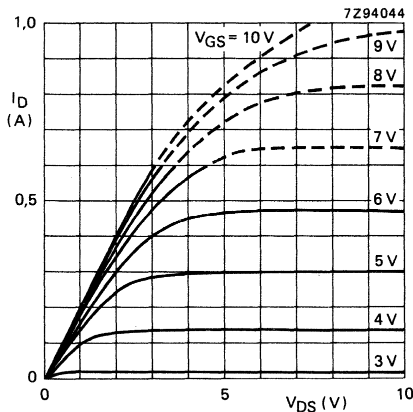


Fig.6 T_j = 25 °C; typical values.

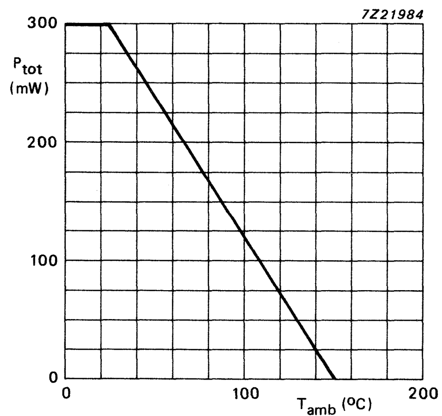


Fig.7 Power derating curve.

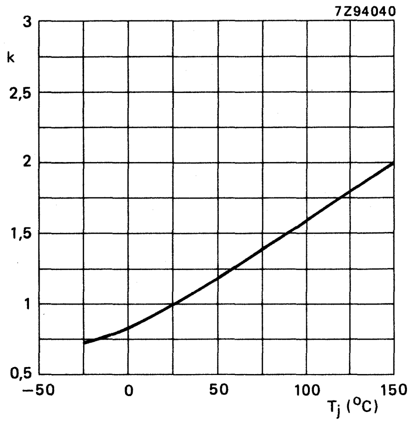


Fig.8 $k = \frac{R_{DS\,on} \text{ at } T_j}{R_{DS\,on} \text{ at } 25\,^{o}C}$; typ. values at 150 mA/5 V.

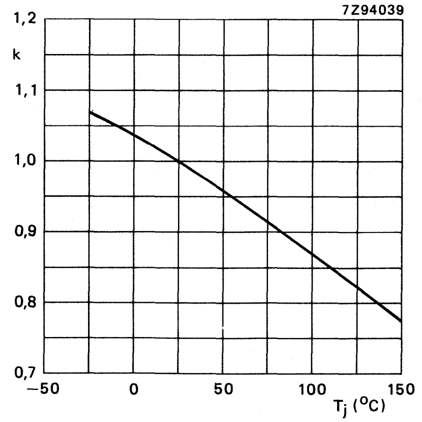


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

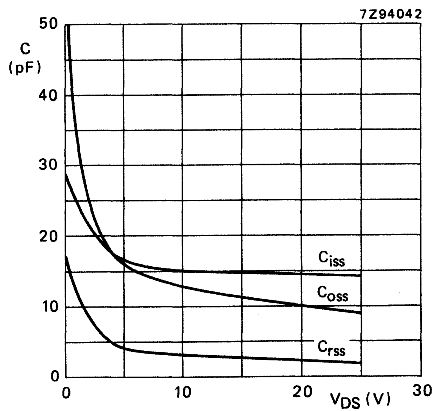


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

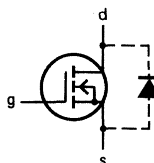
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ.	6	Ω
		max.	12	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS

MECHANICAL DATA

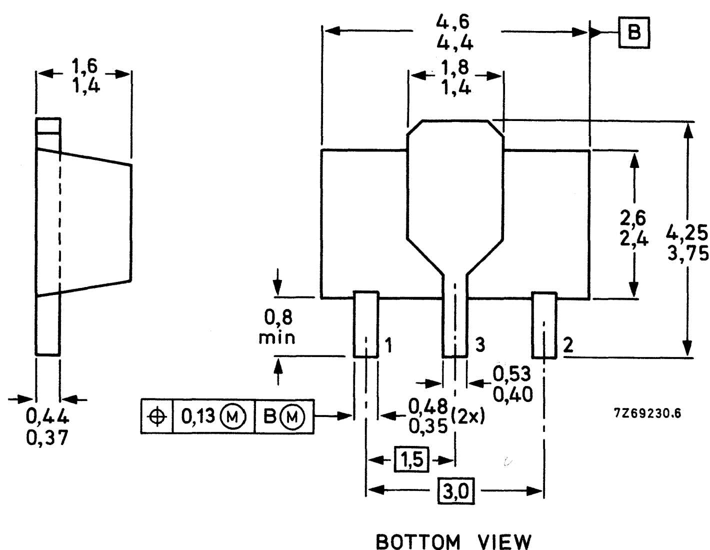
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



Marking: KN



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to	+ 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 12	Ω Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\|y_{fs}\|$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	70 90	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	15 25	ns ns

Note

1. Transistor mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

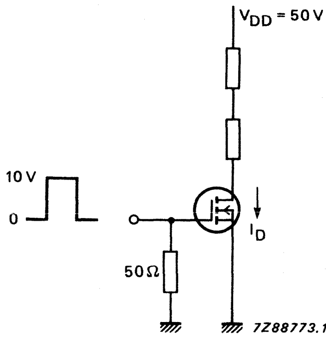


Fig. 2 Switching times test circuit.

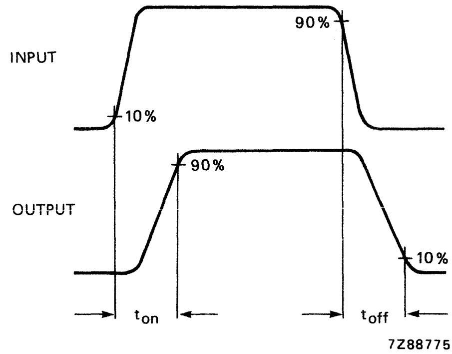


Fig. 3 Input and output waveforms.

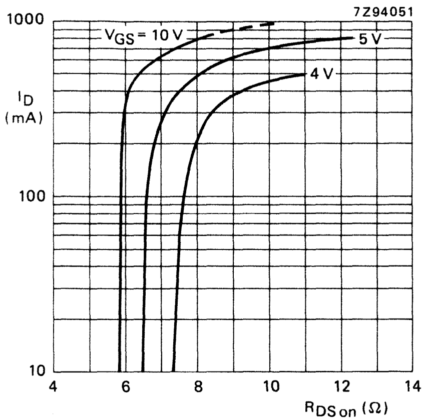


Fig. 4 T_j = 25 °C; typical values.

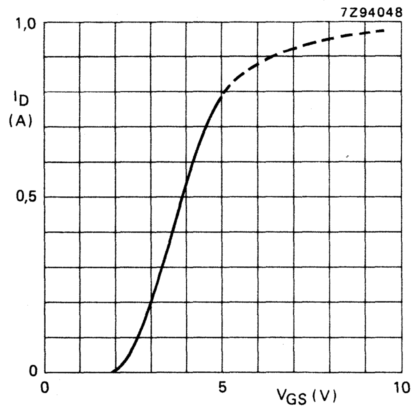


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

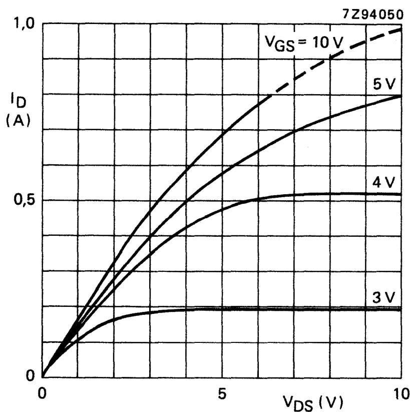


Fig. 6 T_j = 25 °C; typical values.

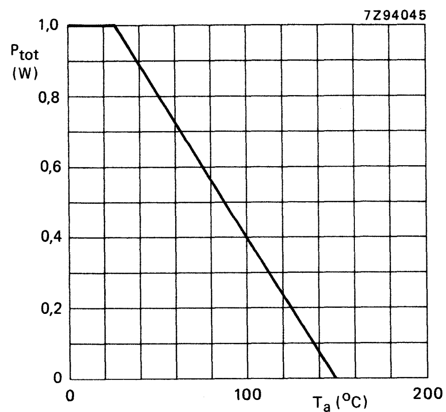


Fig. 7 Power derating curve.

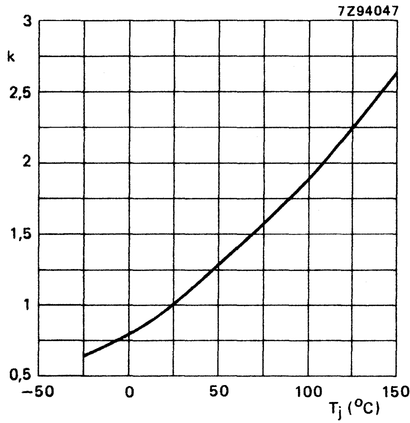


Fig. 8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\ ^oC}$; at 400 mA/10 V; typical values.

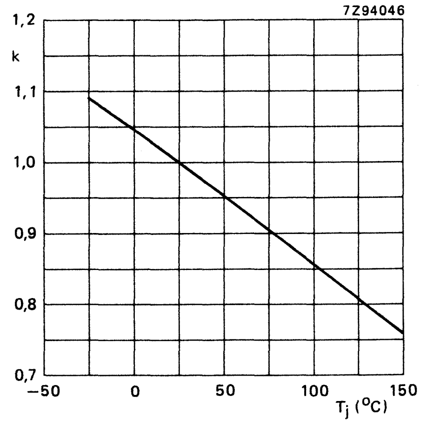


Fig. 9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

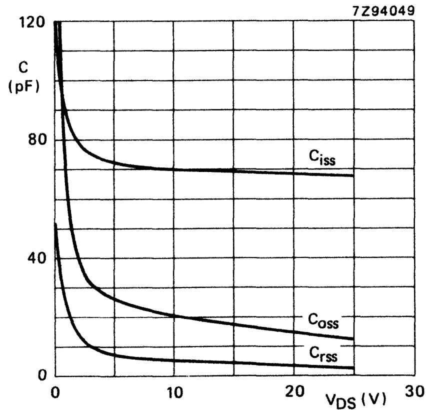


Fig. 10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ.	7	Ω
		max.	10	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS

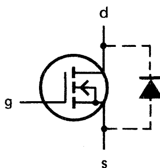
MECHANICAL DATA

Dimensions in mm

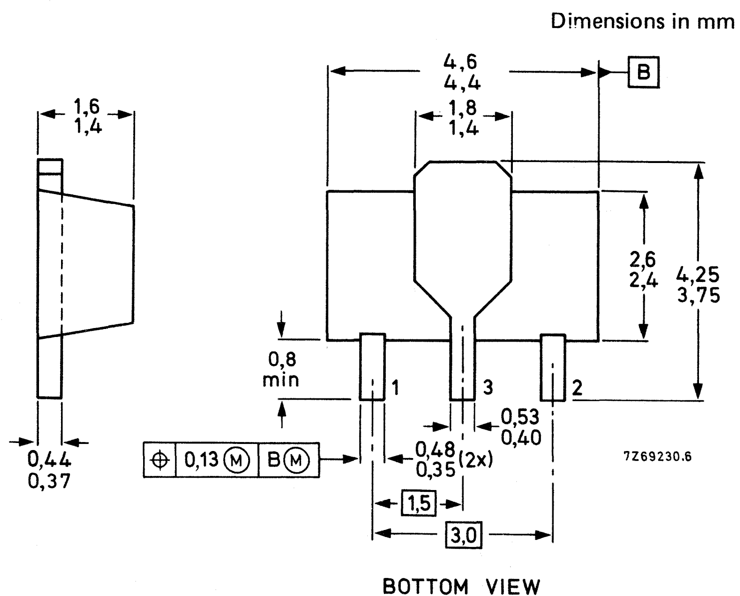
Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain



Marking: K0



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180	V
Drain-source leakage current V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.7 2.7	V V
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 10	Ω Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	50 65	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	6 10	pF pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 15	ns ns

1. Transistors mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

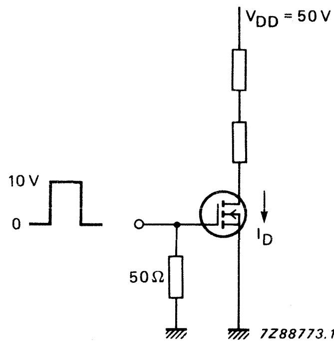


Fig.2 Switching times test circuit.

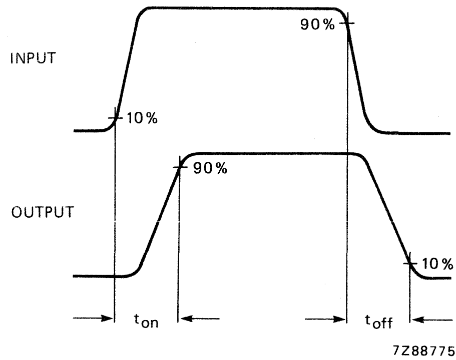


Fig.3 Input and output waveforms.

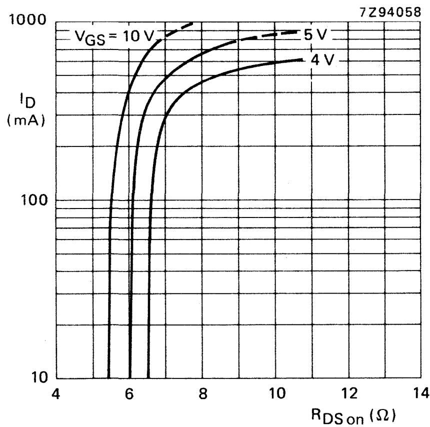


Fig.4 T_j = 25 °C; typical values.

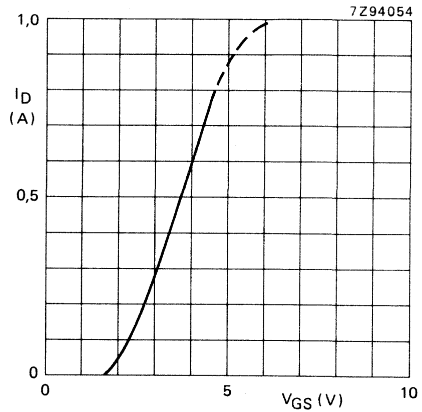


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

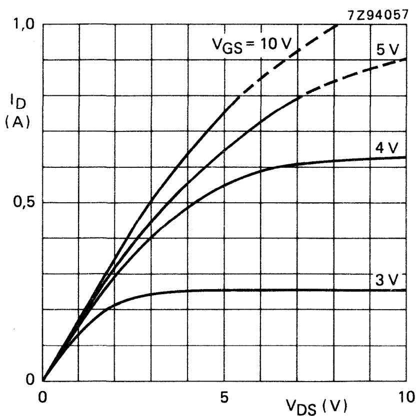


Fig.6 T_j = 25 °C; typical values.

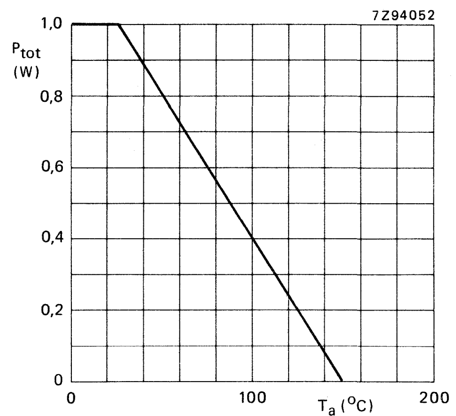


Fig.7 Power derating curve.

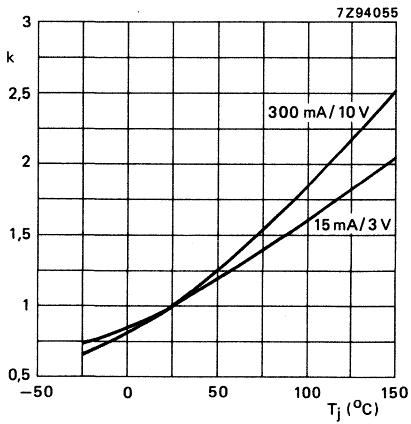


Fig.8 $k = \frac{R_{DS\,on} \text{ at } T_j}{R_{DS\,on} \text{ at } 25\ ^\circ C}$; typical values.

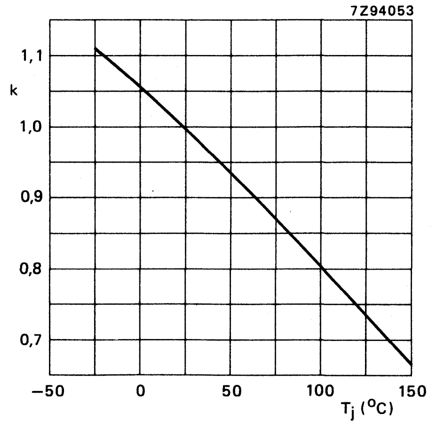


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^\circ C}$; $V_{GS(th)}$ at 0.1 mA; typical values.

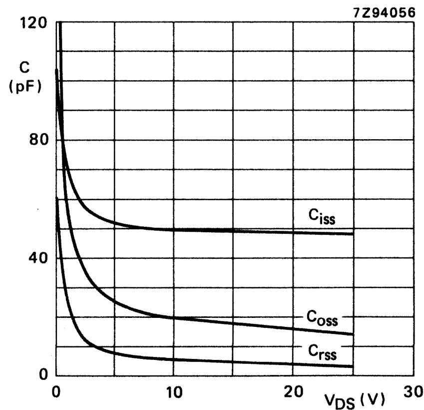


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS

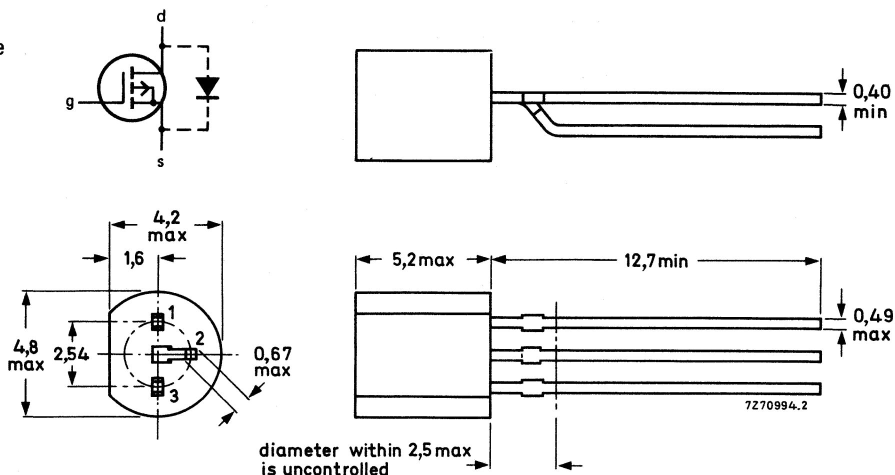
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 µA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1 µA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; $V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|y_{fs}\|$	typ.	200 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 20 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

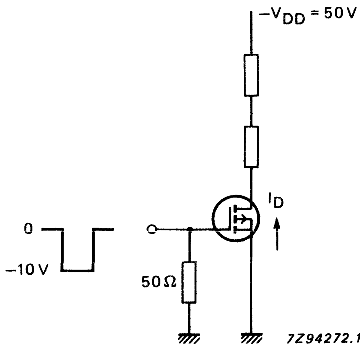


Fig.2 Switching times test circuit.

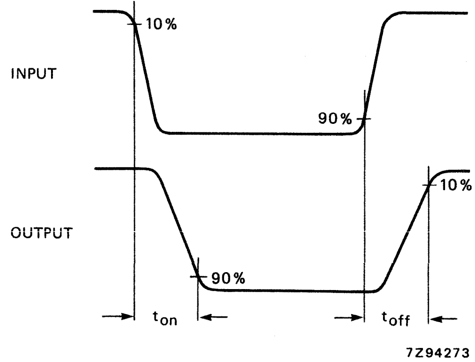


Fig.3 Input and output waveforms.

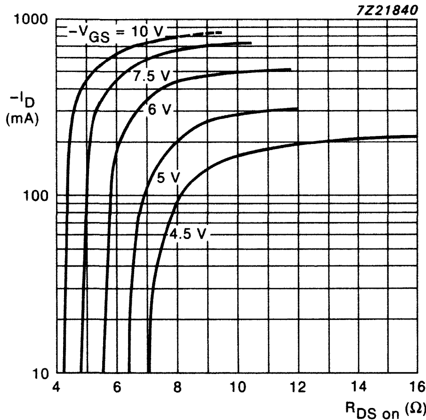


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

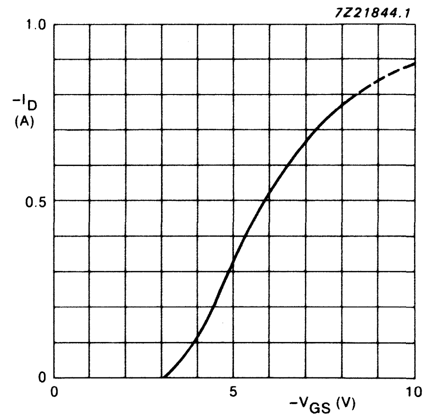


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

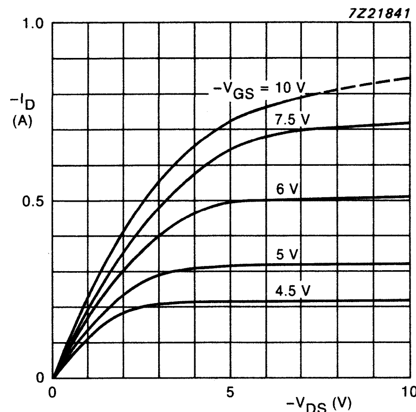


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENCHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ.	7.5	Ω
		max.	10	Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125	mS

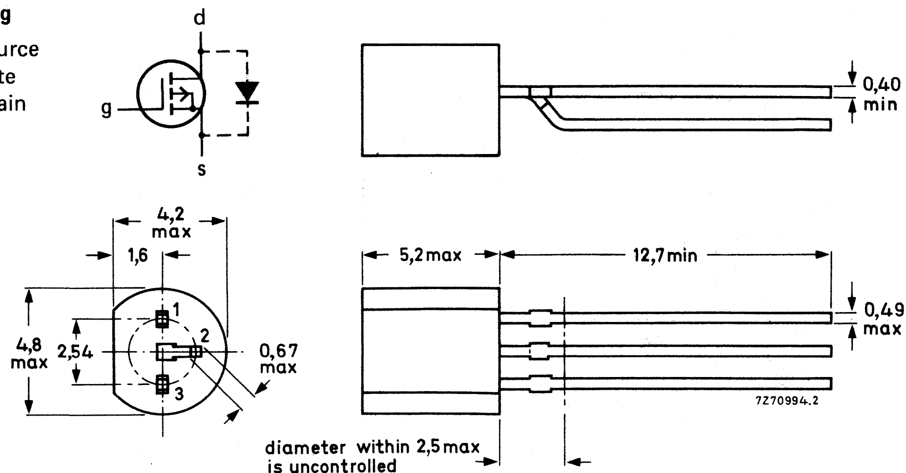
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Drain current (peak)	$-I_{DM}$	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 µA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	µA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; $V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	7.5 10	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|y_{fs}\|$	typ.	125	mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max	30 45	pF pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max	20 30	pF pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max	5 10	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 10	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

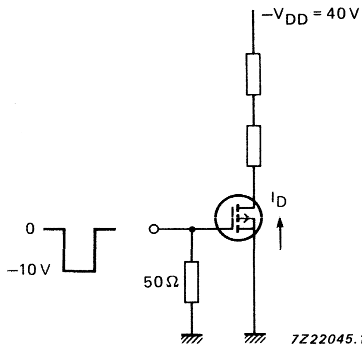


Fig.2 Switching times test circuit.

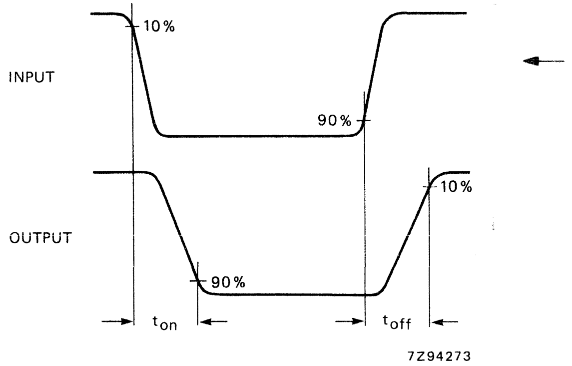


Fig.3 Input and output waveforms.

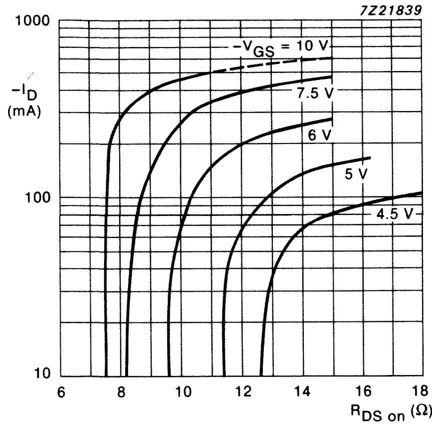


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

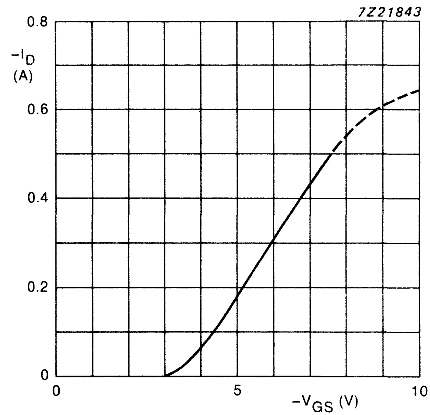


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

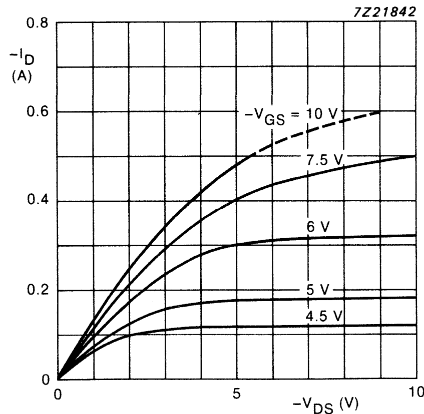


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

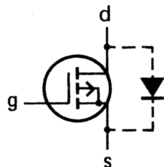
Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,3	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 6	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|y_{fs}\|$	typ.	200	mS

MECHANICAL DATA

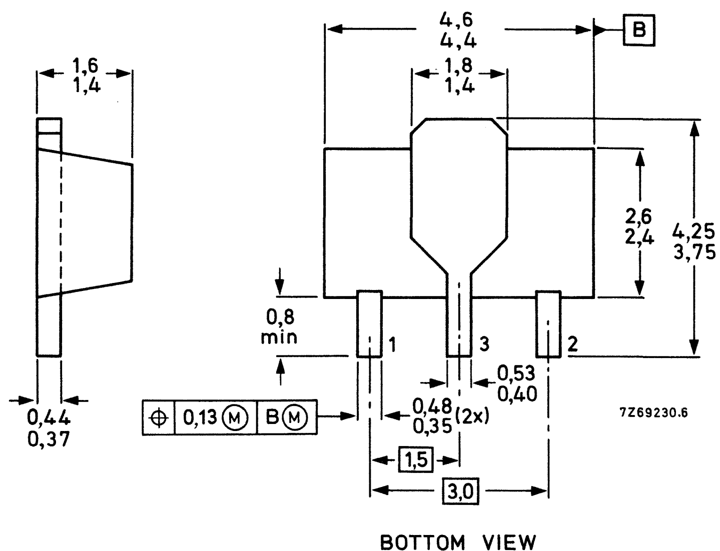
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



marking: LM



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 20 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2 and thickness = 0,7 mm.

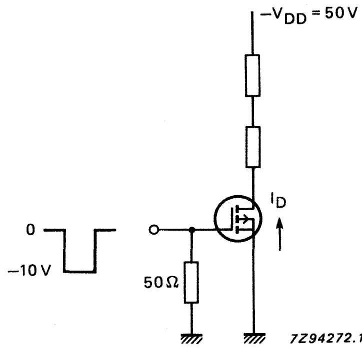


Fig.2 Switching times test circuit.

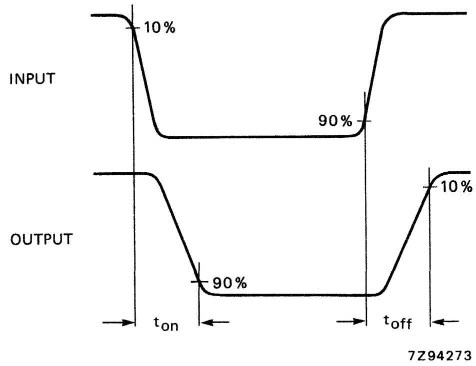


Fig.3 Input and output waveforms.

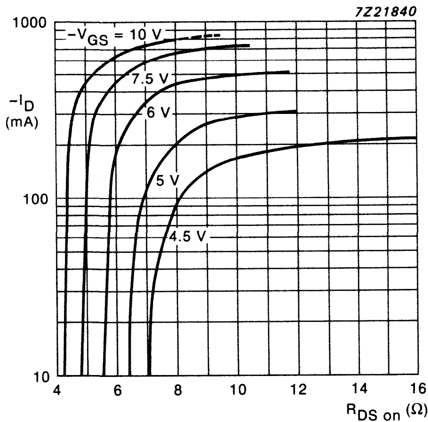


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

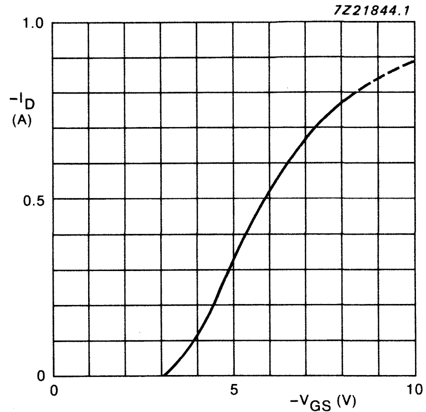


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

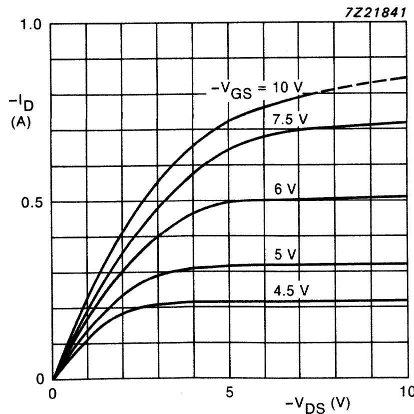


Fig.6 Output characteristics; T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max.	10	Ω
		typ.	7.5	Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125	mS

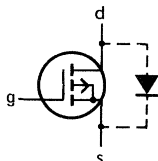
MECHANICAL DATA

Dimensions in mm

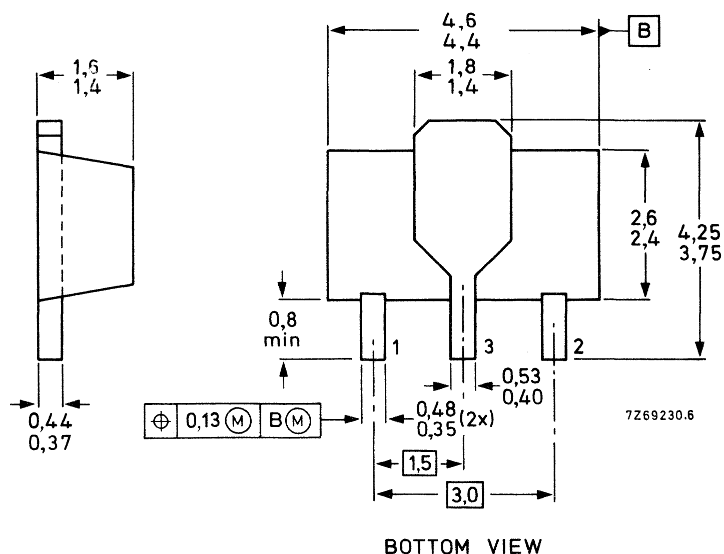
Fig. 1 SOT89.

Pinning:

1 = source
2 = gate
3 = drain



Marking: LN



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Drain current (peak)	$-I_{DM}$	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 10 µA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	µA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ..	10 7.5	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|y_{fs}\|$	typ.	125	mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 45	pF pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 10	ns ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2; thickness = 0,7 mm.

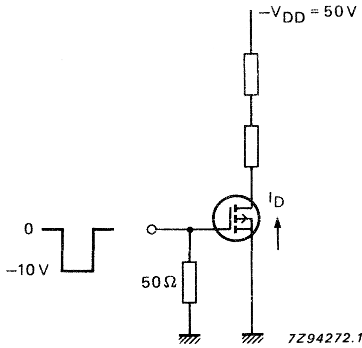


Fig. 2 Switching times test circuit.

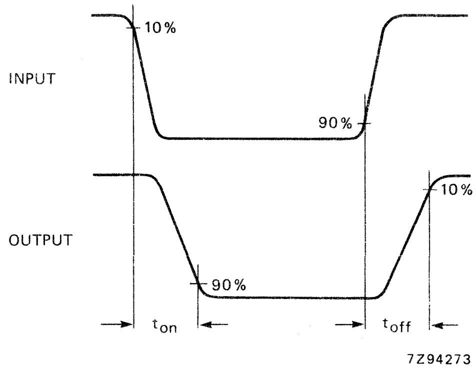


Fig. 3 Input and output waveforms.

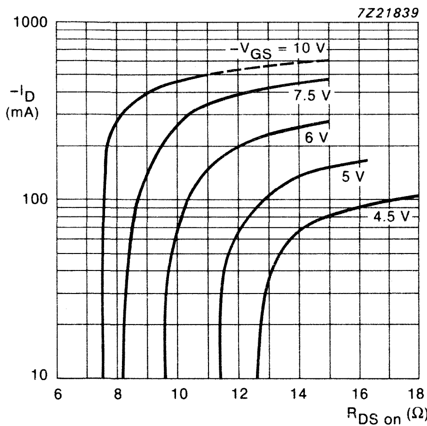


Fig.4 Drain current vs ON-resistance; $T_j = 25$ °C; typical values.

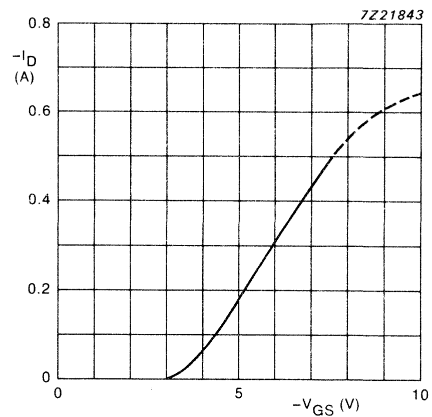


Fig.5 Transfer characteristics; $T_j = 25$ °C; $-V_{DS} = 10$ V; typical values.

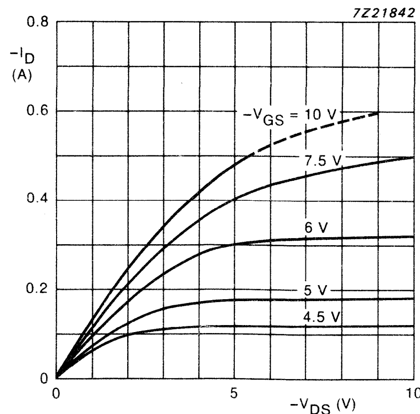


Fig.6 Output characteristics; $T_j = 25$ °C; typical values.

N-channel depletion mode vertical D-MOS transistors

BST124

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a TO-126 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-126

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	450	mA
P_{tot}	total power dissipation	up to T_h = 120 °C	–	6	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	−1.65	−0.75	V

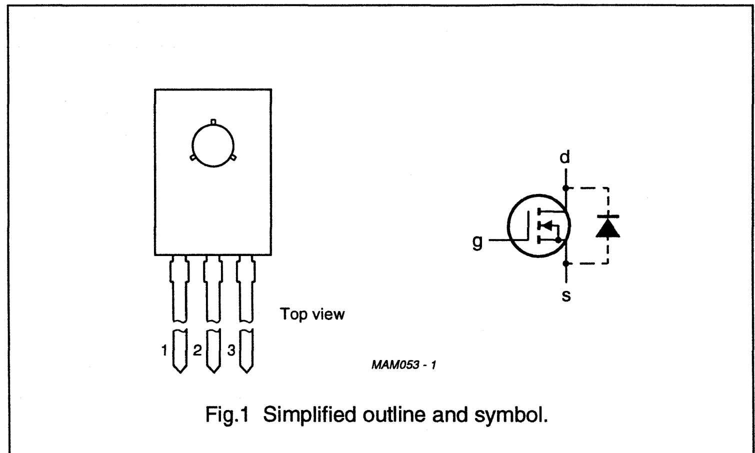


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	450	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_h = 120 °C	–	6	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}h}$	from junction to heatsink	5 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = −3 V	250	–	V
I_{DSX}	drain-source cut-off leakage current	V_{DS} = 200 V; V_{GS} = −3 V	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	100	nA
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	−1.65	−0.75	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = 3 V	−1.4	−0.6	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
		I_D = 250 mA; V_{GS} = 5 V	–	12	Ω
I_{DSS}	drain saturation current	V_{DS} = 25 V; V_{GS} = 0	70	–	mA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	15	pF
Switching times (see Figs 2 and 3)					
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = −3 to +5 V	–	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = +5 to −3 V	–	30	ns

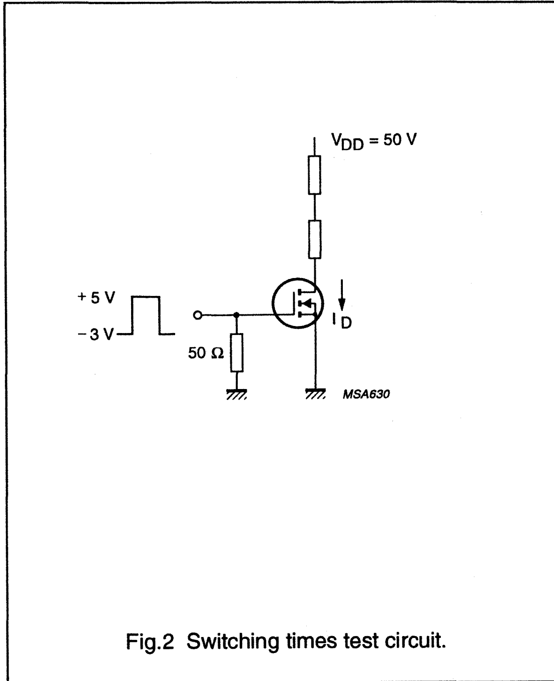


Fig.2 Switching times test circuit.

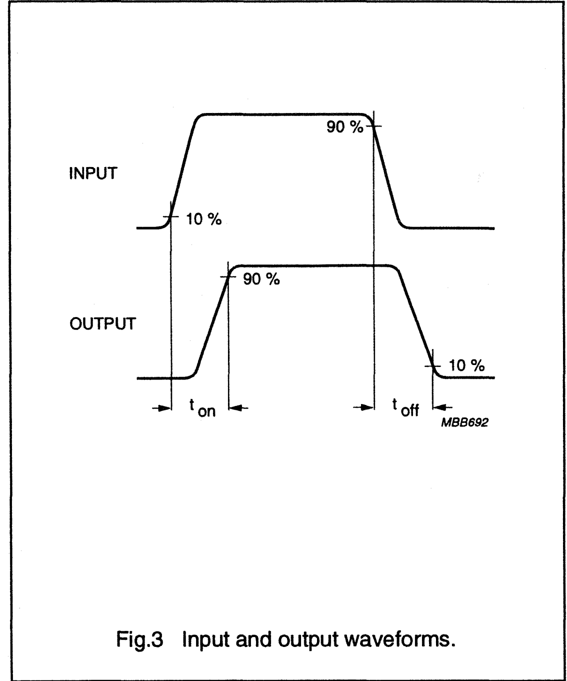


Fig.3 Input and output waveforms.

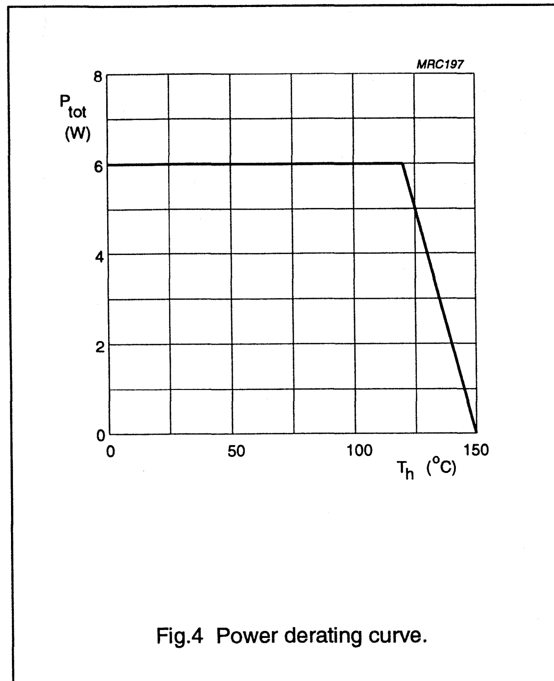
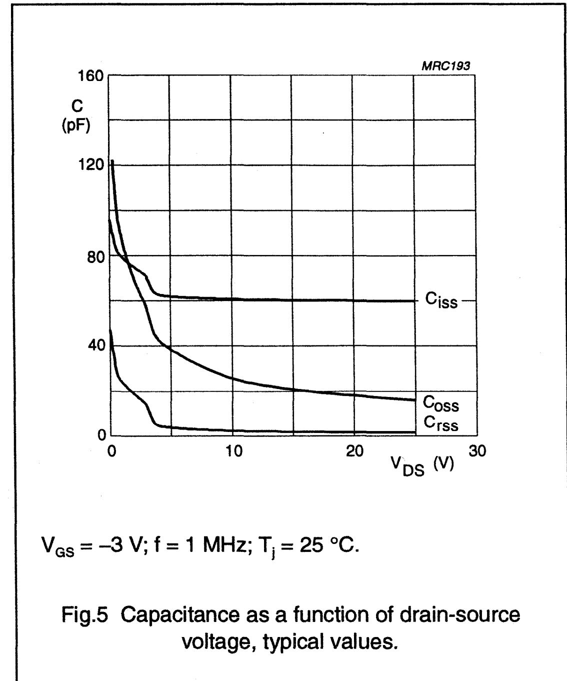
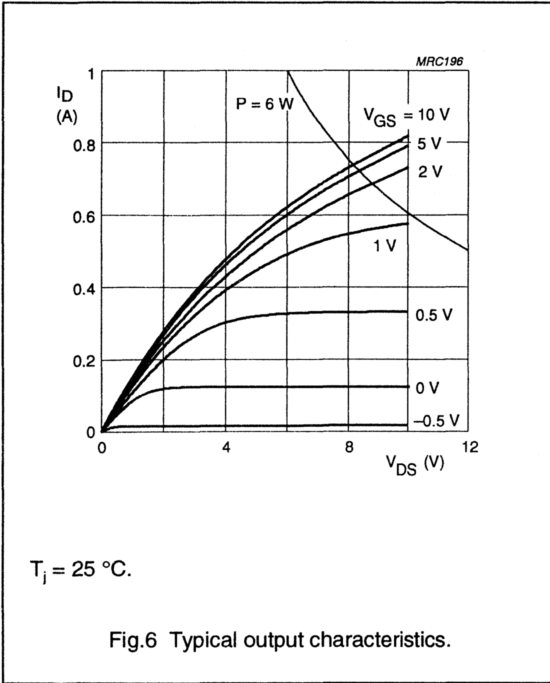


Fig.4 Power derating curve.



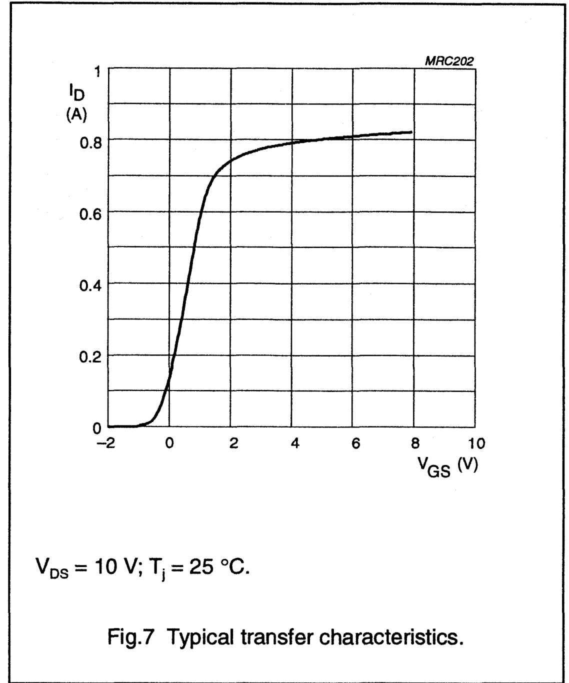
V_{GS} = −3 V; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



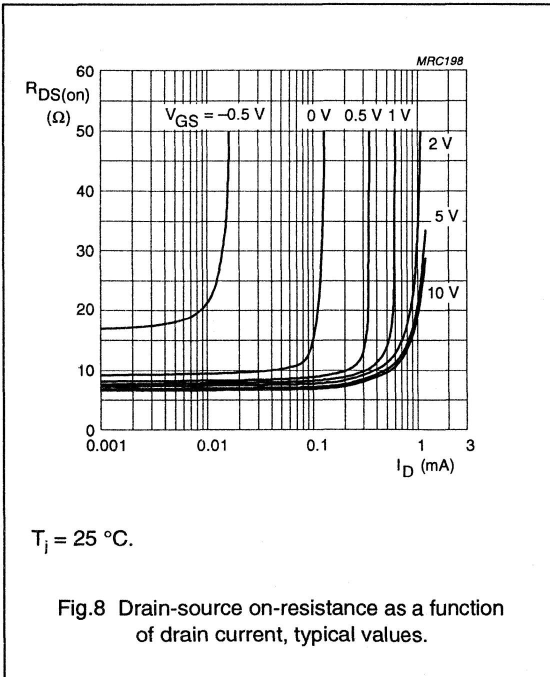
T_j = 25 °C.

Fig.6 Typical output characteristics.



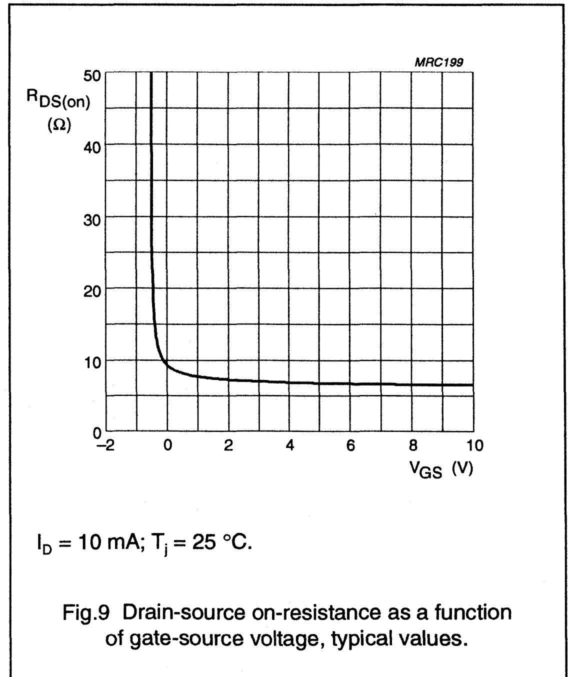
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



I_D = 10 mA; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

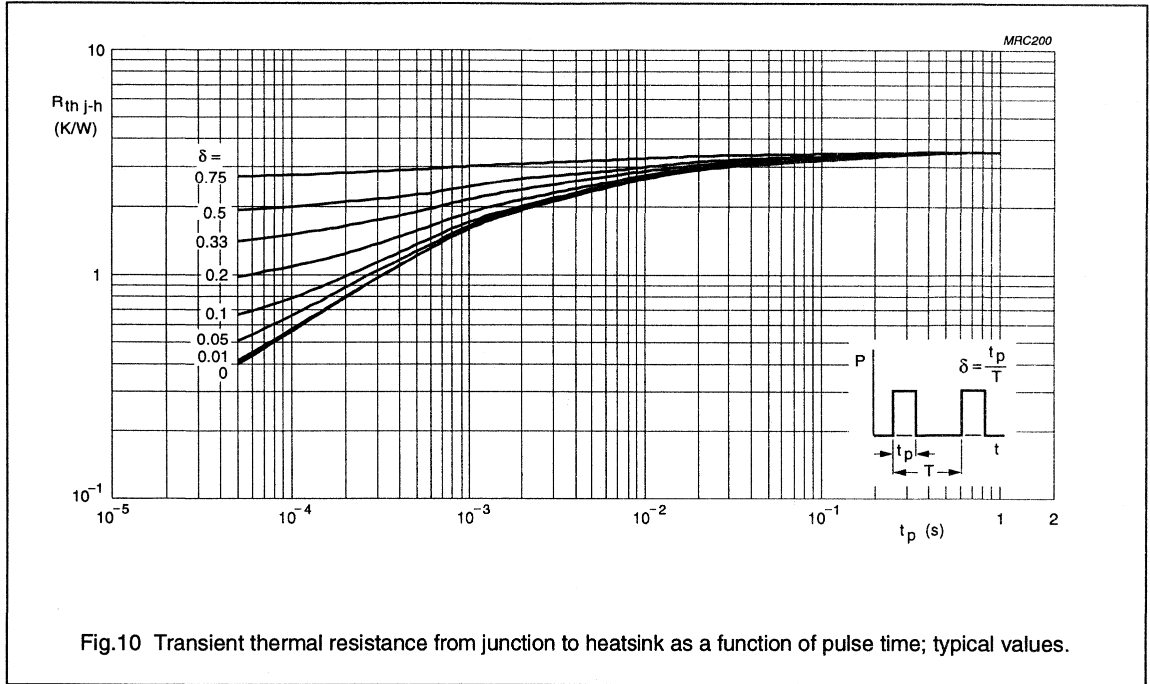
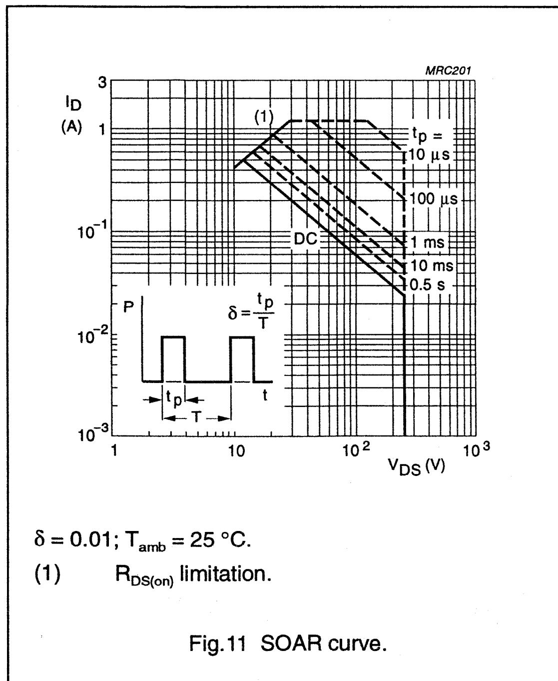


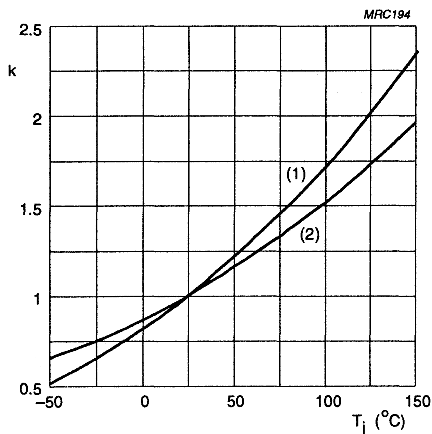
Fig.10 Transient thermal resistance from junction to heatsink as a function of pulse time; typical values.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



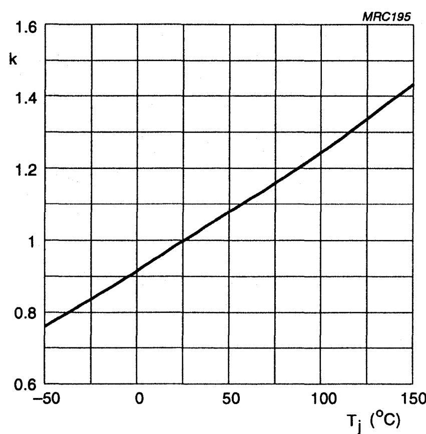
$$k = \frac{R_{DS(on)}\ at\ T_j}{R_{DS(on)}\ at\ 25\ °C}.$$

Typical $R_{DS(on)}$:

(1) I_D = 250 mA; V_{GS} = 5 V.

(2) I_D = 20 mA; V_{GS} = 0.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)}\ at\ T_j}{V_{GS(th)}\ at\ 25\ °C}.$$

Typical $V_{GS(th)}$ at I_D = 1 mA; V_{DS} = 3 V.

Fig.13 Temperature coefficient gate-source threshold voltage.

N-CHANNEL FETS

Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	40			V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	350			mW
			BSV78	**BSV79**	**BSV80**	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage I_D = 1 nA; V_{GS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V	C_{rs}	<	5	5	5	pF
Turn-on time	t_{on}	<	10	18	30	ns
Turn-off time	t_{off}	<	10	16	32	ns

MECHANICAL DATA

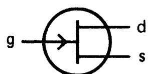
Dimensions in mm

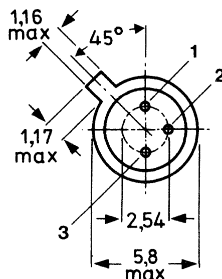
Fig. 1 TO-18.

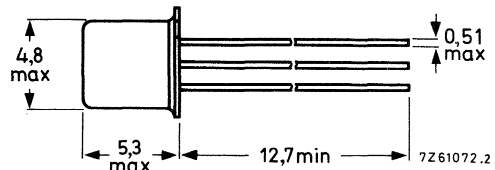
Gate connected to case

Pinning

1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Forward gate current	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 ^oC	P_{tot}	max.	350	mW
Storage temperature range	T_{stg}	−65 to + 175		^oC
Operating junction temperature	T_j	max.	175	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		BSV78	BSV79	BSV80	Unit
Gate cut-off currents						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<		0.25		nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<		0.5		μA
Drain cut-off current						
V_{DS} = 15 V; $-V_{GS}$ = 12 V	I_{DSX}	<		0.25		nA
V_{DS} = 15 V; $-V_{GS}$ = 12 V; T_j = 150 °C	I_{DSX}	<		0.5		μA
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Gate-source voltage						
I_D = 1.5 μA; V_{DS} = 15 V	$-V_{GS}$	>	3.5	1.75	0.75	V
		<	10	6.0	4.0	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	500			mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<		400		mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<			325	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
y parameters at f = 1 MHz (common source)						
$-V_{GS}$ = 10 V; V_{DS} = 0						
Input capacitance	C_{is}	<	10	10	10	pF
Feedback capacitance	C_{rs}	<	5	5	5	pF

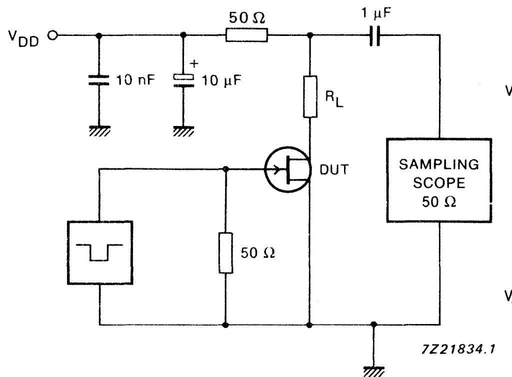
Switching times (see Fig. 2)

Turn-on time when switched from
$-V_{GSoff}$ = 11 V to I_{Don} = 20 mA; V_{DD} = 10 V (**BSV78**)
$-V_{GSoff}$ = 7 V to I_{Don} = 10 mA; V_{DD} = 10 V (**BSV79**)
$-V_{GSoff}$ = 5 V to I_{Don} = 5 mA; V_{DD} = 10 V (**BSV80**)

			BSV78	**BSV79**	**BSV80**	
delay time	t_d	<	5	10	10	ns
rise time	t_r	<	5	8	20	ns
turn-on time	t_{on}	<	10	18	30	ns

Turn-off time when switched from
I_{Don} = 20 mA to $-V_{GSMoff}$ = 11 V; V_{DD} = 10 V (**BSV78**)
I_{Don} = 10 mA to $-V_{GSMoff}$ = 7 V; V_{DD} = 10 V (**BSV79**)
I_{Don} = 5 mA to $-V_{GSMoff}$ = 5 V; V_{DD} = 10 V (**BSV80**)

			BSV78	**BSV79**	**BSV80**	
fall time	t_f	<	6	11	24	ns
storage time	t_s	<	4	5	8	ns
turn-off time	t_{off}	<	10	16	32	ns



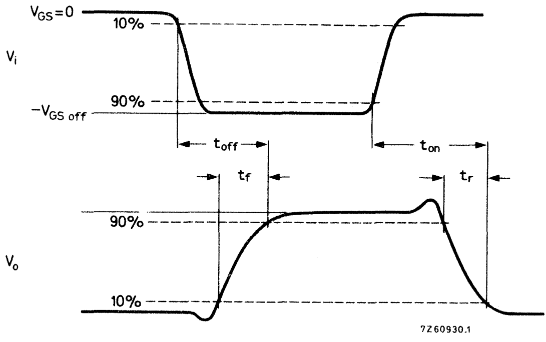


Fig. 2 Switching times test circuit and input and output waveforms.

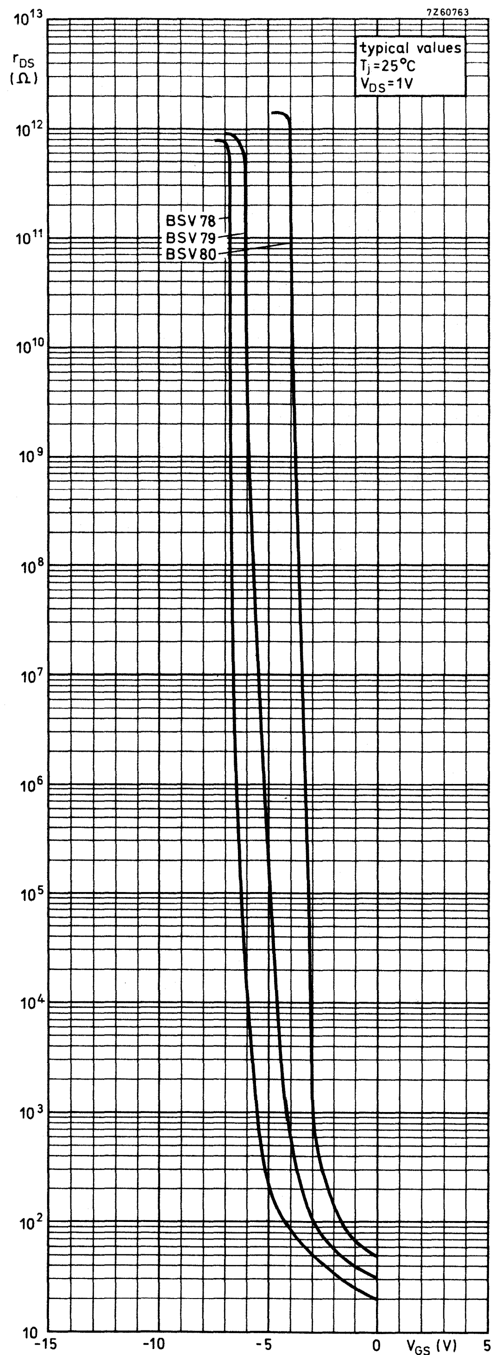
		BSV78	**BSV79**	**BSV80**	
R_L	=	424	909	1885	Ω

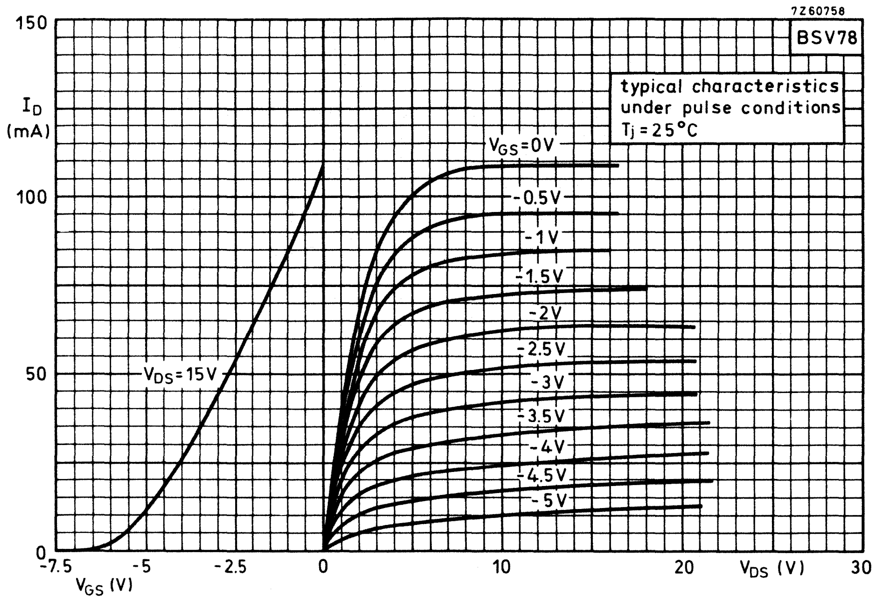
Pulse generator:

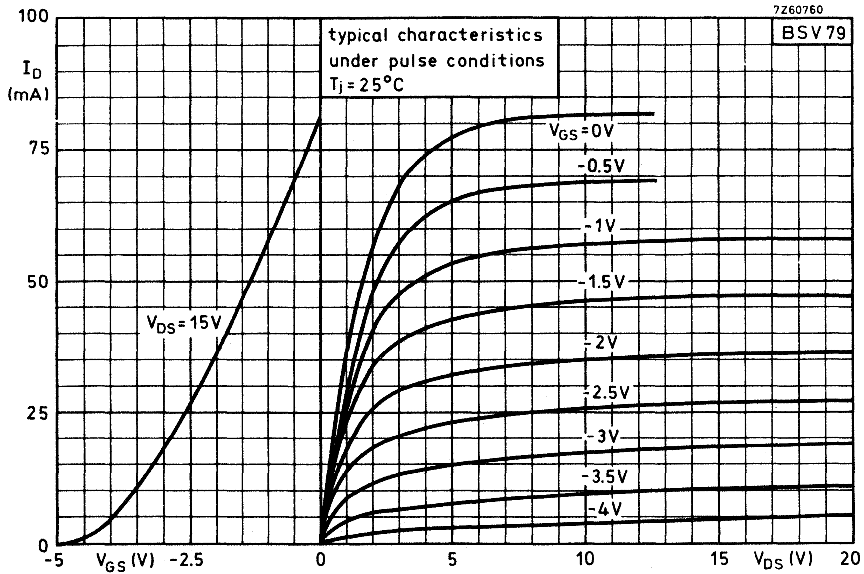
R_i = 50 Ω
t_r < 0.5 ns
t_f < 5 ns

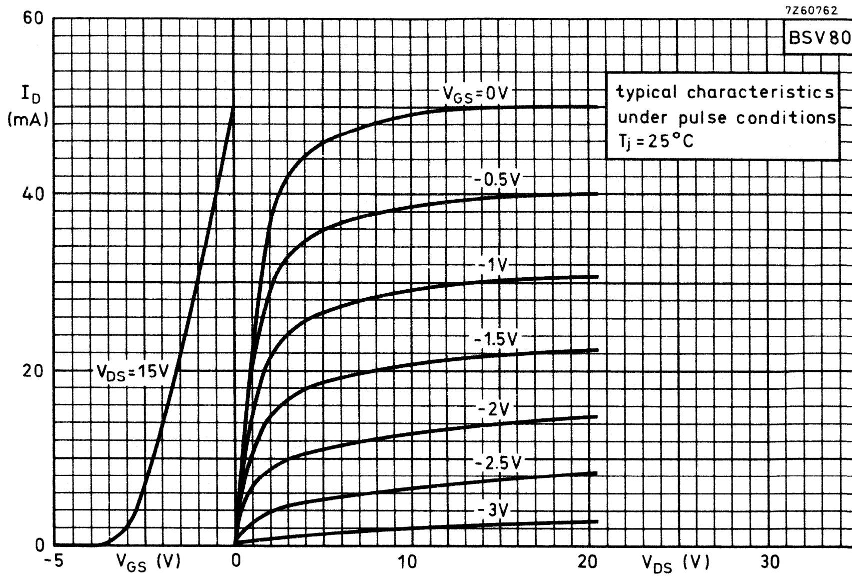
Oscilloscope:

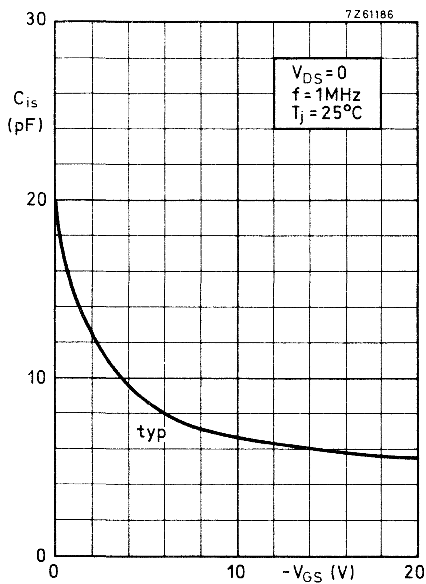
R_i = 50 Ω
t_r < 1 ns
t_f < 1 ns

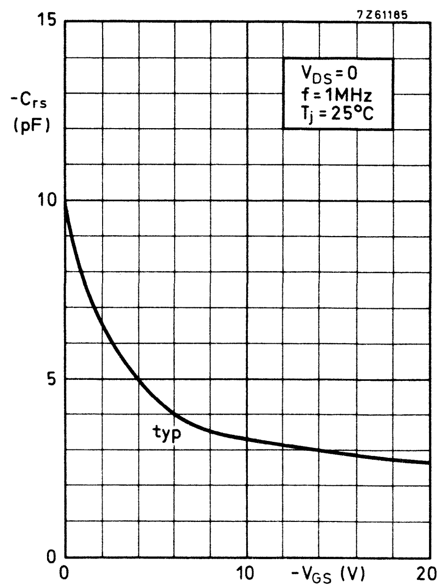

7Z60763
typical values
$T_j = 25\,^{\circ}C$
$V_{DS} = 1V$
r_{DS} (Ω)
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
BSV 78
BSV 79
BSV 80
-15
-10
-5
0
V_{GS} (V)
5

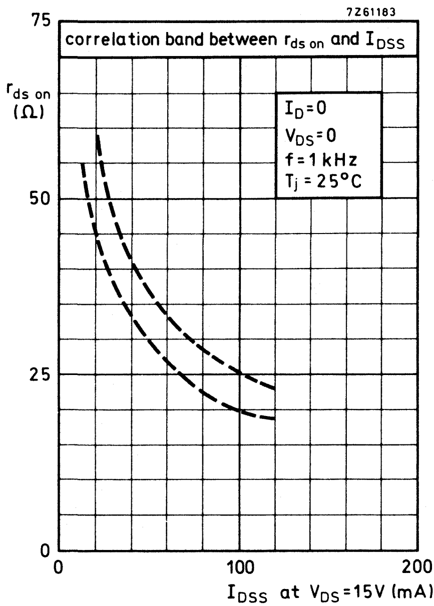

7Z60758
BSV78
typical characteristics
under pulse conditions
Tj = 25 °C
ID
(mA)
150
100
50
0
VGS = 0 V
-0.5 V
-1 V
-1.5 V
-2 V
-2.5 V
-3 V
-3.5 V
-4 V
-4.5 V
-5 V
VDS = 15 V
-7.5
-5
-2.5
0
10
20
30
VGS (V)
VDS (V)

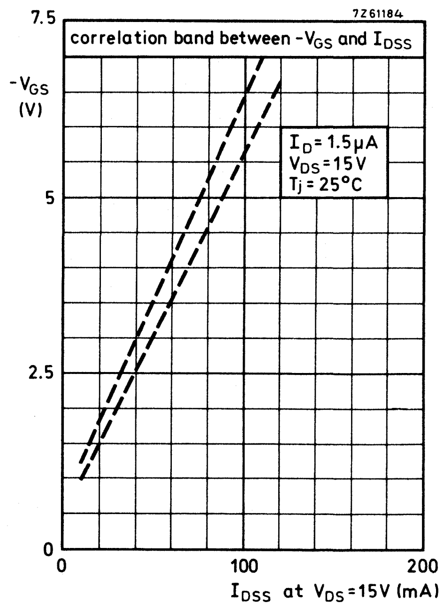

7Z60760
BSV79
typical characteristics
under pulse conditions
Tj = 25 °C
ID
(mA)
100
75
50
25
0
VGS = 0 V
-0.5 V
-1 V
-1.5 V
-2 V
-2.5 V
-3 V
-3.5 V
-4 V
VDS = 15 V
-5
-2.5
0
5
10
15
20
VGS (V)
VDS (V)


7Z60762
BSV80
typical characteristics under pulse conditions
T_j = 25 °C
I_D (mA)
V_{GS} = 0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
V_{DS} = 15V
V_{GS} (V)
V_{DS} (V)
60
40
20
0
-5
0
10
20
30


7Z61186
V_{DS} = 0
f = 1MHz
T_j = 25°C
C_{is} (pF)
typ
$-V_{GS}$ (V)
30
20
10
0
0
10
20


7Z61185
V_{DS} = 0
f = 1MHz
T_j = 25°C
$-C_{rs}$ (pF)
typ
$-V_{GS}$ (V)
15
10
5
0
0
10
20


7Z61183
correlation band between $r_{ds\,on}$ and I_{DSS}
$r_{ds\,on}$ (Ω)
$I_D = 0$
$V_{DS} = 0$
f = 1 kHz
$T_j = 25\,°C$
75
50
25
0
0
100
200
I_{DSS} at $V_{DS} = 15\,V$ (mA)


7Z61184
correlation band between $-V_{GS}$ and I_{DSS}
$-V_{GS}$ (V)
$I_D = 1.5\,\mu A$
$V_{DS} = 15\,V$
$T_j = 25\,°C$
7.5
5
2.5
0
0
100
200
I_{DSS} at $V_{DS} = 15\,V$ (mA)

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

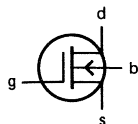
Drain-source resistance (on) at f = 1 kHz			
$V_{DS} = 0$; $V_{GS} = 5$ V; $V_{BS} = 0$	$R_{ds\,on}$	max.	50 Ω
Drain-source resistance (off)			
$V_{DS} = 10$ V; $-V_{GS} = 5$ V; $V_{BS} = 0$	$R_{DS\,off}$	min.	10 GΩ
Feedback capacitance at f = 1 MHz			
$-V_{GS} = 5$ V; $V_{DS} = 0$; $I_B = 0$	C_{rs}	typ.	0.5 pF
$-V_{GD} = 5$ V; $V_{SD} = 0$; $I_B = 0$	C_{rd}	typ.	0.5 pF

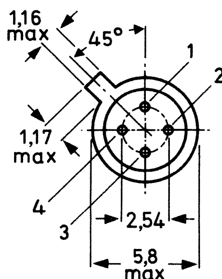
MECHANICAL DATA

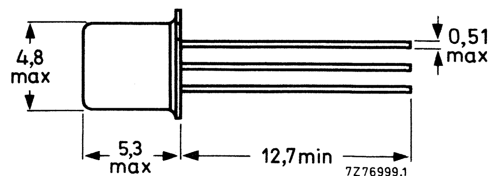
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = drain
2 = source
3 = gate
4 = substrate (b)
connected to case







Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	V_{GB}	max.	10	V
		min.	−10	V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	$V_{G\text{-}N}$	max.	15	V
		min.	−15	V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $t < 10$ ms	$V_{G\text{-}N}$	max.	50	V
		min.	−50	V
Drain current (DC)	I_D	max.	25	mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0.1$	I_{DM}	max.	50	mA
Source current (peak value) $t_p = 20$ ms; $\delta = 0.1$	I_{SM}	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−65 to + 125	^oC
Junction temperature	T_j	max.	125	^oC

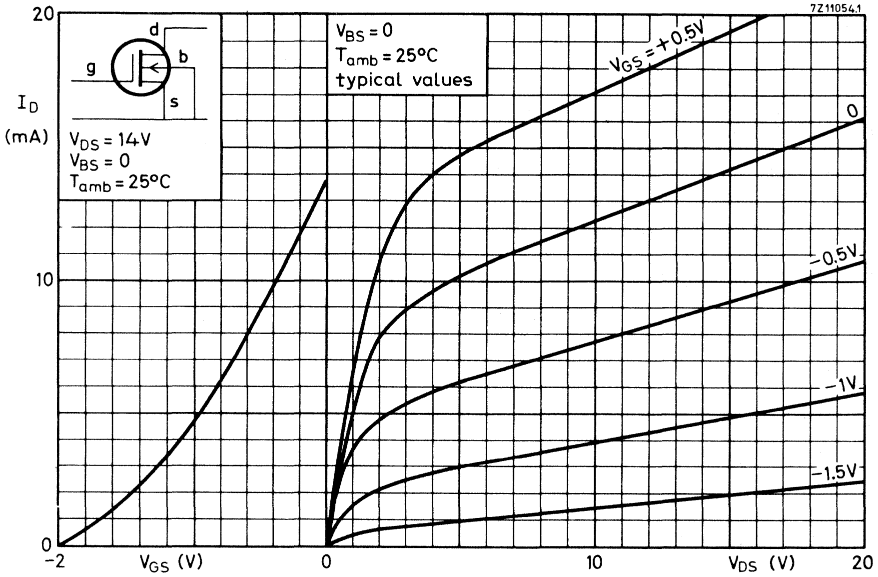
THERMAL RESISTANCE

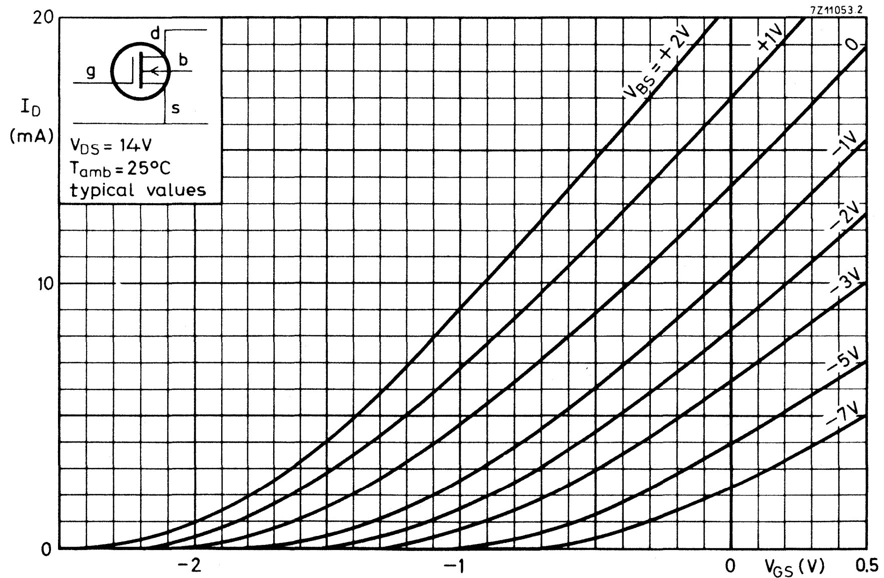
Parameter	Symbol		Value
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500 K/W

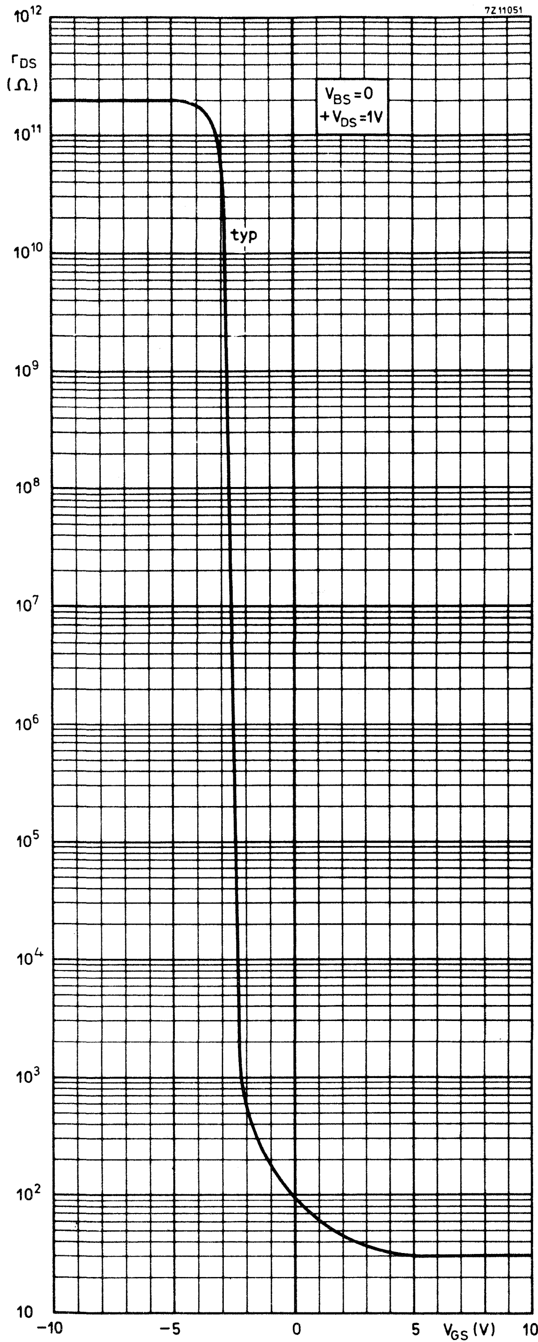
CHARACTERISTICS

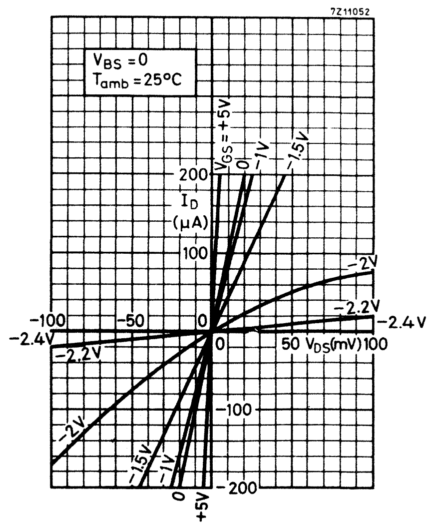
T_j = 25 °C unless otherwise specified

Drain cut-off currents; $V_{BS} = 0$				
$V_{DS} = 10$ V; $-V_{GS} = 5$ V	I_{DSX}	<	1	nA
$V_{DS} = 10$ V; $-V_{GS} = 5$ V; $T_j = 125$ °C	I_{DSX}	<	1	μA
Source cut-off currents; $V_{BD} = 0$				
$V_{SD} = 10$ V; $-V_{GD} = 5$ V	I_{SDX}	<	1	nA
$V_{SD} = 10$ V; $-V_{GD} = 5$ V; $T_j = 125$ °C	I_{SDX}	<	1	μA
Gate currents; $V_{BS} = 0$				
$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10$ V; $V_{DS} = 0$	I_{GSS}	<	10	pA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125$ °C	$-I_{GSS}$	<	200	pA
$V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125$ °C	I_{GSS}	<	200	pA
Bulk currents; $V_{GB} = 0$				
$-V_{BD} = 30$ V; $I_S = 0$	$-I_{BDO}$	<	10	μA
$-V_{BS} = 30$ V; $I_D = 0$	$-I_{BSO}$	<	10	μA
Drain-source resistance (on) at f = 1 kHz; $V_{BS} = 0$				
$V_{GS} = 0$; $V_{DS} = 0$	$R_{ds\ on}$	<	100	Ω
$V_{GS} = 0$; $V_{DS} = 0$; $T_j = 125$ °C	$R_{ds\ on}$	<	150	Ω
$+V_{GS} = 5$ V; $V_{DS} = 0$	$R_{ds\ on}$	<	50	Ω
Drain-source resistance (off)				
$-V_{GS} = 5$ V; $V_{DS} = 10$ V; $V_{BS} = 0$	$R_{DS\ off}$	>	10	GΩ
Feedback capacitances at f = 1 MHz				
$-V_{GS} = 5$ V; $V_{DS} = 0$; $I_B = 0$	C_{rs}	typ.	0.5	pF
$-V_{GD} = 5$ V; $V_{SD} = 0$; $I_B = 0$	C_{rd}	typ.	0.5	pF
Gate to all other terminals capacitance at f = 1 MHz				
$-V_{GB} = 5$ V; $V_{SB} = V_{DB} = 0$	C_{g-n}	<	6	pF


7Z11054.1
$V_{BS} = 0$
$T_{amb} = 25°C$
typical values
I_D
(mA)
$V_{DS} = 14V$
$V_{BS} = 0$
$T_{amb} = 25°C$
$V_{GS} = +0.5V$
0
−0.5V
−1V
−1.5V
V_{GS} (V)
V_{DS} (V)
20
10
0
−2
0
10
20
d
g
b
s


7Z11053.2
I_D
(mA)
$V_{DS} = 14V$
$T_{amb} = 25°C$
typical values
$V_{BS} = +2V$
+1V
0
−1V
−2V
−3V
−5V
−7V
V_{GS} (V)
20
10
0
−2
−1
0
0.5
d
g
b
s


7Z11051
r_{DS} (Ω)
$V_{BS}=0$
$+V_{DS}=1V$
typ
10^{12}
10^{11}
10^{10}
10^9
10^8
10^7
10^6
10^5
10^4
10^3
10^2
10
−10
−5
0
5
V_{GS} (V)
10


7Z11052
$V_{BS}=0$
$T_{amb}=25°C$
$V_{GS}=+5V$
0
−1V
−1.5V
200
I_D (μA)
100
−2V
−2.2V
−2.4V
−100
−50
0
50
V_{DS}(mV)
100
−100
−200
+5V

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

J108/J109/J110
N-channel junction FETs

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for J108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-92 envelope. They are intended for use in applications such as analog switches, choppers and commutators.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

Note

1. Drain and source are interchangeable.

PIN CONFIGURATION

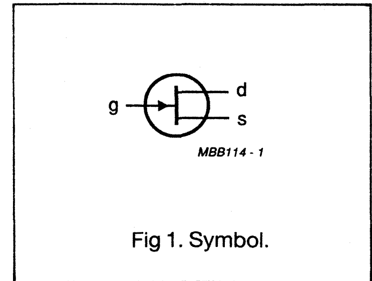


Fig 1. Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C	-	400	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	250	K/W

STATIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS} = 10$ V $V_{DS} = 5$ V		-	3	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V	J108 J109 J110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ μA $V_{DS} = 0$		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ μA $V_{DS} = 5$ V	J108 J109 J110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V	J108 J109 J110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.2)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (J108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (J109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (J110).

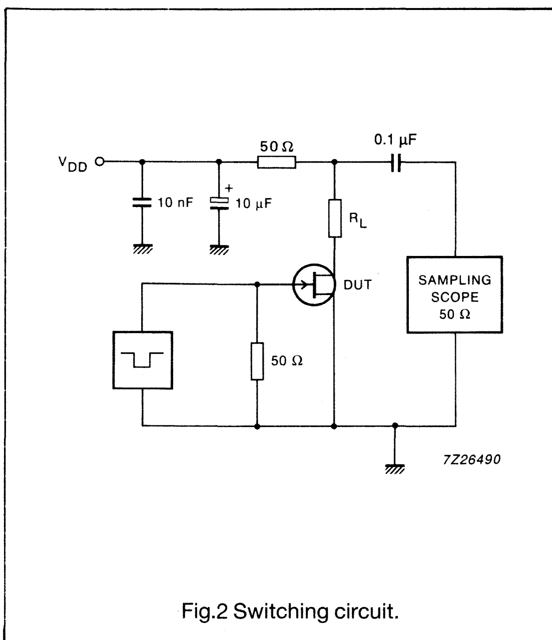


Fig.2 Switching circuit.

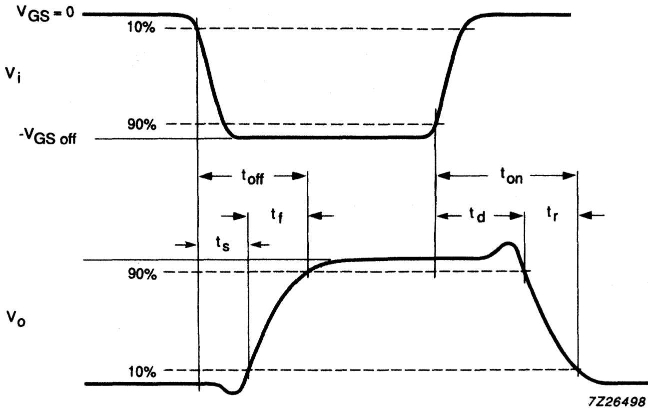


Fig.3 Input and output waveforms.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

Features

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS\ on}$ at zero gate voltage

QUICK REFERENCE DATA

			J111	J112	J113	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	400	400	mW
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

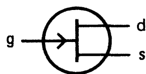
MECHANICAL DATA

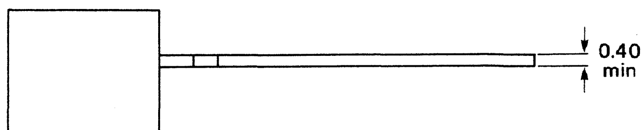
Dimensions in mm

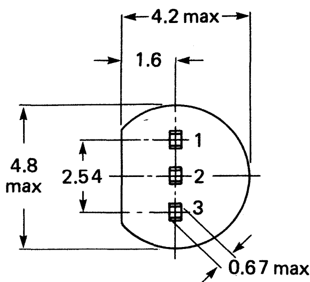
Fig.1 TO-92.

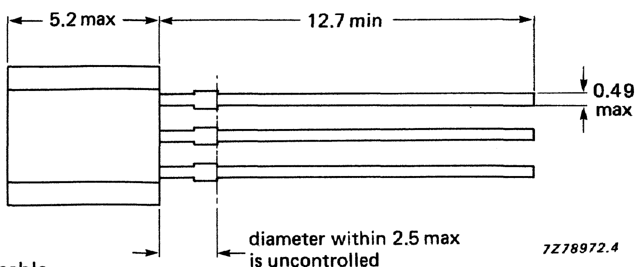
Pinning

1 = Gate
2 = Source
3 = Drain









Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Gate-source voltage	$-V_{GSO}$	max.	40 V
Gate-drain voltage	$-V_{GDO}$	max.	40 V
Gate forward current (DC)	I_G	max.	50 mA
Total power dissipation up to $T_{amb} = 50\ ^oC$	P_{tot}	max.	400 mW
Storage temperature range	T_{stg}		−65 to + 150 ^oC
Junction temperature	T_j	max.	150 ^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W

STATIC CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

			J111	J112	J113	
Gate reverse current $-V_{GS} = 15$ V; $V_{DS} = 0$	$-I_{GSS}$	max.	1	1	1	nA
Drain cut-off current $V_{DS} = 5$ V; $-V_{GS} = 10$ V	$-I_{DSX}$	max.	1	1	1	nA
Drain saturation current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	min.	20	5	2	mA
Gate-source breakdown voltage $-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage $V_{DS} = 5$ V; $I_D = 1\ \mu A$	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance $V_{DS} = 0.1$ V; $V_{GS} = 0$	$R_{DS\ on}$	max.	30	50	100	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{is}	typ.	6 pF
V_{DS} = $-V_{GS}$ = 0; f = 1 MHz	C_{is}	typ.	22 pF
		max.	28 pF
Feedback capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{rs}	typ.	3 pF

Switching times

test conditions
V_{DD} = 10 V; V_{GS} = 0 to V_{GSoff}
$-V_{GS\,off}$ = 12 V; R_L = 750 Ω for J111
$-V_{GS\,off}$ = 7 V; R_L = 1550 Ω for J112
$-V_{GS\,off}$ = 5 V; R_L = 3150 Ω for J113

Rise time	t_r	typ.	6 ns
Turn-on time	t_{on}	typ.	13 ns
Fall time	t_f	typ.	15 ns
Turn-off time	t_{off}	typ.	35 ns

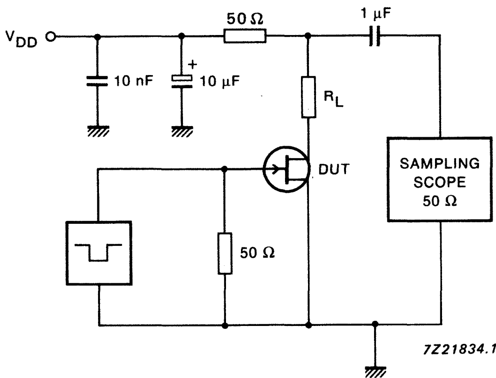


Fig.2 Switching times test circuit.

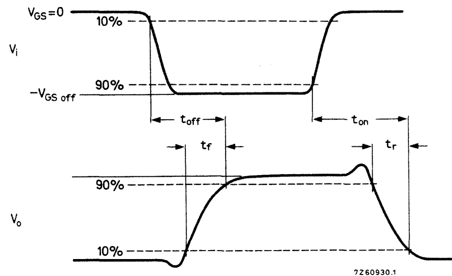


Fig.3 Input and output waveforms.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate current	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW

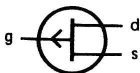
			J174	J175	J176	J177	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	max.	85	125	250	300	Ω

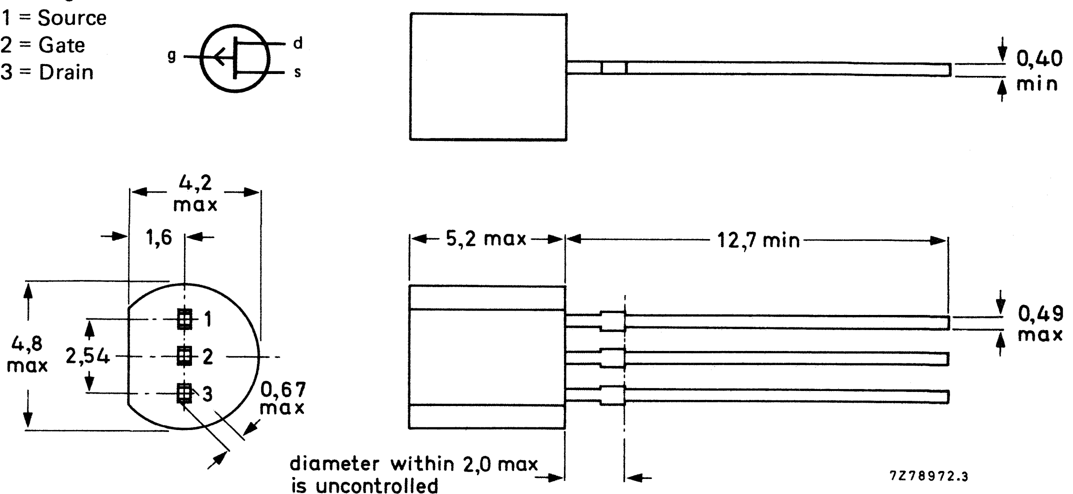
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning:
1 = Source
2 = Gate
3 = Drain





Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			J174	J175	J176	J177	
Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	max.	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	max.	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	min.	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\,off}$	min.	5	3	1	0.8	V
		max.	10	6	4	2.25	V
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	R_{DSon}	max.	85	125	250	300	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz				
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.	8	pF
$-V_{GS} = V_{DS} = 0$	C_{is}	typ.	30	pF
Feedback capacitance, f = 1 MHz				
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.	4	pF

Switching times (see Fig. 2 + 3)			J174	J175	J176	J177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage time	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

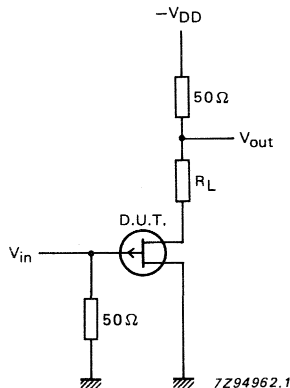


Fig. 2 Switching times test circuit.

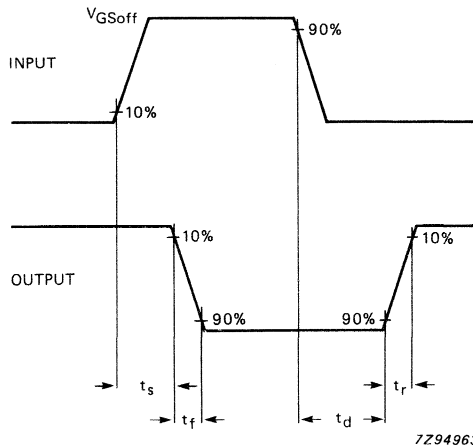


Fig. 3 Input and output waveforms;
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$.

N-channel silicon field-effect transistors

J308/309/310

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-92 envelope. They are intended for use in the AM input stage in car radios and in UHF/VHF amplifiers, oscillators and mixers.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

PIN CONFIGURATION

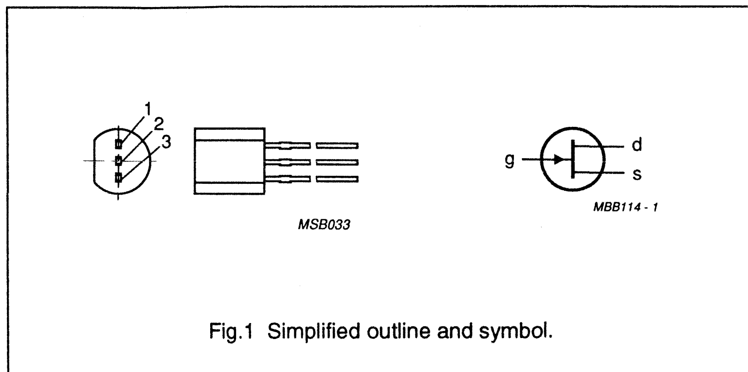


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	J308		12	60	mA
	J309		12	30	mA
	J310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA			
	J308		1	6.5	V
	J309		1	4	V
	J310		2	6.5	V
Y_{fs}	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	250	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead minimum 10 x 10 mm

STATIC CHARACTERISTICS

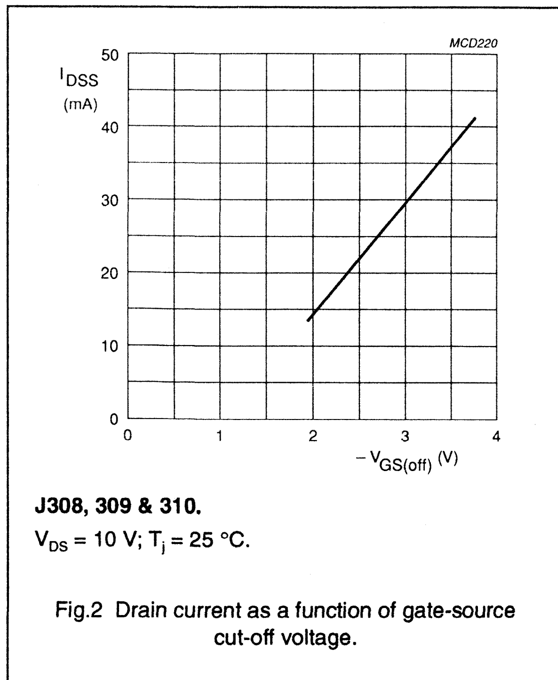
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	–	–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	J308		12	–	60	mA
	J309		12	–	30	mA
	J310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	J308		1	–	6.5	V
	J309		1	–	4	V
	J310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\|Y_{os}\|$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

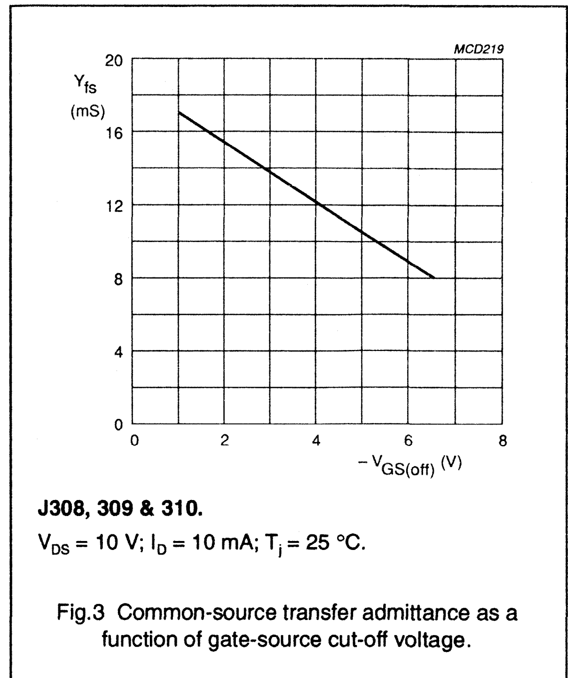
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\bar{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

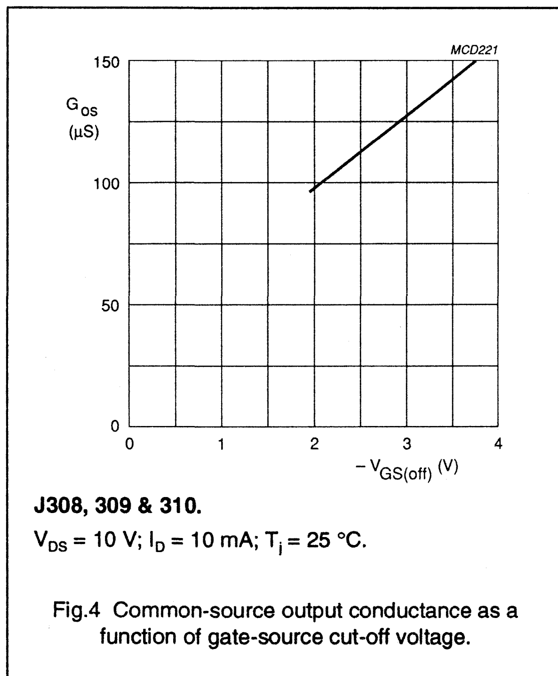
Fig.2 Drain current as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

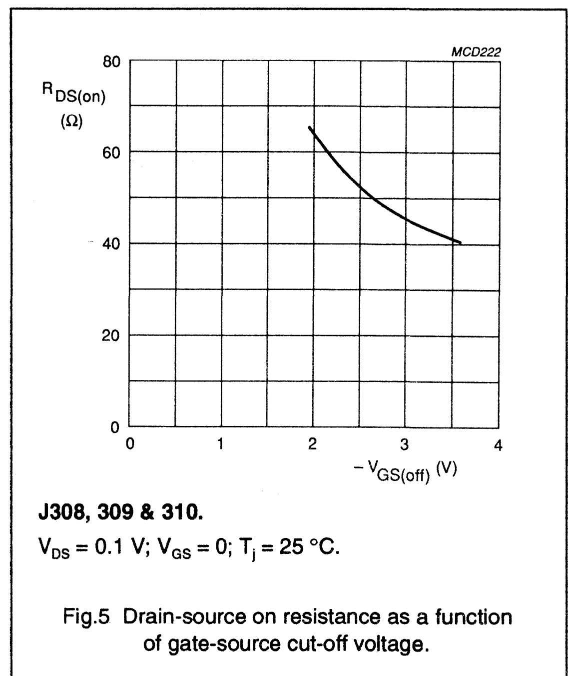
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

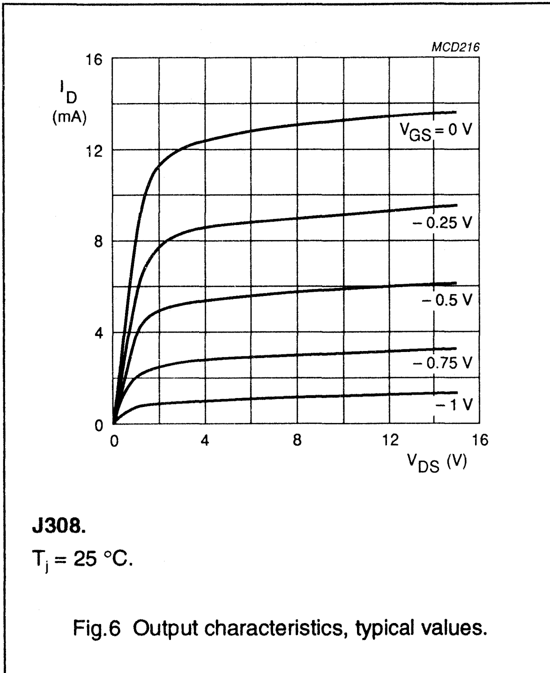
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

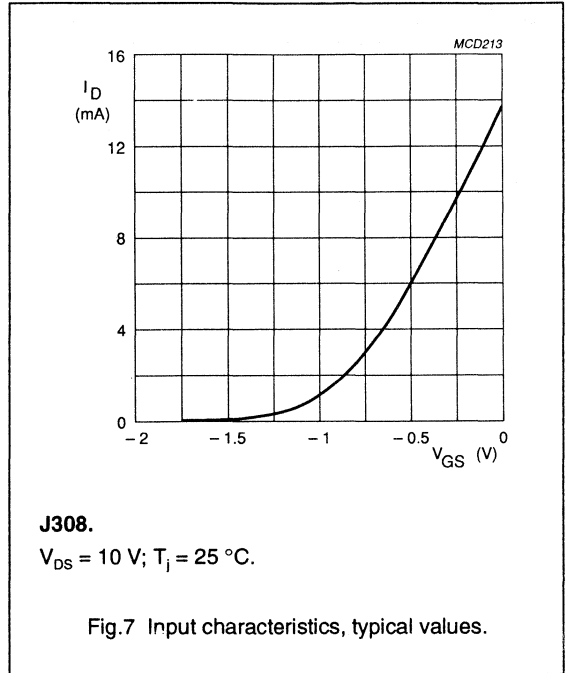
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



J308.

T_j = 25 °C.

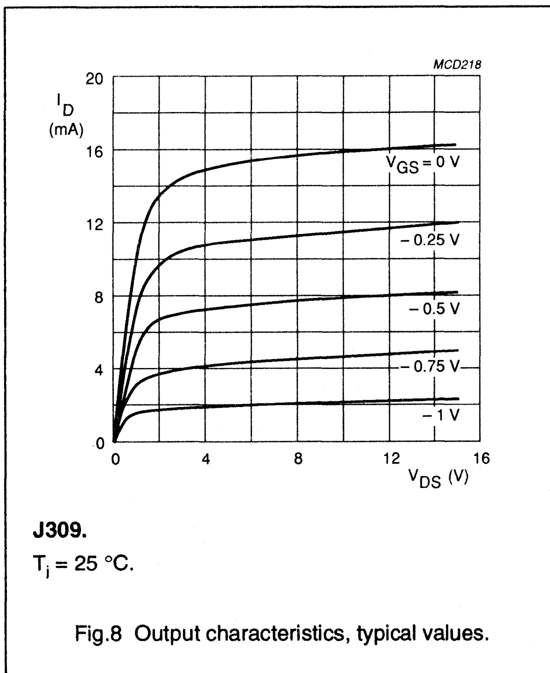
Fig.6 Output characteristics, typical values.



J308.

V_{DS} = 10 V; T_j = 25 °C.

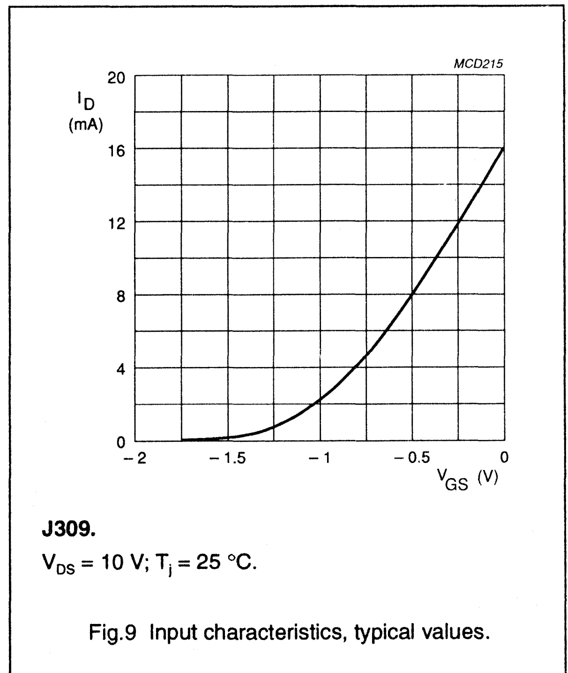
Fig.7 Input characteristics, typical values.



J309.

T_j = 25 °C.

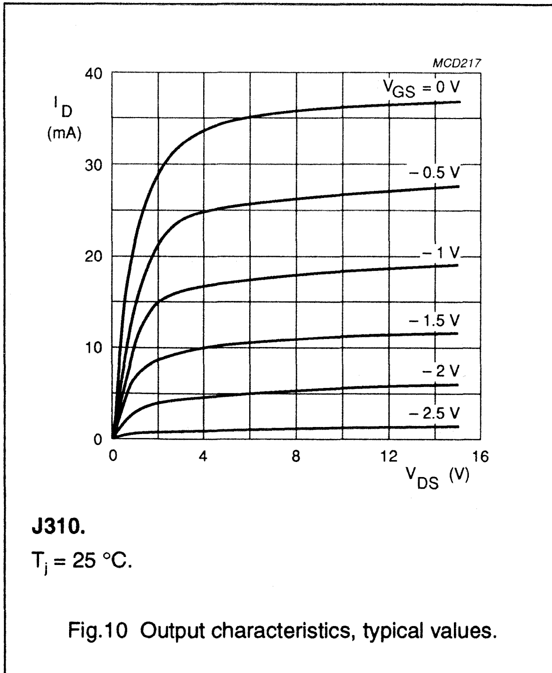
Fig.8 Output characteristics, typical values.



J309.

V_{DS} = 10 V; T_j = 25 °C.

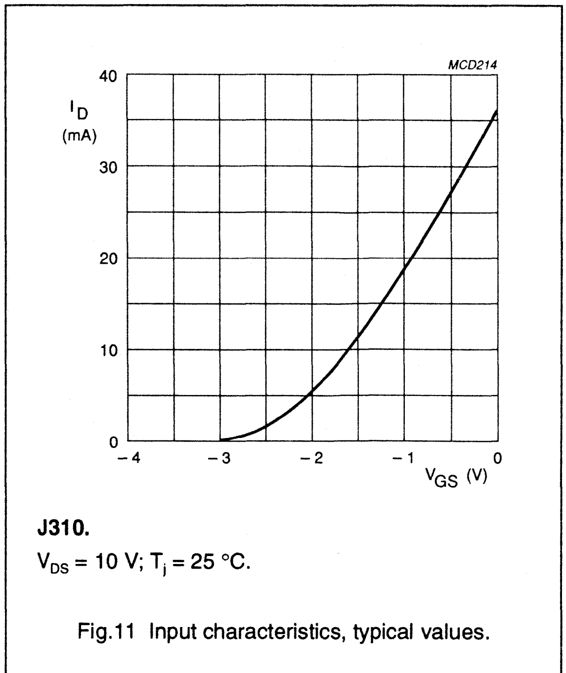
Fig.9 Input characteristics, typical values.



J310.

T_j = 25 °C.

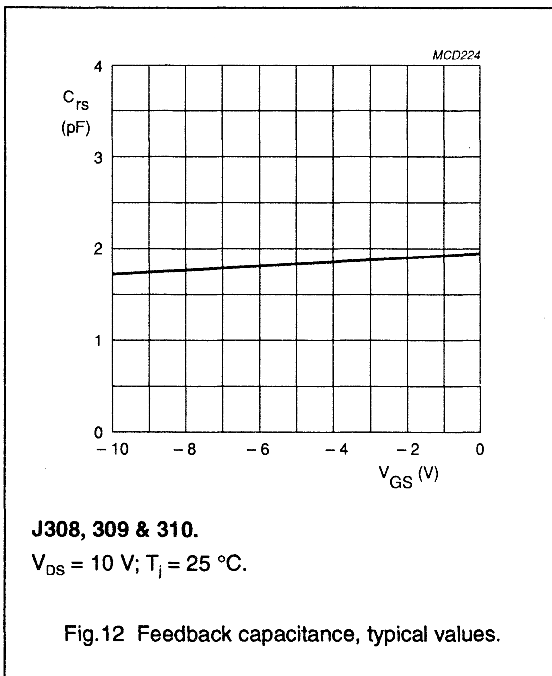
Fig.10 Output characteristics, typical values.



J310.

V_{DS} = 10 V; T_j = 25 °C.

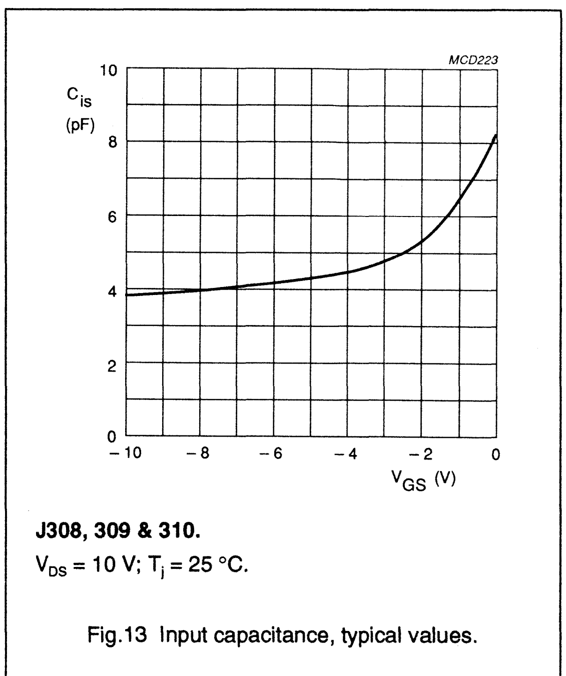
Fig.11 Input characteristics, typical values.



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

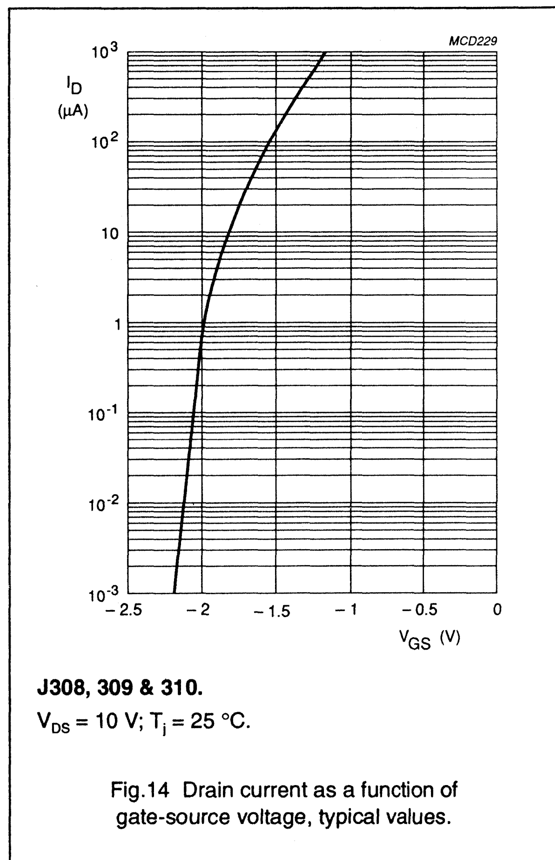
Fig.12 Feedback capacitance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

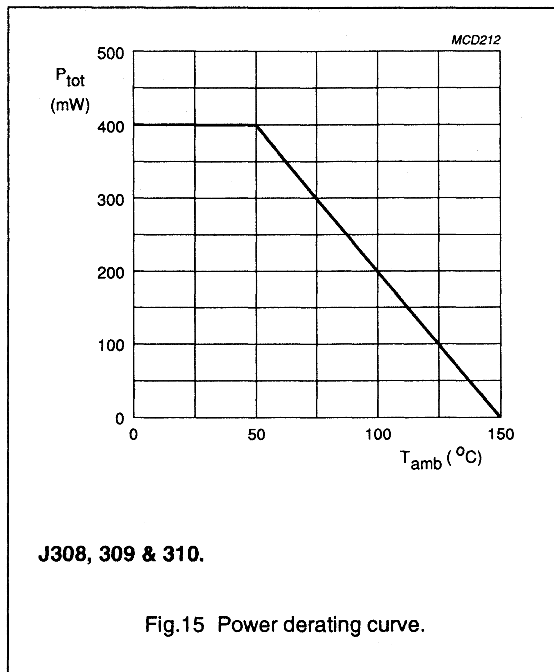
Fig.13 Input capacitance, typical values.



J308, 309 & 310.

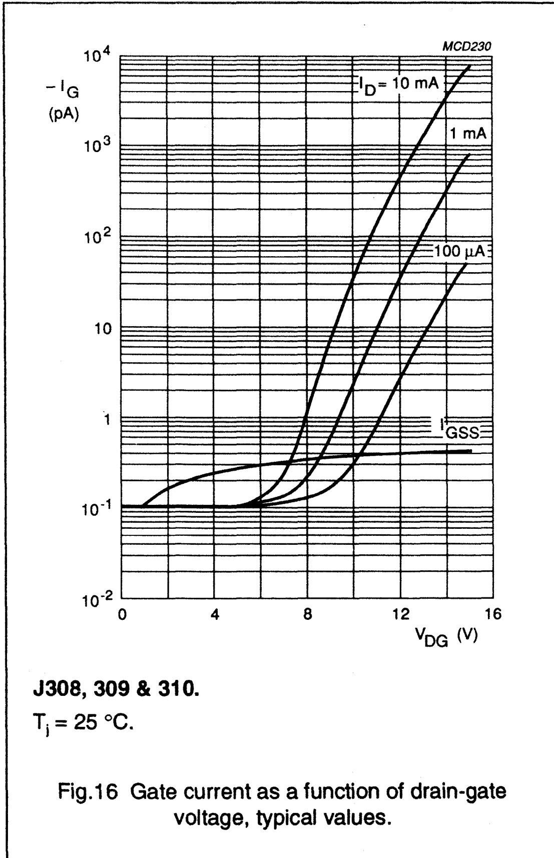
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



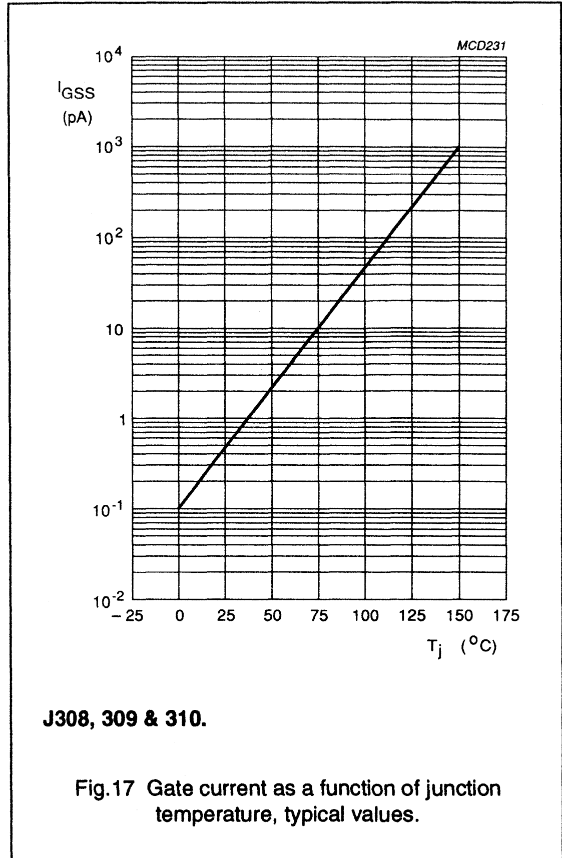
J308, 309 & 310.

Fig.15 Power derating curve.



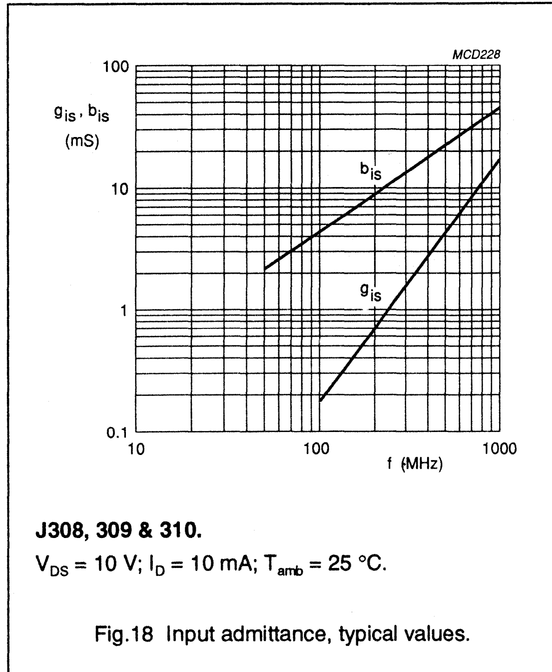
J308, 309 & 310.
T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



J308, 309 & 310.

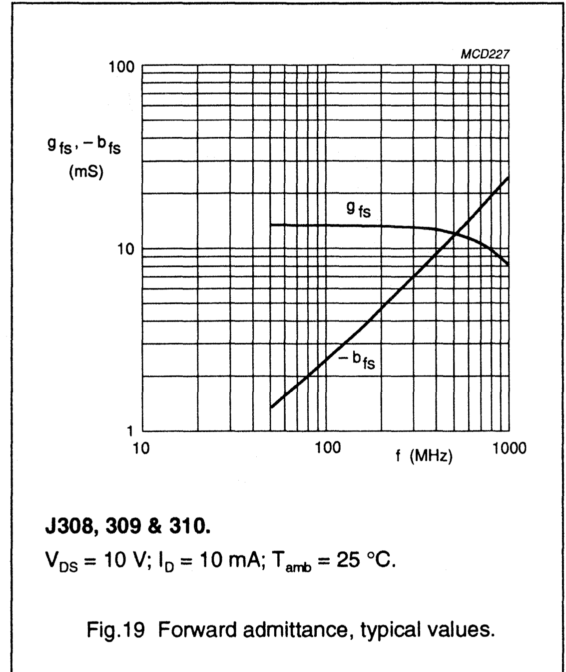
Fig.17 Gate current as a function of junction temperature, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

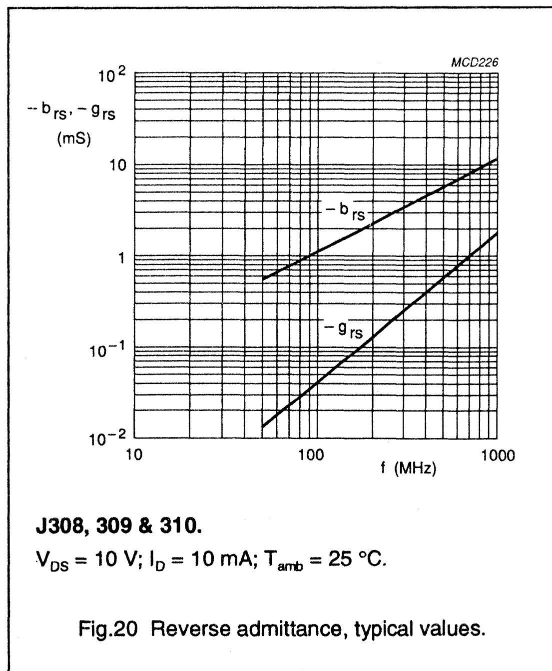
Fig.18 Input admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

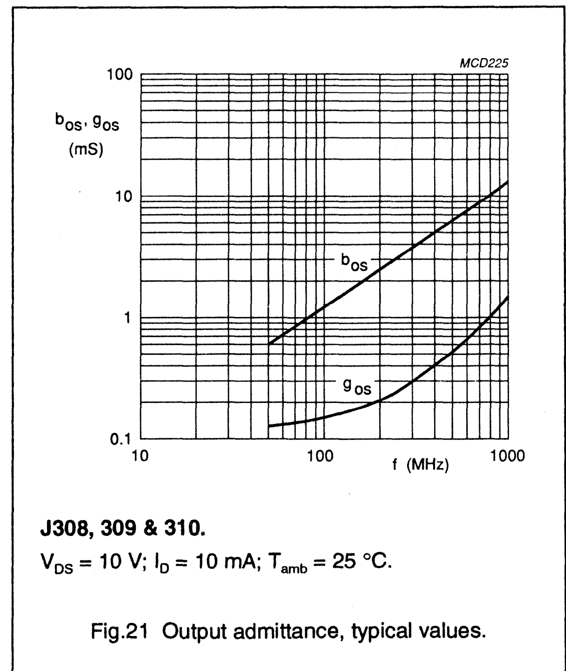
Fig.19 Forward admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	November 1990

PMBF107
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	100	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	28	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.4	V

PIN CONFIGURATION

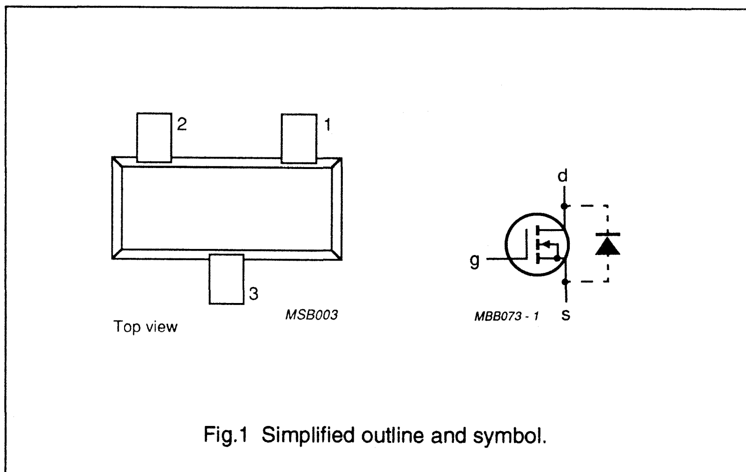


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	100	mA
I_{DM}	drain current	peak value	–	250	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printboard.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printboard.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain cut-off current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
		I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

PMBF107

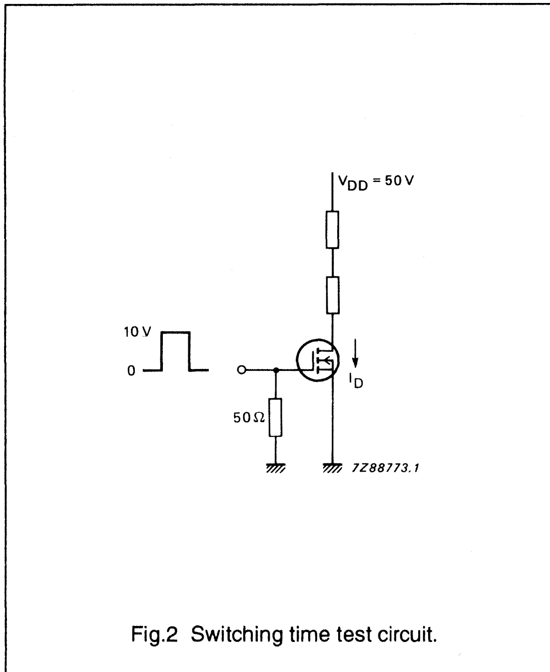


Fig.2 Switching time test circuit.

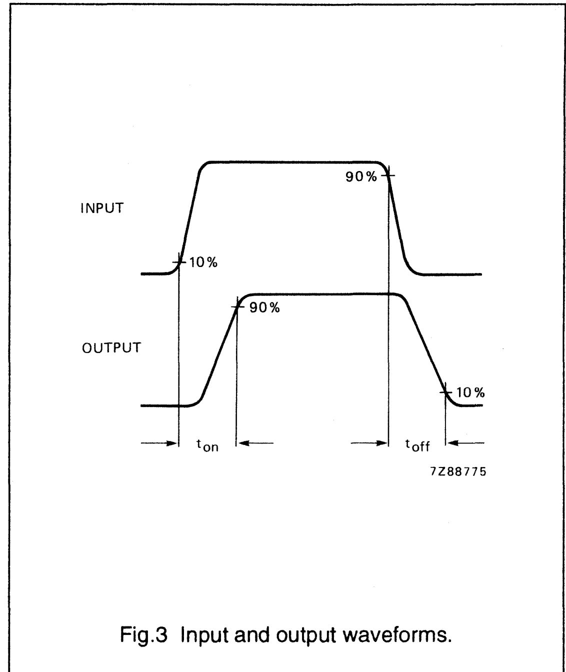


Fig.3 Input and output waveforms.

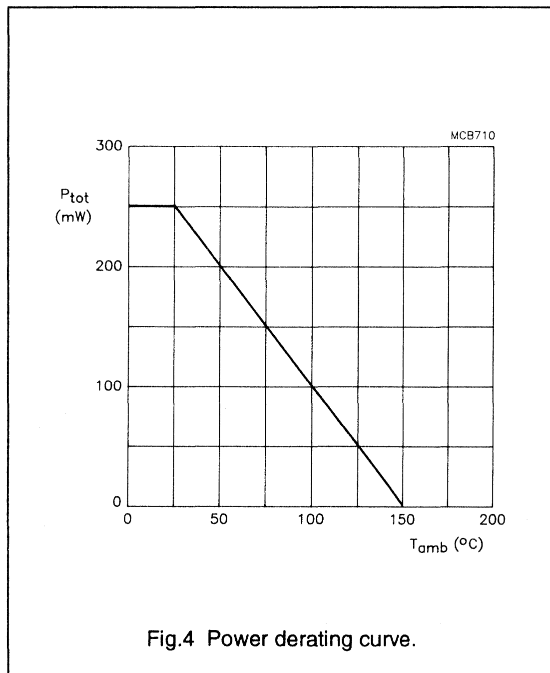


Fig.4 Power derating curve.

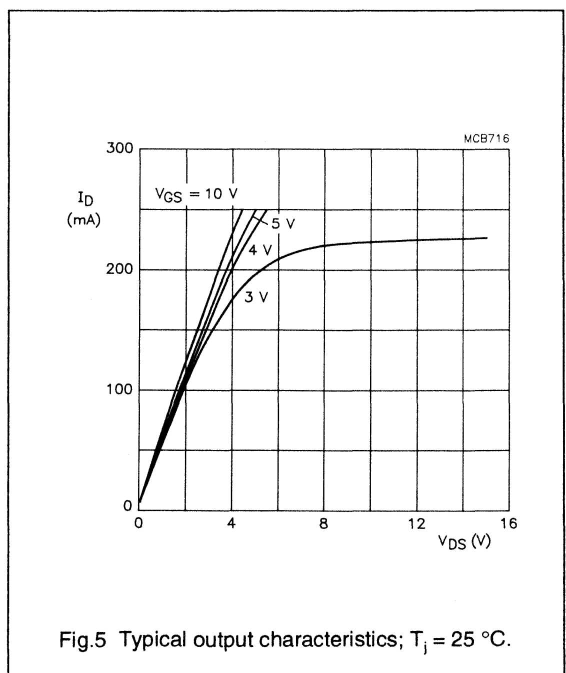


Fig.5 Typical output characteristics; T_j = 25 °C.

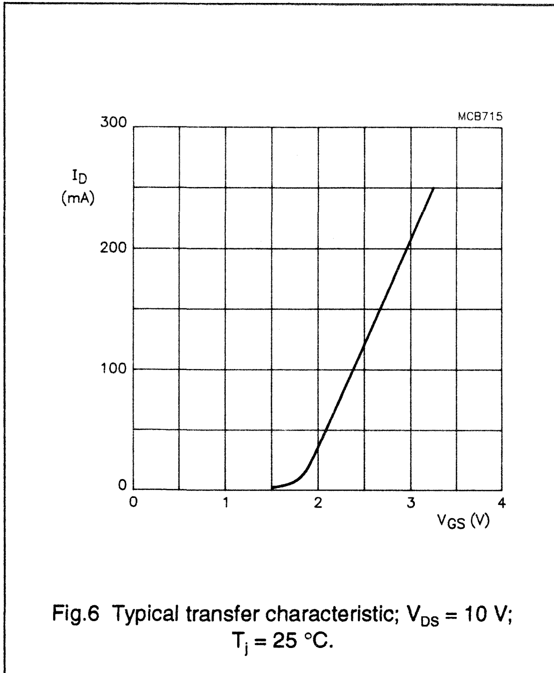


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

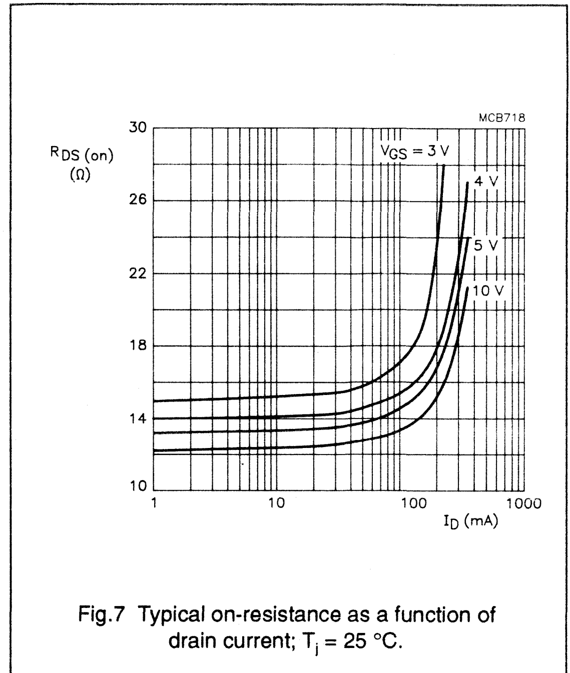


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

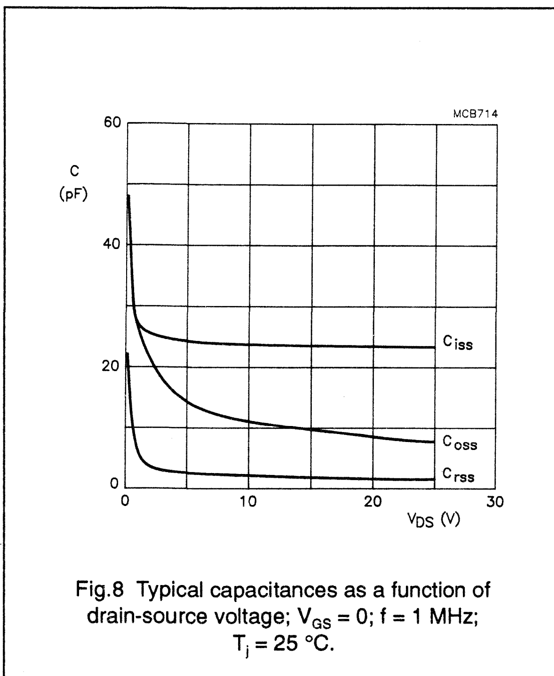
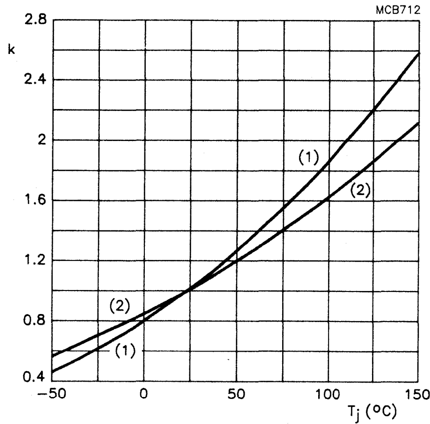


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.



(1) I_D = 150 mA; V_{GS} = 10 V.

(2) I_D = 20 mA; V_{GS} = 2.6 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^\circ C}$; typical $R_{DS(on)}$.

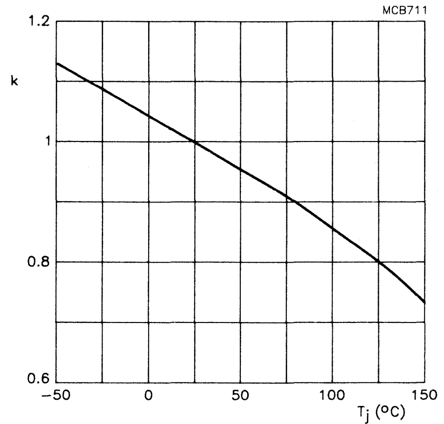


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^\circ C}$; typical $V_{GS(th)}$ at 1 mA.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ.	2.5	Ω
		max.	5.0	Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min.	100	mS
		typ.	200	mS

MECHANICAL DATA

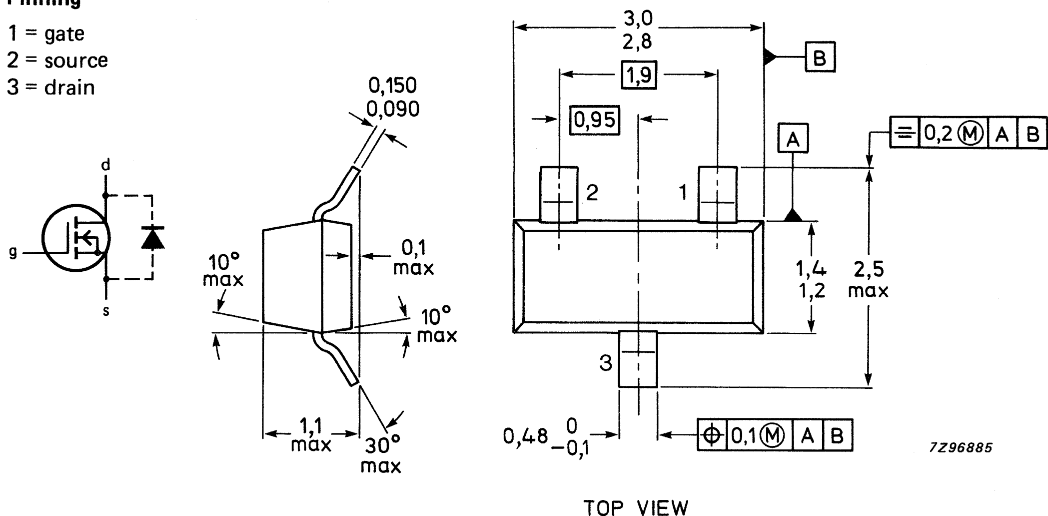
Dimensions in mm

Fig.1 SOT23.

Marking code:
PMBF170 = pKX

Pinning

1 = gate
2 = source
3 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300	mW (note 1)
		max.	250	mW (note 2)
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W
From junction to ambient (note 2)	$R_{th\ j\text{-}a}$	=	500	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	60	V
		typ.	90	V
Drain-source leakage current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	500	nA
V_{DS} = 48V; V_{GS} = 0	I_{DSS}	max.	1	μA
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10	nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	3.0	V
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ.	2.5	Ω
		max.	5.0	Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min.	100	mS
		typ.	200	mS
Input capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{iss}	typ.	25	pF
		max.	40	pF
Output capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{oss}	typ.	22	pF
		max.	30	pF
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{rss}	typ.	6	pF
		max.	10	pF

Notes

1. Mounted on ceramic substrate measuring 10 mm x 8 mm x 0.7 mm.
2. Mounted on printed-circuit board.

Switching times			
V_{GS} = 0 to 10 V; I_D = 200 mA ; V_{DD} = 50 V	t_{on}	max.	10 ns
	t_{off}	max.	15 ns

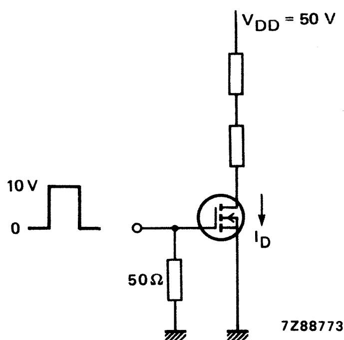


Fig.2 Switching times test circuit.

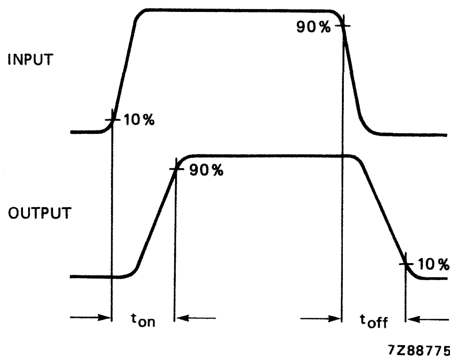


Fig.3 Input and output waveforms.

N-CHANNEL FETS

Symmetrical silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power chopper or switching applications in industry.

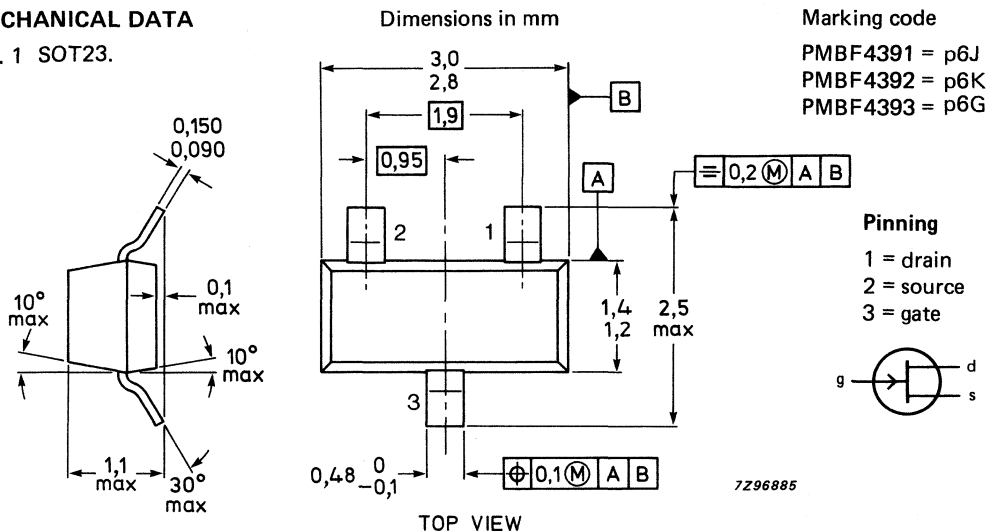
QUICK REFERENCE DATA

			PMBF4391	PMBF4392	PMBF4393	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current $V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage $V_{DS} = 20$ V; $I_D = 1$ nA	$-V_{(P)GS}$	>	4	2	0.5	V
		<	10	5	3	V
Drain-source resistance (on) at f = 1 kHz $I_D = 0$; $V_{GS} = 0$	$R_{ds\ on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz $-V_{GS} = 12$ V; $V_{DS} = 0$	C_{rs}	<	3.5	3.5	3.5	pF
Turn-off time $V_{DD} = 10$ V; $V_{GS} = 0$						
$I_D = 12$ mA; $-V_{GSM} = 12$ V	t_{off}	<	20	–	–	ns
$I_D = 6$ mA; $-V_{GSM} = 7$ V	t_{off}	<	–	35	–	ns
$I_D = 3$ mA; $-V_{GSM} = 5$ V	t_{off}	<	–	–	50	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT23.



Marking code

PMBF4391 = p6J
PMBF4392 = p6K
PMBF4393 = p6G

Pinning

1 = drain
2 = source
3 = gate

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Drain-gate voltage	V_{DGO}	max.	40 V
Gate-source voltage	$-V_{GSO}$	max.	40 V
Gate current (DC)	I_G	max.	50 mA
Total power dissipation up to T_{amb} = 40 °C*	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source voltage			
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1 V
Gate-source cut-off current			
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	<	0.1 nA
V_{DS} = 0 V; $-V_{GS}$ = 20 V; T_{amb} = 150 °C	$-I_{GSS}$	<	0.2 μA

			PMBF4391	PMBF4392	PMBF4393
Drain current					
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5 mA
		<	150	75	30 mA
Gate-source breakdown voltage					
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40 V
Gate-source cut-off voltage					
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4	2	0.5 V
		<	10	5	3 V
Drain-source voltage (on)					
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	– V
I_D = 6 mA; V_{GS} = 0	V_{DSon}	<		0.4	– V
I_D = 3 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4 V
Drain-source resistance (on)					
I_D = 0; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$r_{ds\ on}$	<	30	60	100 Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

			PMBF4391	PMBF4392	PMBF4393	
Drain cut-off current						
$-V_{GS} = 12$ V; $V_{DS} = 20$ V	I_{DSX}	<	0.1	–	–	nA
$-V_{GS} = 7$ V; $V_{DS} = 20$ V	I_{DSX}	<	–	0.1	–	nA
$-V_{GS} = 5$ V; $V_{DS} = 20$ V	I_{DSX}	<	–	–	0.1	nA
$-V_{GS} = 12$ V; $V_{DS} = 20$ V; $T_{amb} = 150\,^oC$	I_{DSX}	<	0.2	–	–	μA
$-V_{GS} = 7$ V; $V_{DS} = 20$ V; $T_{amb} = 150\,^oC$	I_{DSX}	<	–	0.2	–	μA
$-V_{GS} = 5$ V; $V_{DS} = 20$ V; $T_{amb} = 150\,^oC$	I_{DSX}	<	–	–	0.2	μA
y-parameters (common source) $V_{DS} = 20$ V; $V_{GS} = 0$; f = 1 MHz; $T_{amb} = 25\,^oC$						
Input capacitance	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS} = 12$ V	C_{rs}	<	3.5	–	–	pF
$-V_{GS} = 7$ V	C_{rs}	<	–	3.5	–	pF
$-V_{GS} = 5$ V	C_{rs}	<	–	–	3.5	pF
Switching times $V_{DD} = 10$ V; $V_{GS} = 0$						
Conditions I_D and $-V_{GSoff}$	I_D	=	12	6	3	mA
	$-V_{GS\,off}$	=	12	7	5	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

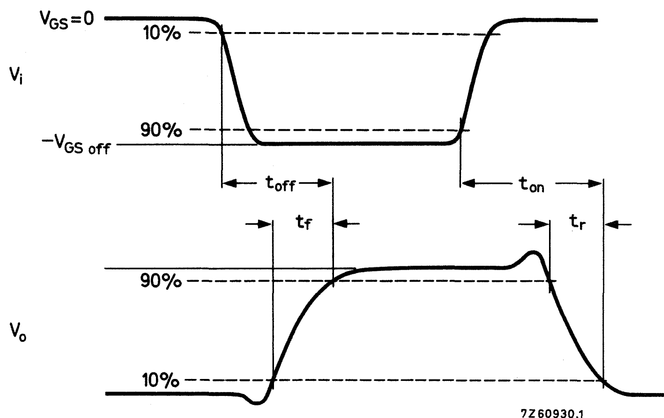
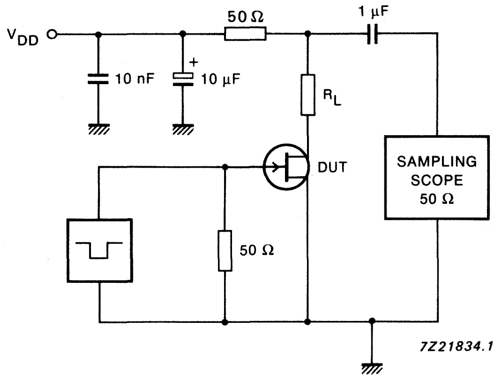


Fig.2 Switching times waveforms.



Pulse generator:

t_r	<	0.5 ns
t_f	<	0.5 ns
t_p	=	100 μs
δ	=	0.01

Oscilloscope:

R_i	=	50 Ω

Fig. 3 Test circuit.

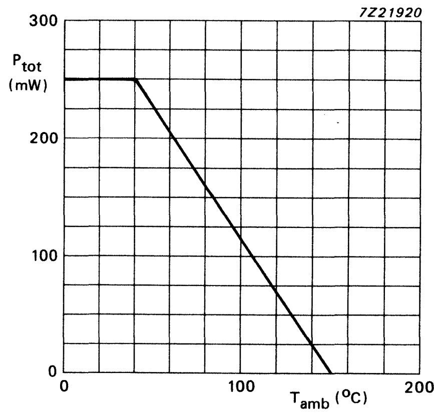


Fig.4 Power derating curve.

N-channel field-effect transistor PMBF4416; PMBF4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT23

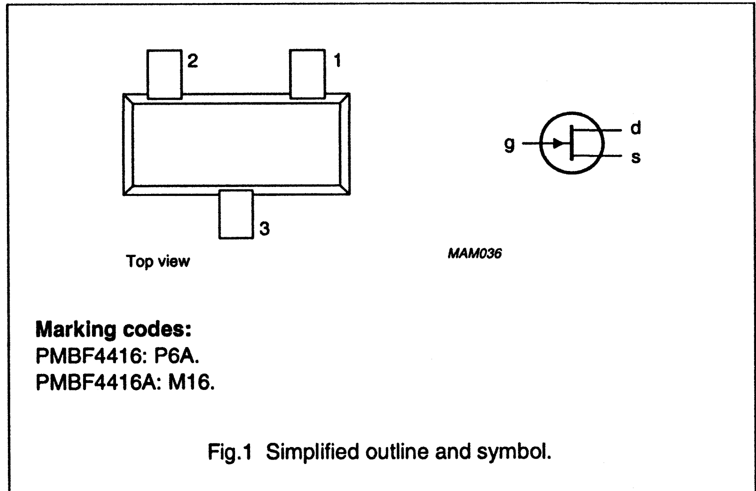
PIN	DESCRIPTION
1	source
2	drain
3	gate

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PMBF4416		–	30	V
	PMBF4416A		–	35	V
I_{DSS}	drain-source current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF4416		–	–6	V
	PMBF4416A		–2.5	–6	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS



Marking codes:
PMBF4416: P6A.
PMBF4416A: M16.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PMBF4416		–	30	V
	PMBF4416A		–	35	V
V_{GSO}	gate-source voltage				
	PMBF4416		–	–30	V
	PMBF4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	PMBF4416		–	–30	V
	PMBF4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

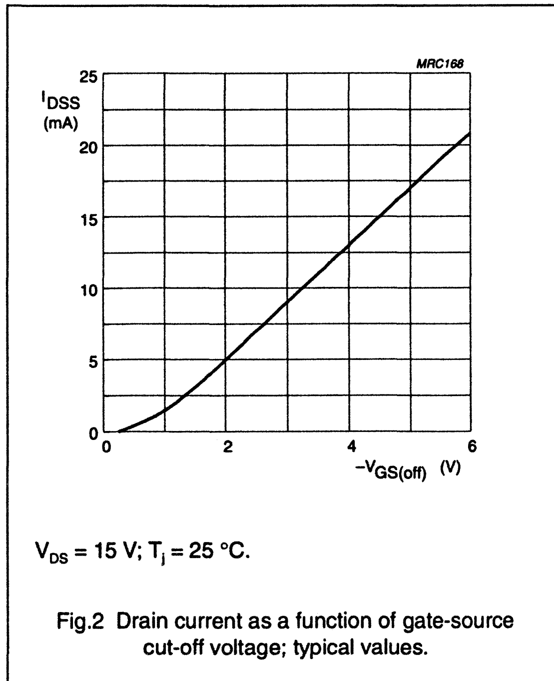
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA			
	PMBF4416		–30	–	V
	PMBF4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF4416		–	–6	V
	PMBF4416A		–2.5	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\|Y_{os}\|$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF4416		–	50	μS
	PMBF4416A		–	50	μS

DYNAMIC CHARACTERISTICS

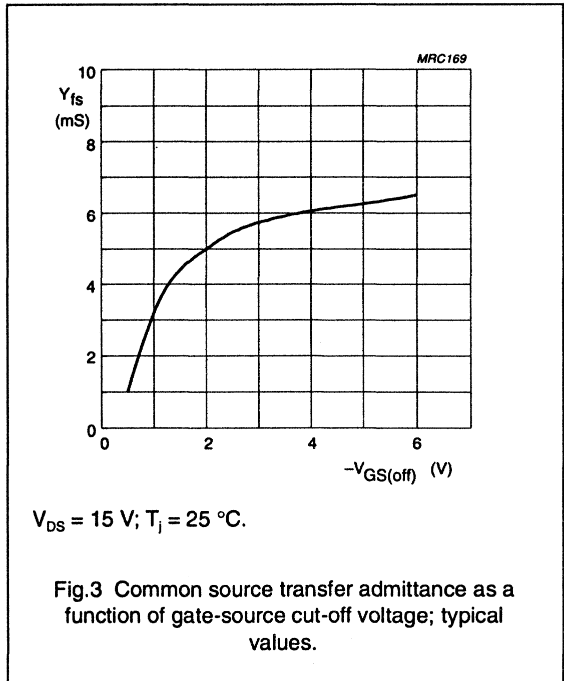
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	µS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	−8	–	µS
		f = 400 MHz	–	−100	–	µS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	µS
		f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



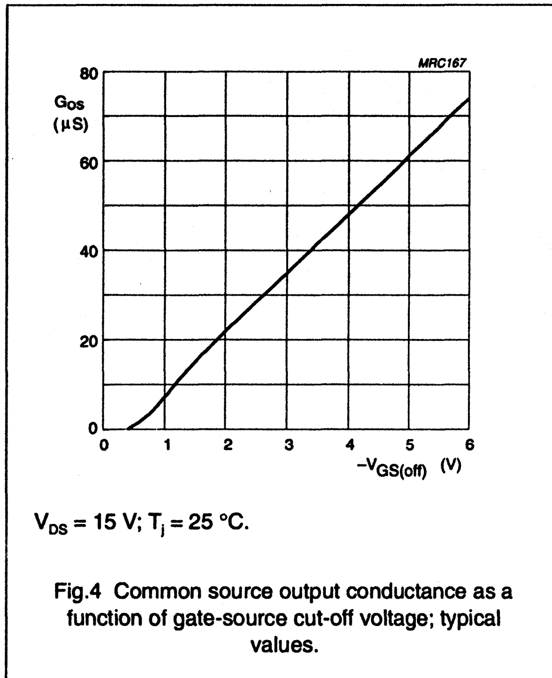
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



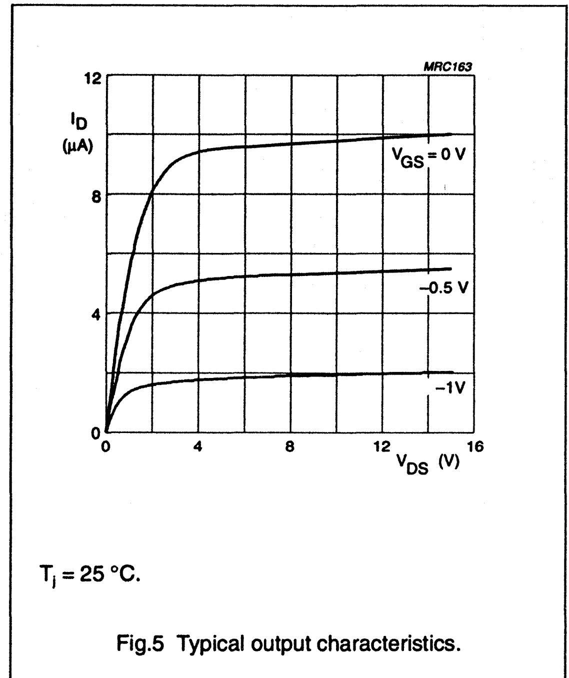
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



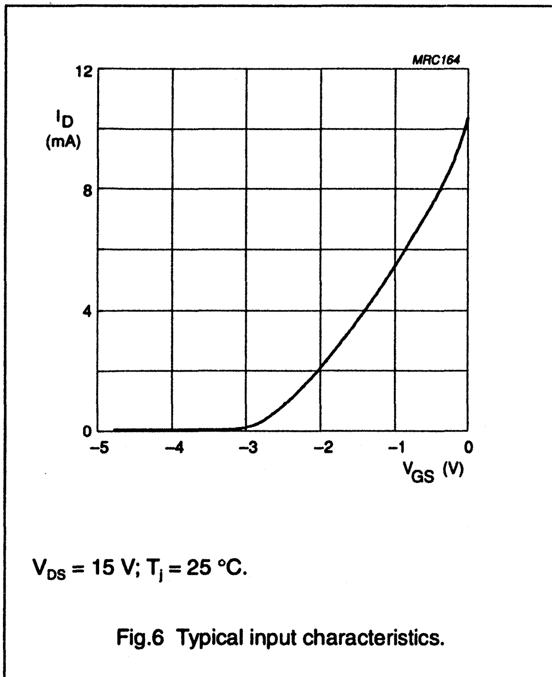
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



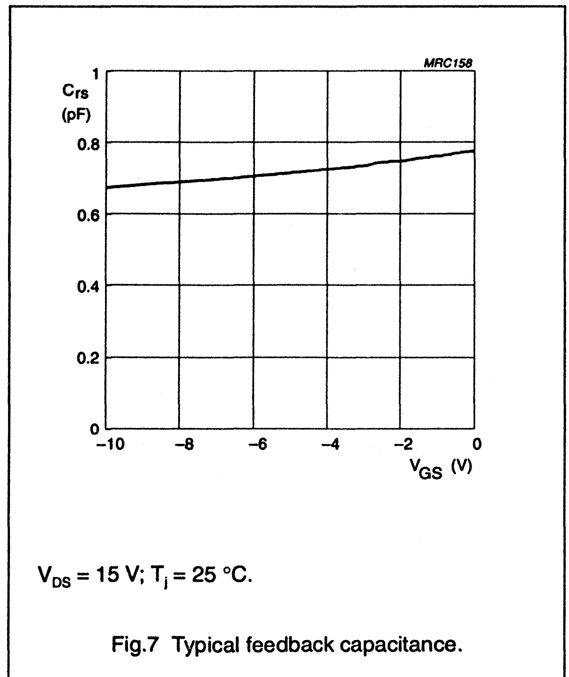
T_j = 25 °C.

Fig.5 Typical output characteristics.



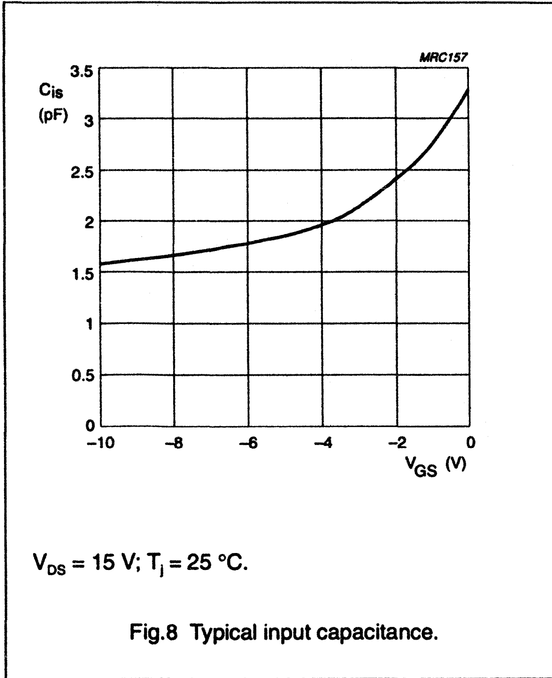
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

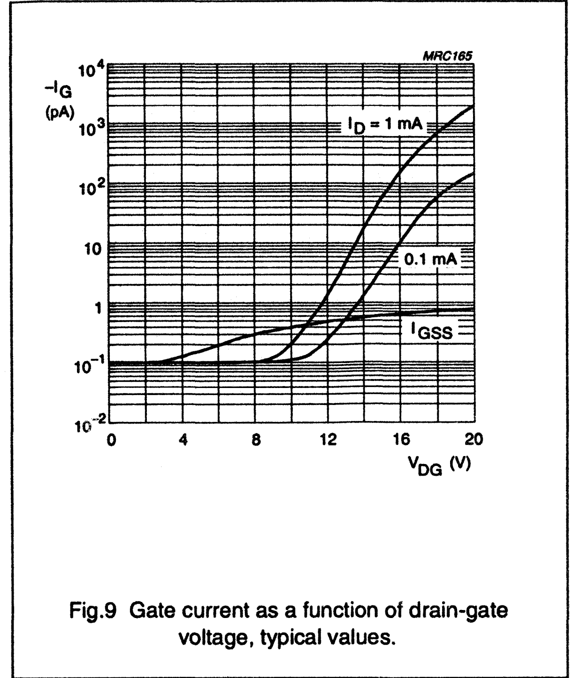


Fig.9 Gate current as a function of drain-gate voltage, typical values.

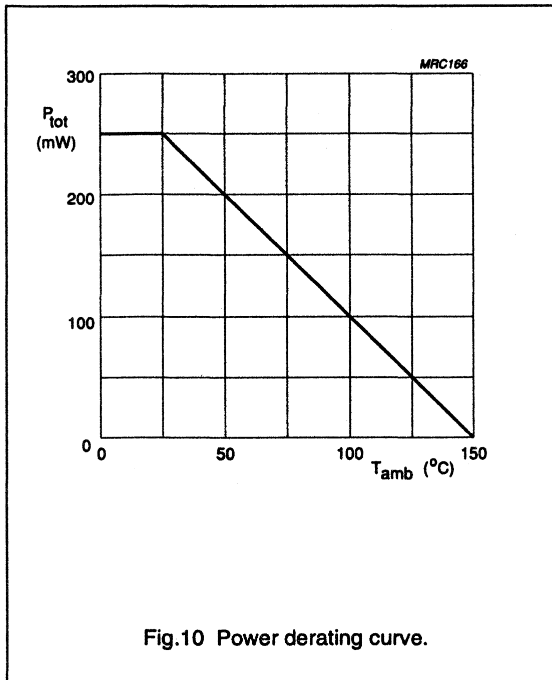
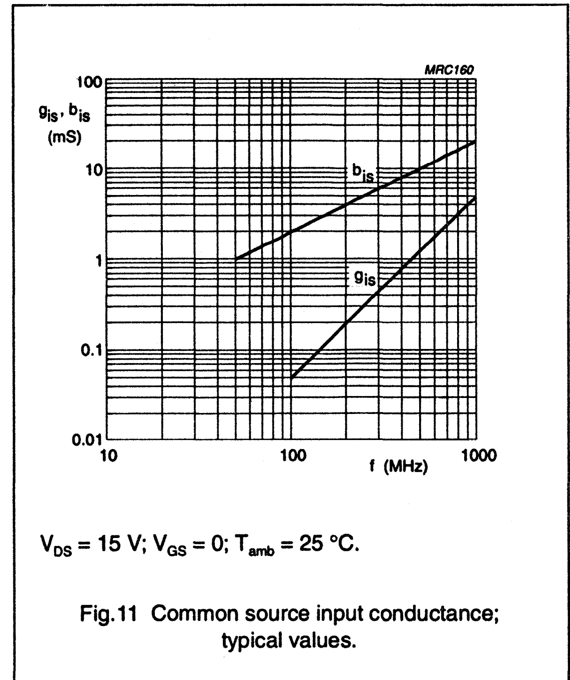
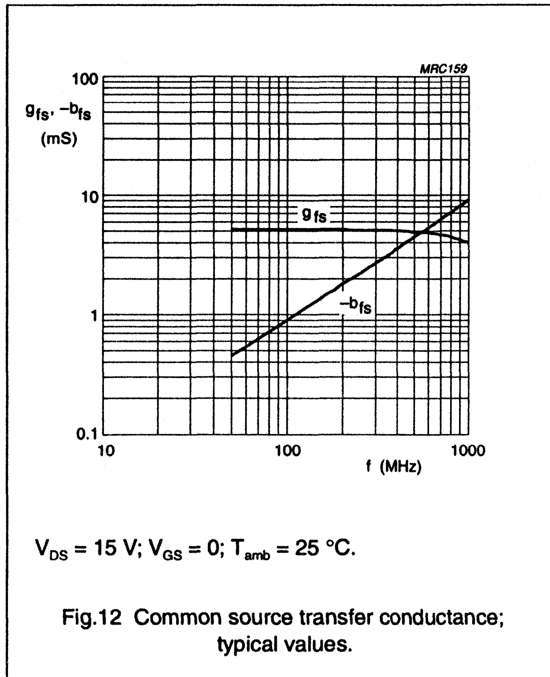


Fig.10 Power derating curve.



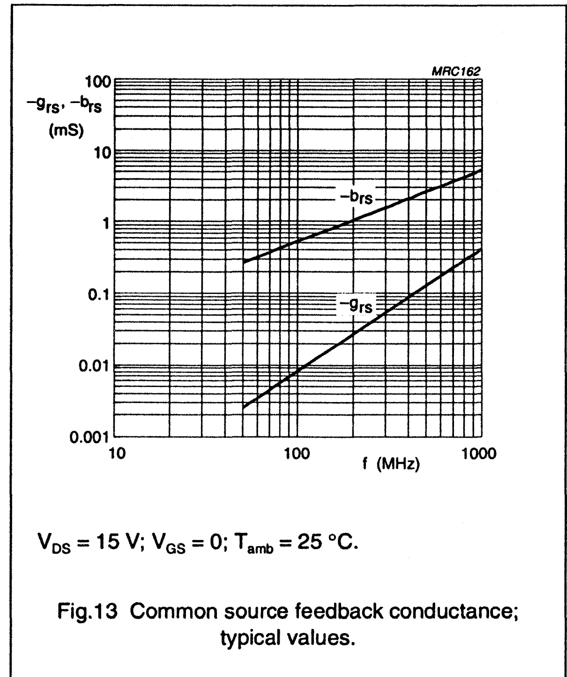
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



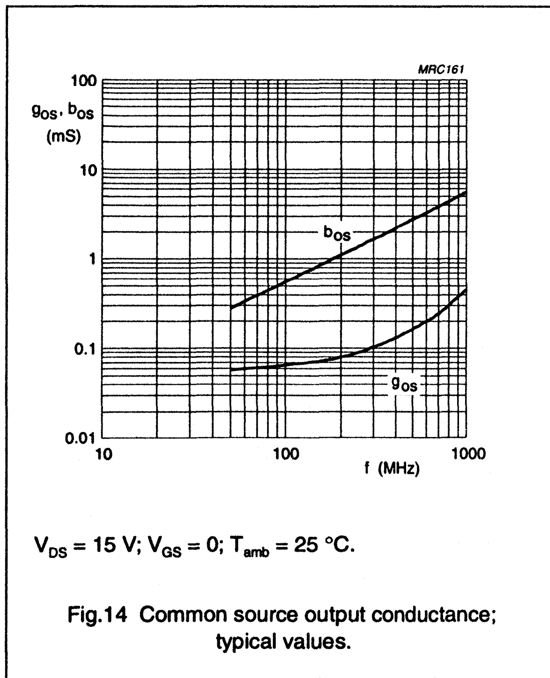
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for PMBF4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V²
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

Note

1. Parameter not extracted; default value.

N-channel field-effect transistors PMBF5484; PMBF5485; PMBF5486

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel, symmetrical, silicon junction FETs in a surface-mountable SOT23 envelope. Intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT23

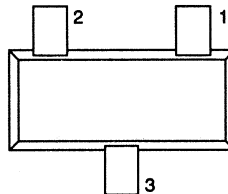
PIN	DESCRIPTION
1	source
2	drain
3	gate

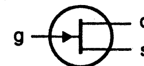
CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		1	5	mA
	PMBF5485		4	10	mA
	PMBF5486		8	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF5484		−0.3	−3	V
	PMBF5485		−0.5	−4	V
	PMBF5486		−2	−6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz			
	PMBF5484		3	6	mS
	PMBF5485		3.5	7	mS
	PMBF5486		4	8	mS





Marking codes:
PMBF5484: p6B
PMBF5485: p6M
PMBF5486: p6H

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	gate-drain voltage		–	–25	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

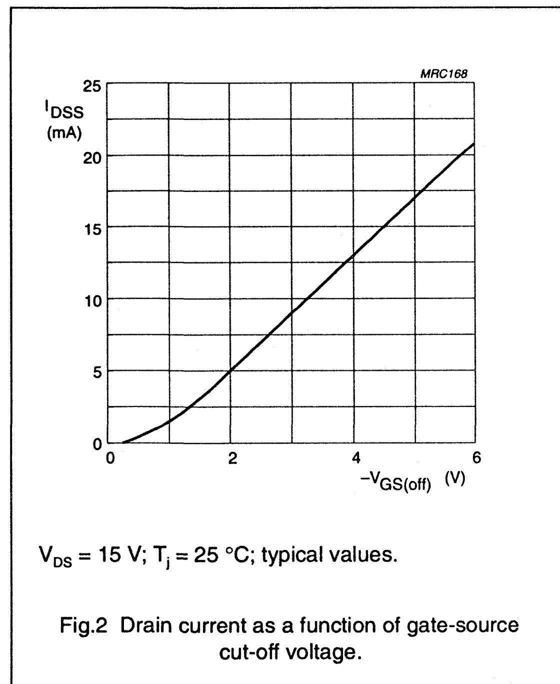
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA	–25	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		1	5	mA
	PMBF5485		4	10	mA
	PMBF5486		8	20	mA
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF5484		–0.3	–3	V
	PMBF5485		–0.5	–4	V
	PMBF5486		–2	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		3	6	mS
	PMBF5485		3.5	7	mS
	PMBF5486		4	8	mS
$\|Y_{os}\|$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		–	50	μS
	PMBF5485		–	60	μS
	PMBF5486		–	75	μS

DYNAMIC CHARACTERISTICS

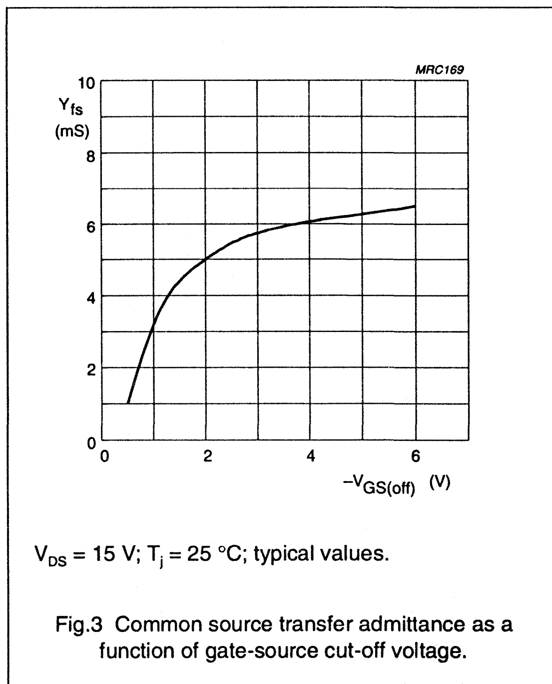
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	5	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	1	pF
g_{is}	common source input conductance					
	PMBF5484	f = 100 MHz	100	–	–	µS
	PMBF5485; PMBF5486	f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance					
	PMBF5484	f = 100 MHz	2.5	–	–	mS
	PMBF5485	f = 400 MHz	3	–	1	mS
	PMBF5486	f = 400 MHz	3.5	–	1	mS
g_{os}	common source output conductance					
	PMBF5484	f = 100 MHz	–	–	75	µS
	PMBF5485; PMBF5486	f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



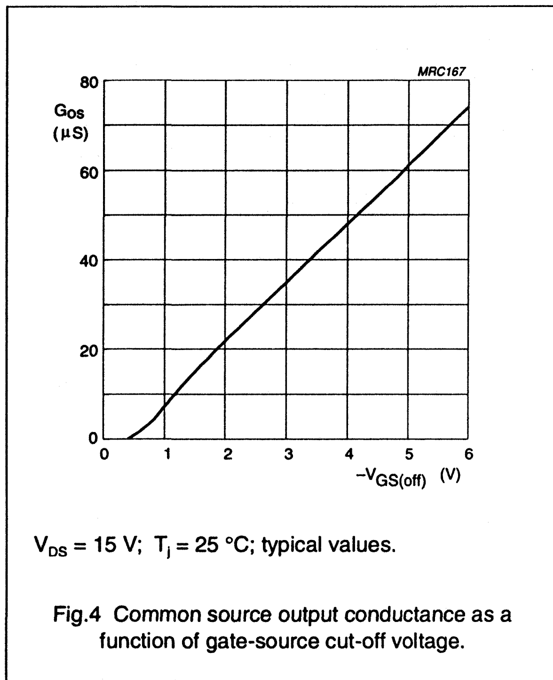
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.2 Drain current as a function of gate-source cut-off voltage.



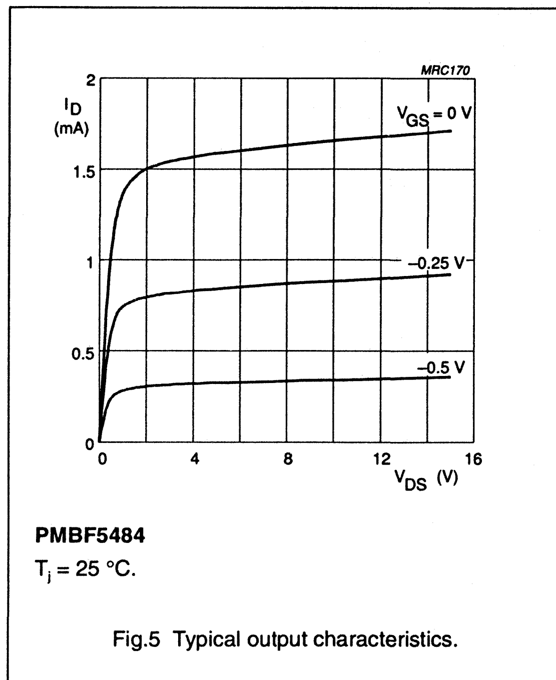
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



V_{DS} = 15 V; T_j = 25 °C; typical values.

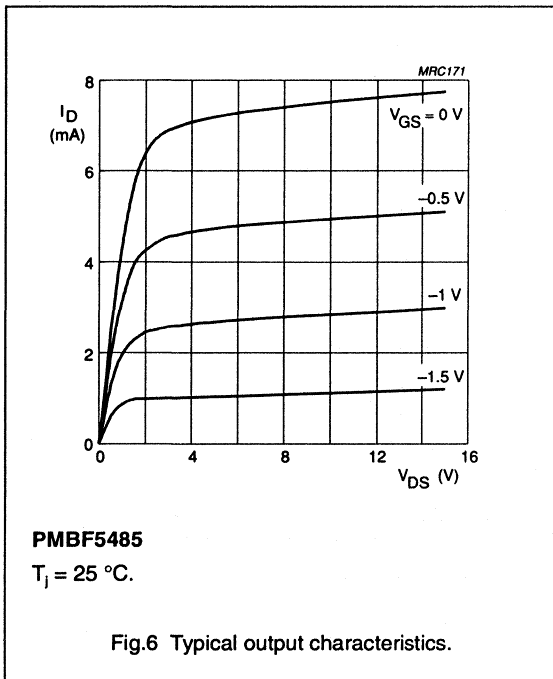
Fig.4 Common source output conductance as a function of gate-source cut-off voltage.



PMBF5484

T_j = 25 °C.

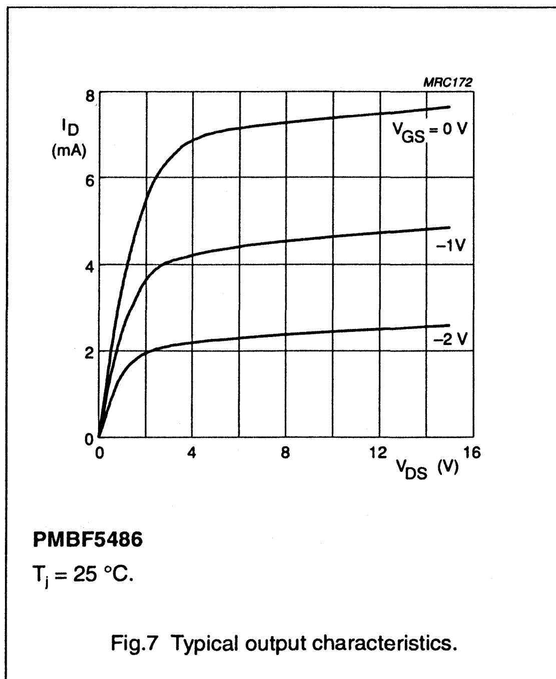
Fig.5 Typical output characteristics.



PMBF5485

T_j = 25 °C.

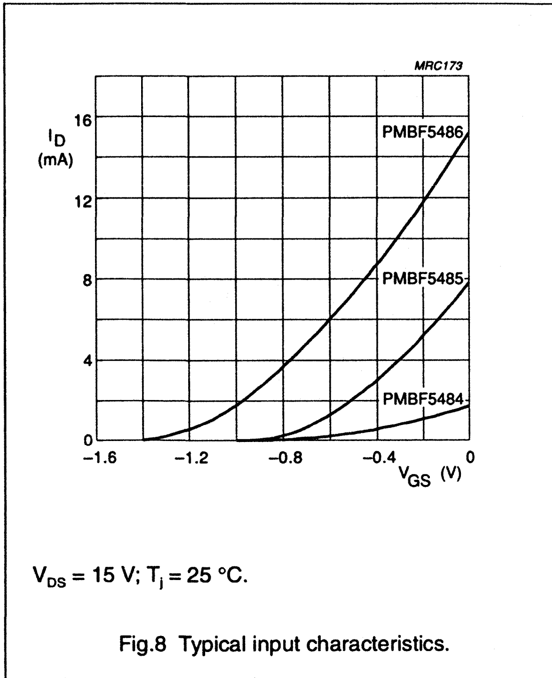
Fig.6 Typical output characteristics.



PMBF5486

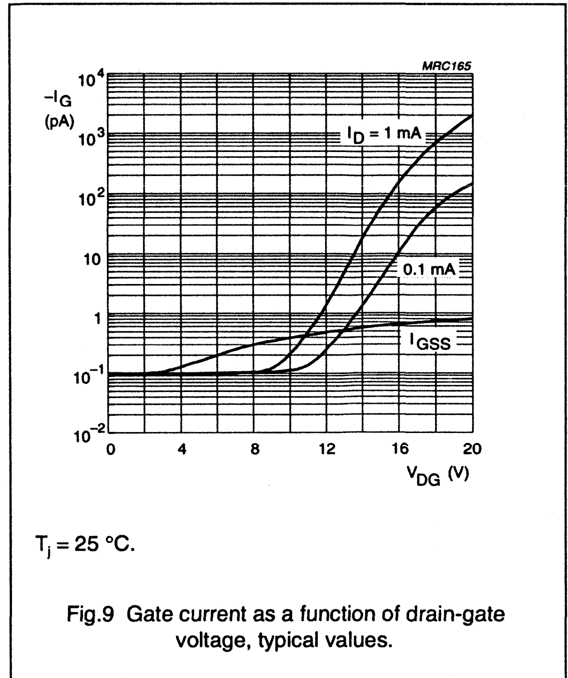
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input characteristics.



T_j = 25 °C.

Fig.9 Gate current as a function of drain-gate voltage, typical values.

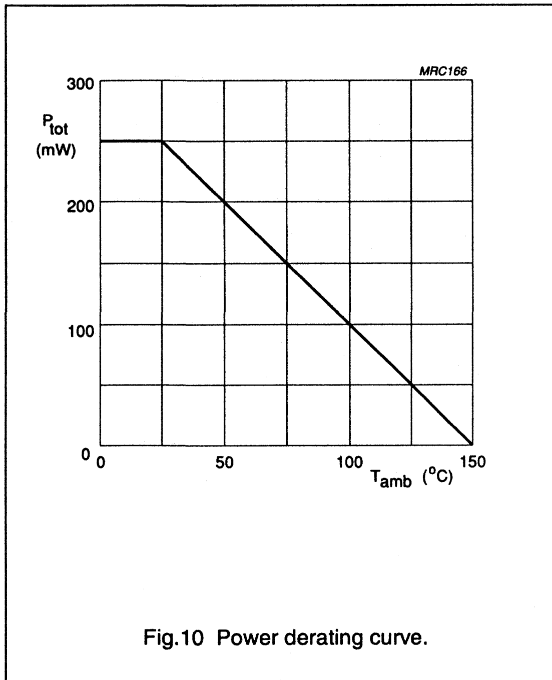
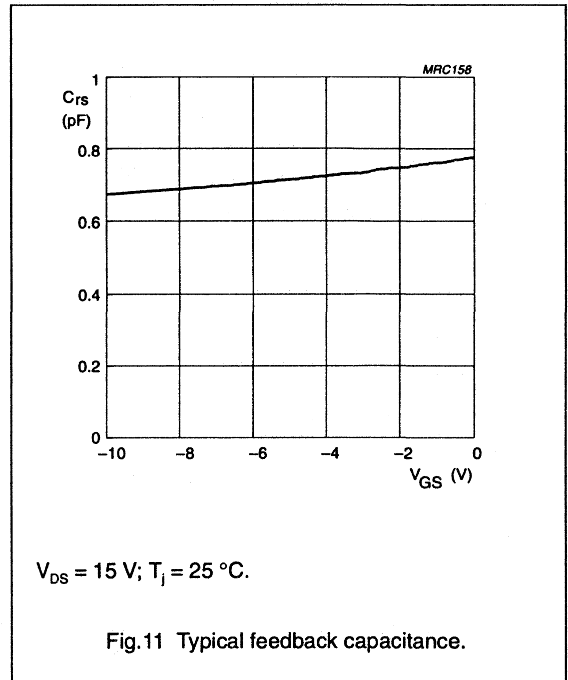
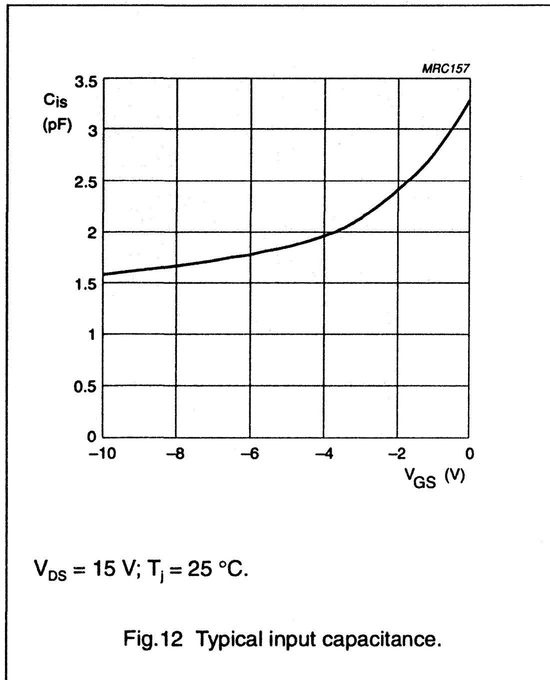


Fig.10 Power derating curve.



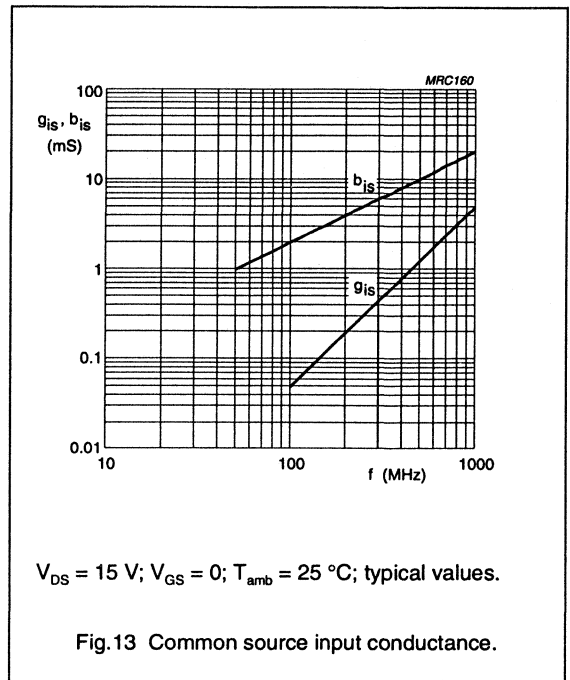
V_{DS} = 15 V; T_j = 25 °C.

Fig.11 Typical feedback capacitance.



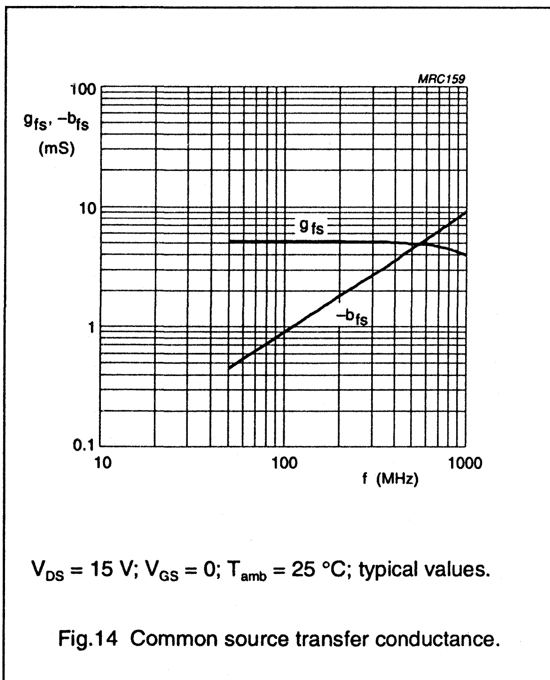
V_{DS} = 15 V; T_j = 25 °C.

Fig.12 Typical input capacitance.



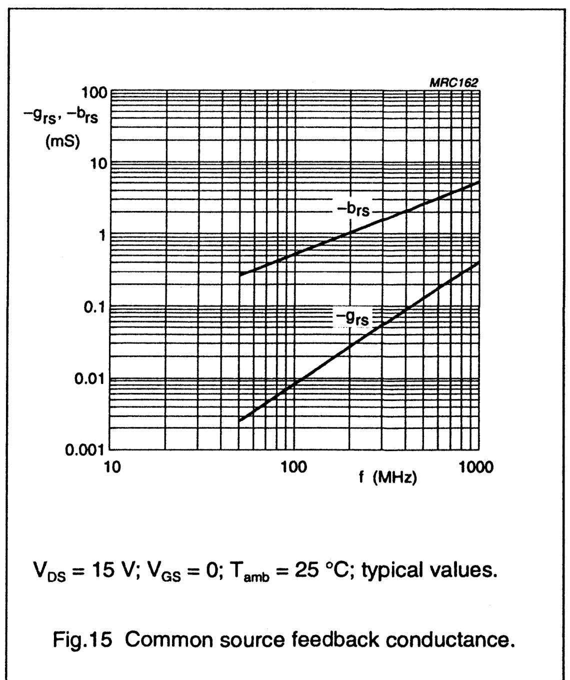
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.13 Common source input conductance.



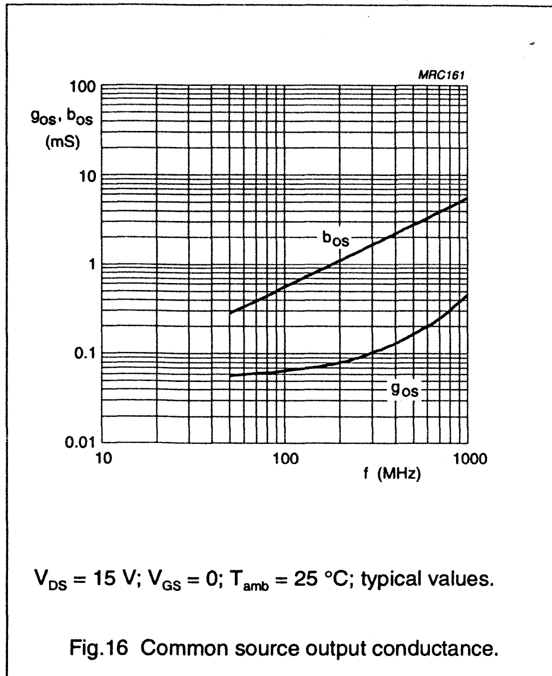
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.14 Common source transfer conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.15 Common source feedback conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.16 Common source output conductance.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

PMBFJ108/PMBFJ109/ PMBFJ110
N-channel junction FETs

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for PMBFJ108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT23 envelope. They are intended for use in applications such as analog switches, choppers and commutators, and in audio amplifiers.

PIN CONFIGURATION

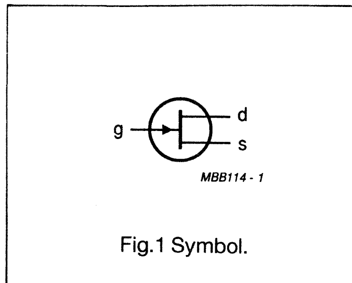


Fig.1 Symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	-	250	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Notes

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V V_{DS} = 0		-	3	nA
I_{DSX}	drain-source cut-off current	V_{GS} = −10 V V_{DS} = 5 V		-	3	nA
I_{DSS}	drain current	V_{GS} = 0 V_{DS} = 15 V	PMBFJ108 PMBFJ109 PMBFJ110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 μA V_{DS} = 5 V	PMBFJ108 PMBFJ109 PMBFJ110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V V_{DS} = 0.1 V	PMBFJ108 PMBFJ109 PMBFJ110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.2)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (PMBFJ108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (PMBFJ109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (PMBFJ110).

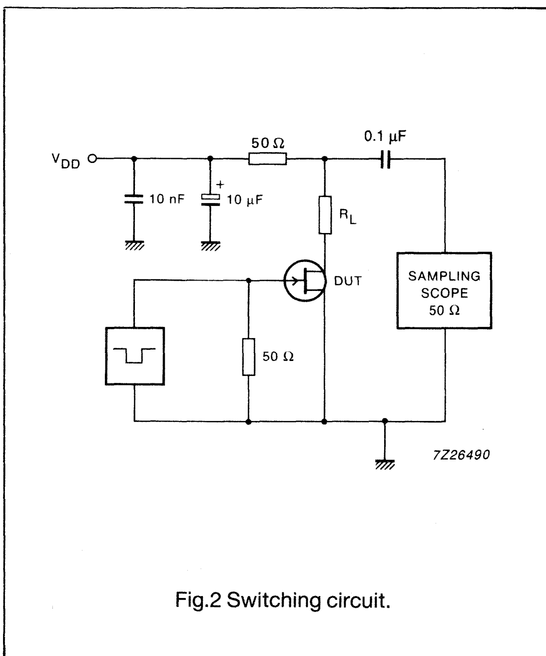


Fig.2 Switching circuit.

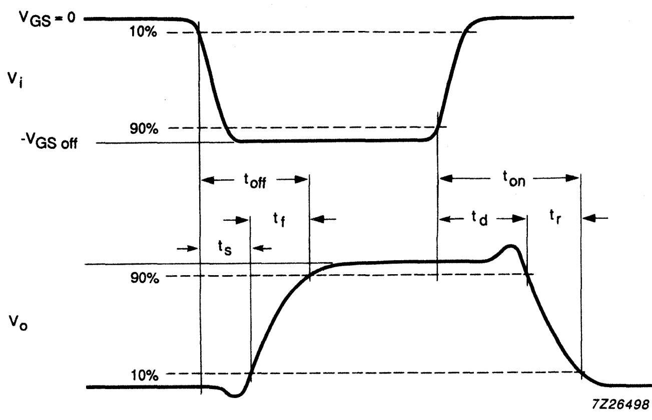


Fig.3 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

PMBFJ111/PMBFJ112/ PMBFJ113
N-channel junction FETs

FEATURES

- High-speed switching
- Low $R_{DS(on)}$ at zero gate voltage (< 30 Ω for PMBFJ111)
- Interchangeability of drain and source connections.

DESCRIPTION

Silicon n-channel junction field-effect transistors in a surface-mount SOT23 envelope. They are intended for use in applications such as analog switches, choppers, commutators, multiplexers and thin and thick film hybrids.

PIN CONFIGURATION

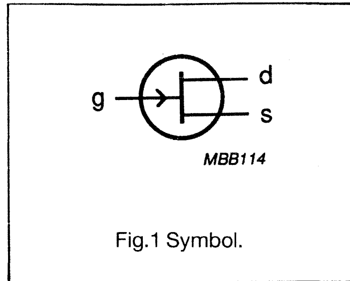


Fig.1 Symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	40	V
$-V_{GSO}$	gate-source voltage		-	40	V
$-V_{GDO}$	gate-drain voltage		-	40	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C note 1	-	300	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL CHARACTERISTICS

$T_j = P(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430	K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500	K/W

Notes

1. Mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.
2. Mounted on printed circuit board.

STATIC CHARACTERISTICS

$T_j = 25\ °C$.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$		-	1	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V	PMBFJ111 PMBFJ112 PMBFJ113	20 5 2	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ µA $V_{DS} = 0$		40	-	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ µA $V_{DS} = 5$ V	PMBFJ111 PMBFJ112 PMBFJ113	3 1 0.5	10 5 3	V
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V	PMBFJ111 PMBFJ112 PMBFJ113	- - -	30 50 100	Ω

DYNAMIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{iss}	input capacitance	$V_{DS} = 0$ $-V_{GS} = 10$ V f = 1 MHz	6	-	pF
		$V_{DS} = 0$ $-V_{GS} = 0$ f = 1 MHz $T_{amb} = 25$ °C	22	28	pF
C_{rss}	feedback capacitance	$V_{DS} = 0$ $-V_{GS} = 10$ V f = 1 MHz	3	-	pF
Switching times (see Fig.2)					
t_r	rise time	note 1	6	-	ns
t_{on}	turn-on time	note 1	13	-	ns
t_f	fall time	note 1	15	-	ns
t_{off}	turn-off time	note 1	35	-	ns

Notes

1. Test conditions for switching times are as follows:
   $V_{DD} = 10$ V, $V_{GS} = 0$ to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)} = 12$ V, $R_L = 750$ Ω (PMBFJ111);
   $-V_{GS(off)} = 7$ V, $R_L = 1550$ Ω (PMBFJ112);
   $-V_{GS(off)} = 5$ V, $R_L = 3150$ Ω (PMBFJ113).

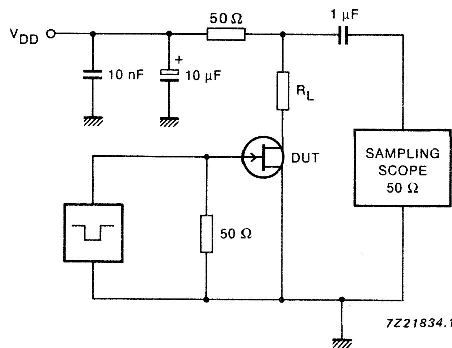


Fig.2 Switching circuit.

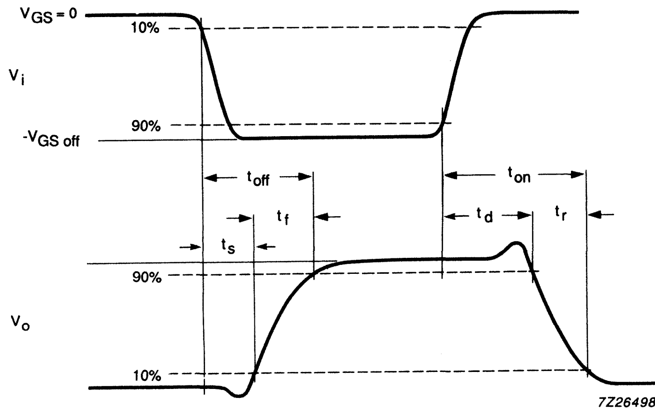


Fig.3 Input and output waveforms.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT-23 envelopes.

They are intended for application with analogue switches, choppers, commutators etc. using SMD technology.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30				V
Gate-source voltage	V_{GSO}	max.	30				V
Gate current	$-I_G$	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300				mW
			PMBFJ174	**175**	**176**	**177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

MECHANICAL DATA

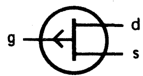
Dimensions in mm

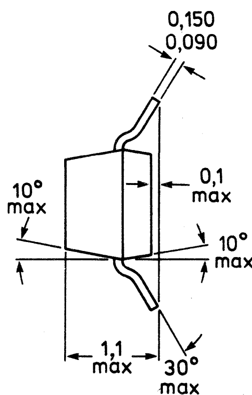
Fig. 1 SOT-23.

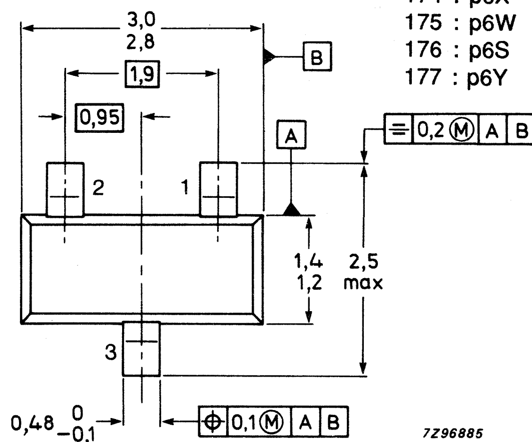
Marking codes:

174 : p6X
175 : p6W
176 : p6S
177 : p6Y

Pinning:
1 = Drain
2 = Source
3 = Gate







TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PMBFJ174	175	176	177	
Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\,off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz				
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.	8	pF
$-V_{GS}$ = V_{DS} = 0	C_{is}	typ.	30	pF
Feedback capacitance, f = 1 MHz				
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.	4	pF

Switching times (see Fig. 2 + 3)			PMBFJ174	175	176	177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage temperature	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

Rise time input voltage < 1 ns

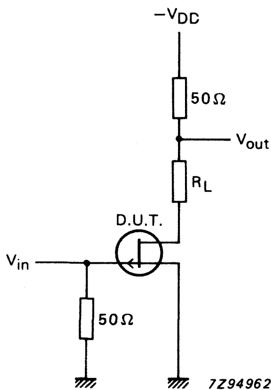


Fig. 2 Switching times test circuit

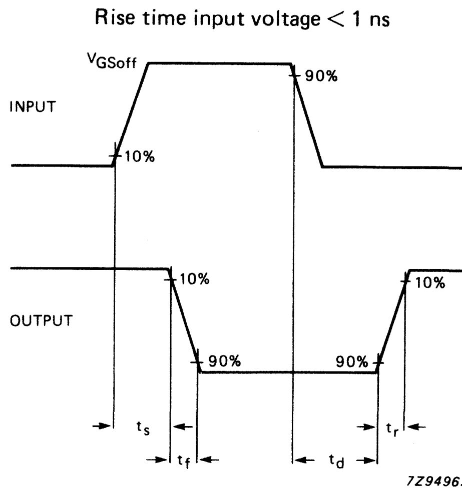


Fig. 3 Input and output waveforms

$t_d + t_r = t_{on}$

$t_s + t_f = t_{off}$

N-channel silicon field-effect transistors

PMBFJ308/309/310

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT23 envelope. They are intended for use in VHF amplifiers, the AM input stage of car radios, oscillators and mixers.

PINNING - SOT23

PIN	DESCRIPTION
1	source
2	drain
3	gate

PIN CONFIGURATION

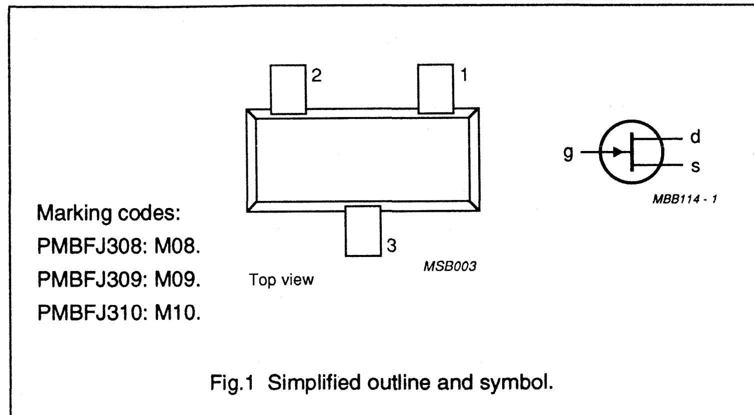


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	PMBFJ308		12	60	mA
	PMBFJ309		12	30	mA
	PMBFJ310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA			
	PMBFJ308		1	6.5	V
	PMBFJ309		1	4	V
	PMBFJ310		2	6.5	V
$\lvert Y_{fs} \rvert$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

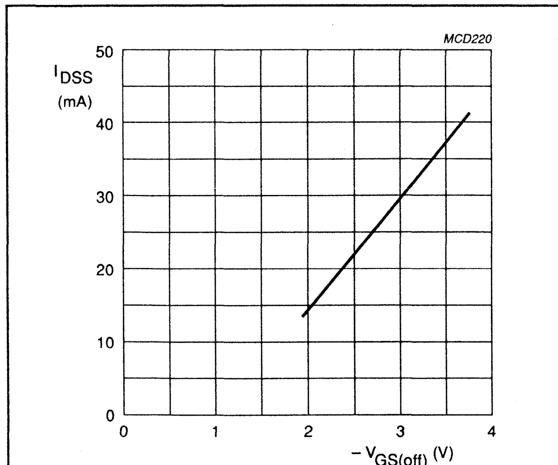
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	–	–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	PMBFJ308		12	–	60	mA
	PMBFJ309		12	–	30	mA
	PMBFJ310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	PMBFJ308		1	–	6.5	V
	PMBFJ309		1	–	4	V
	PMBFJ310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\|Y_{os}\|$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

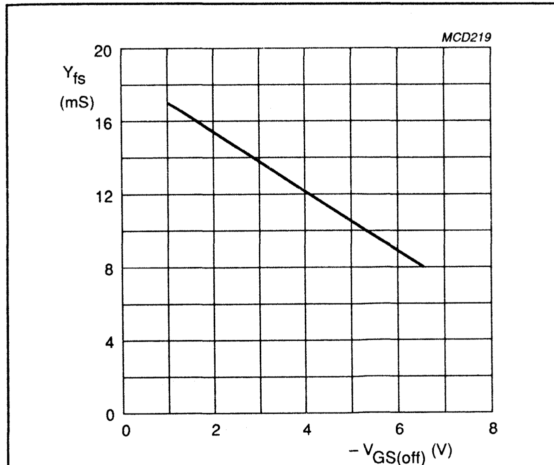
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\bar{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

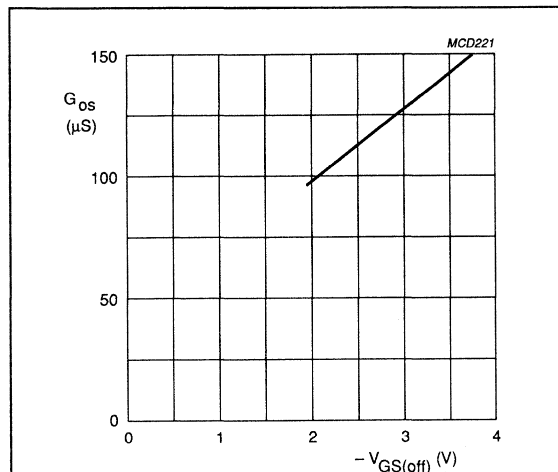
Fig.2 Drain current as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

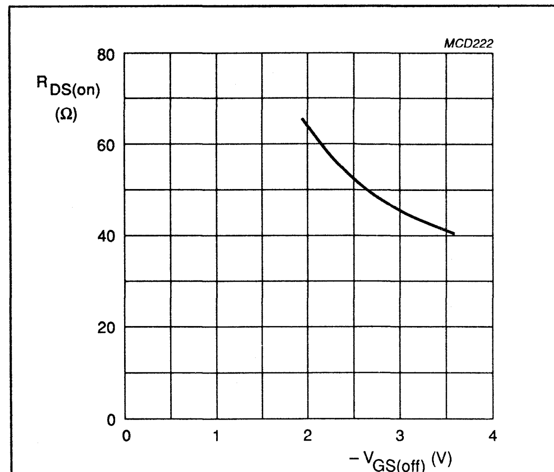
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

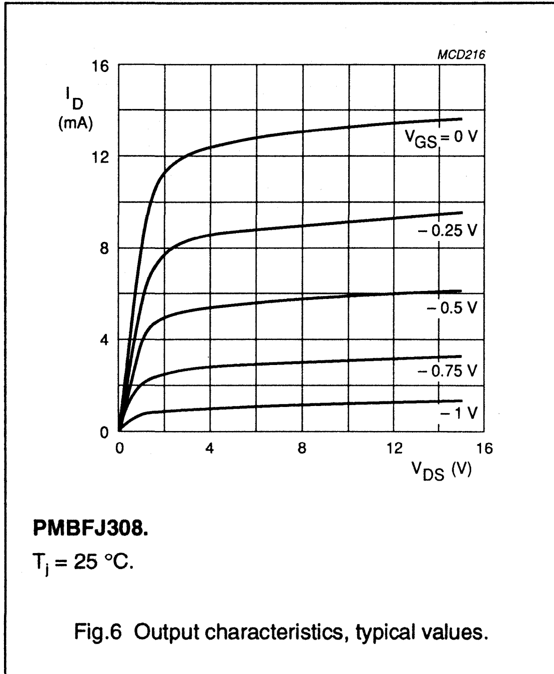
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

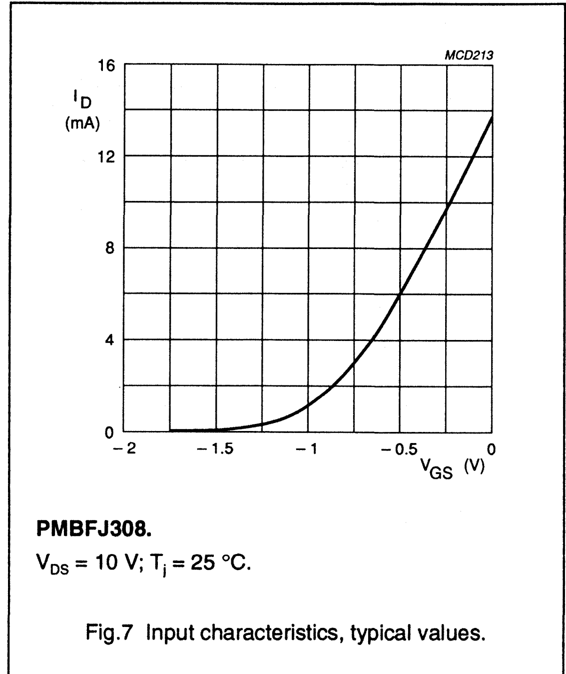
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



PMBFJ308.

T_j = 25 °C.

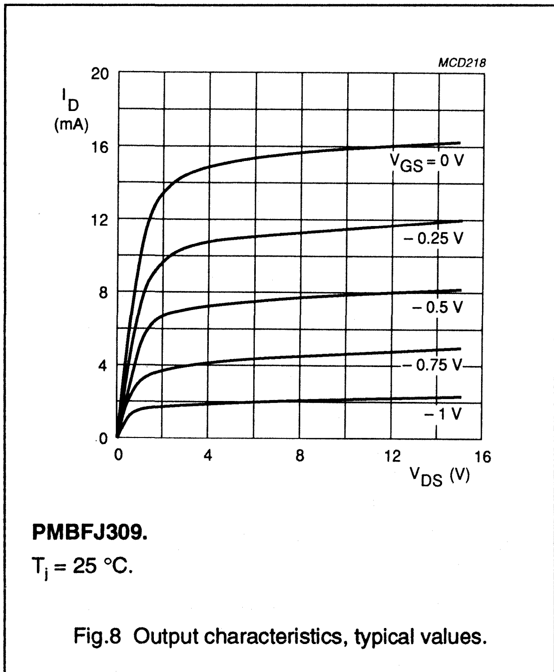
Fig.6 Output characteristics, typical values.



PMBFJ308.

V_{DS} = 10 V; T_j = 25 °C.

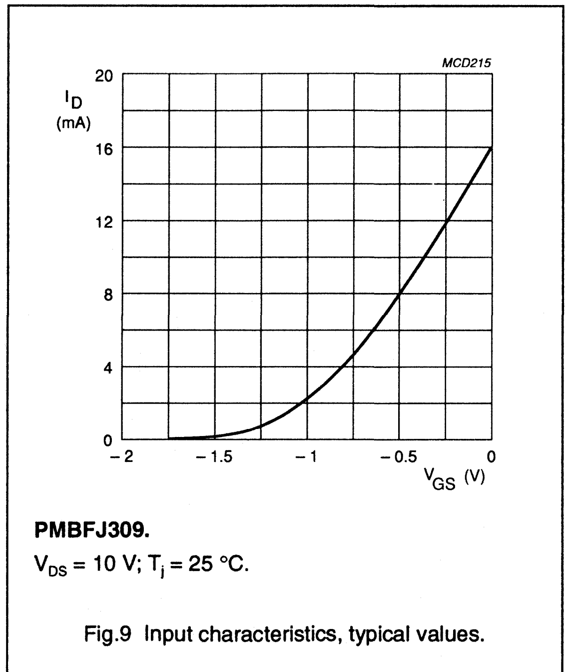
Fig.7 Input characteristics, typical values.



PMBFJ309.

T_j = 25 °C.

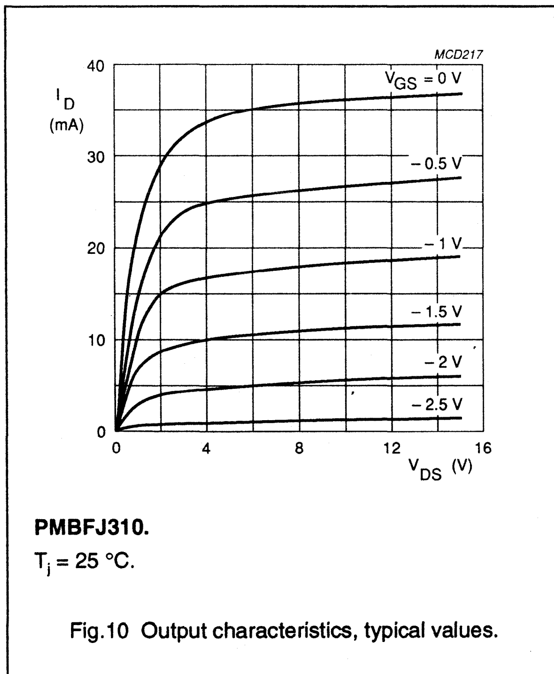
Fig.8 Output characteristics, typical values.



PMBFJ309.

V_{DS} = 10 V; T_j = 25 °C.

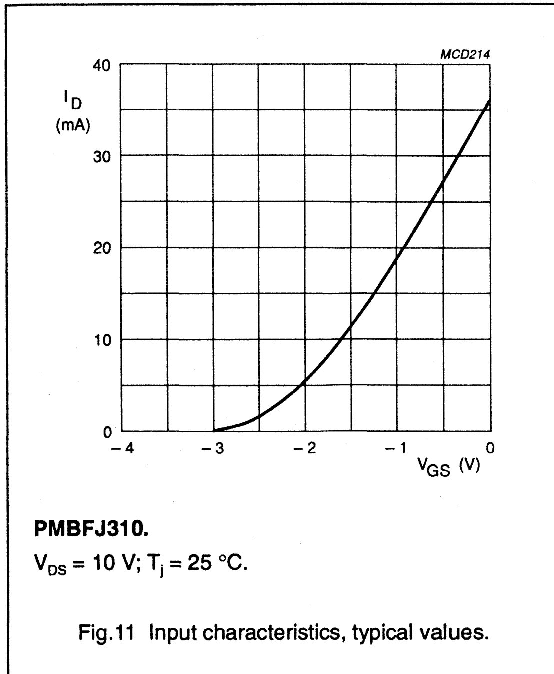
Fig.9 Input characteristics, typical values.



PMBFJ310.

T_j = 25 °C.

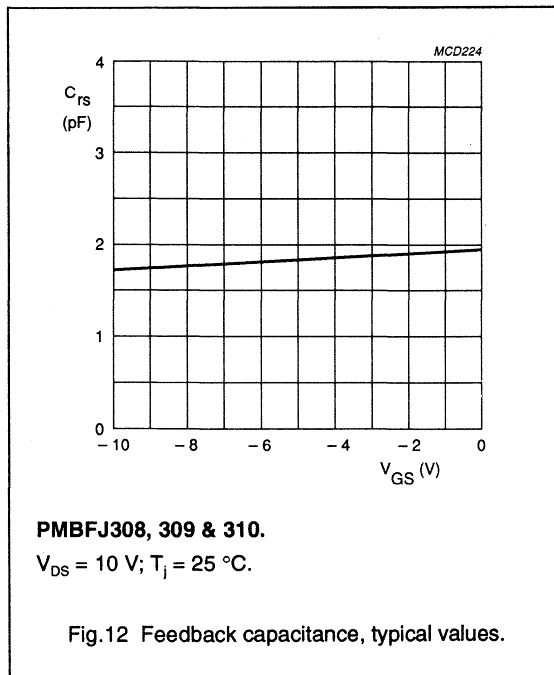
Fig.10 Output characteristics, typical values.



PMBFJ310.

V_{DS} = 10 V; T_j = 25 °C.

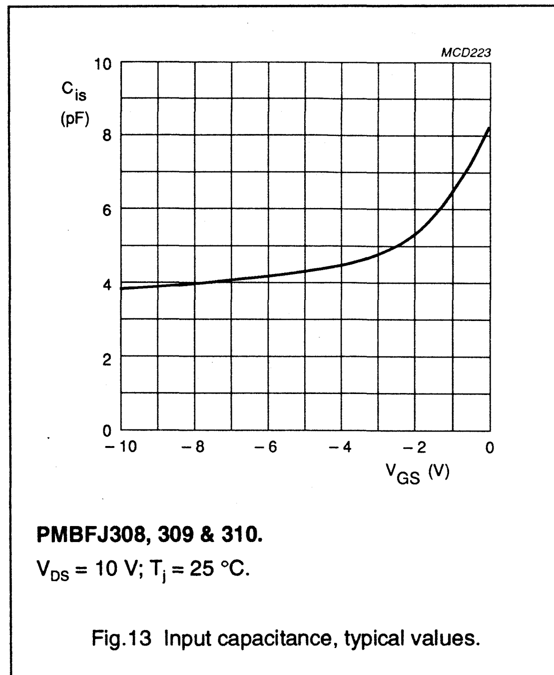
Fig.11 Input characteristics, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

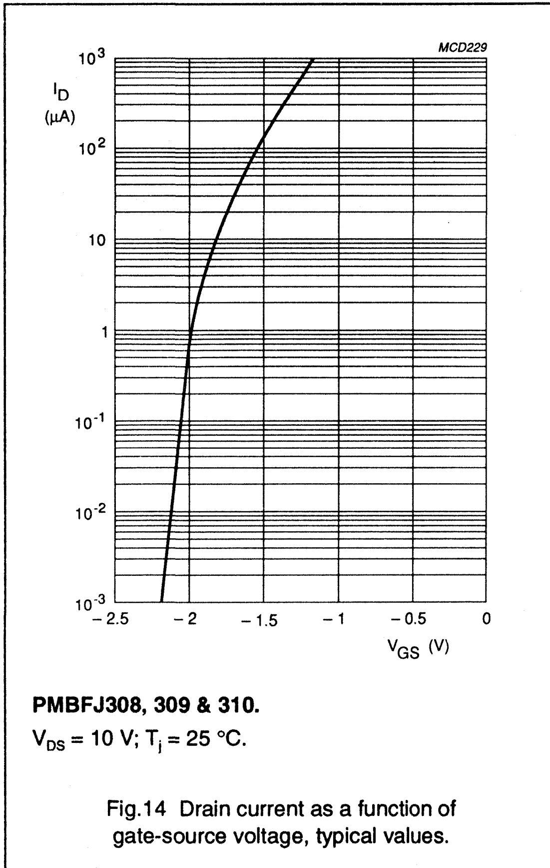
Fig.12 Feedback capacitance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

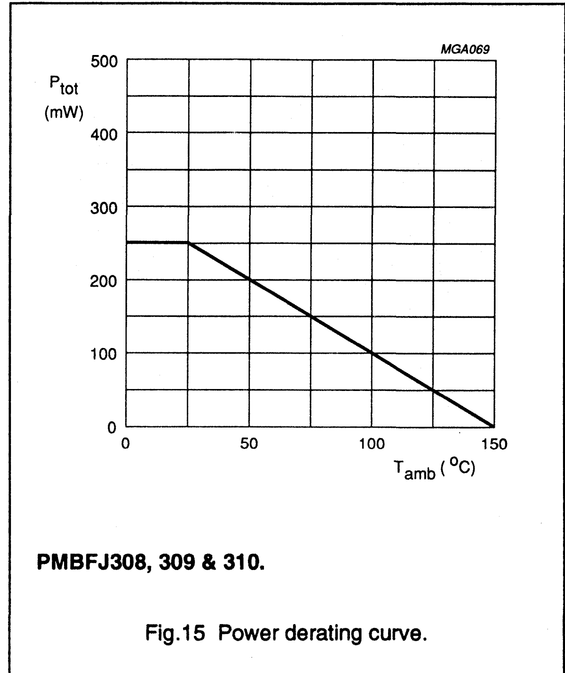
Fig.13 Input capacitance, typical values.



PMBFJ308, 309 & 310.

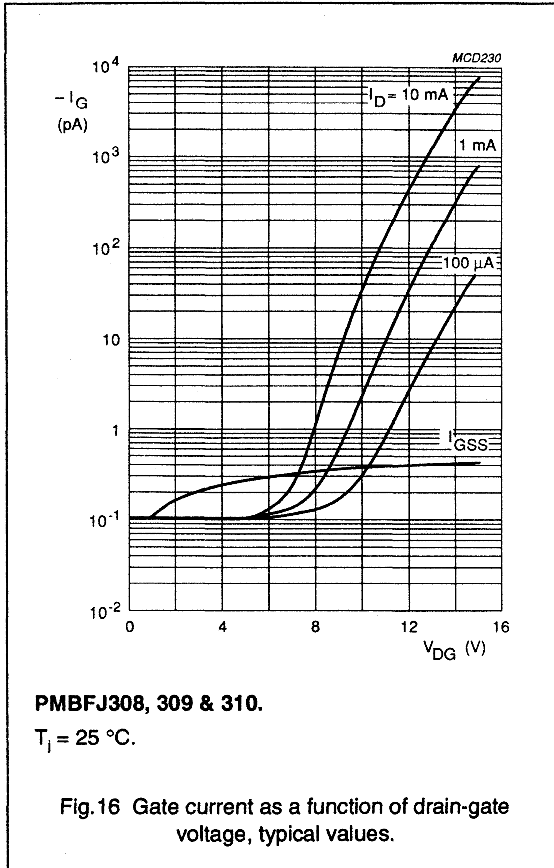
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



PMBFJ308, 309 & 310.

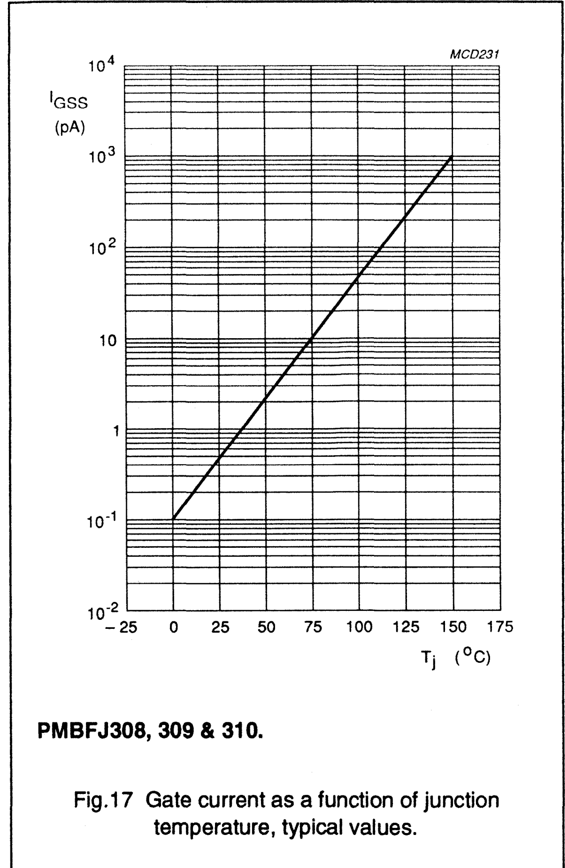
Fig.15 Power derating curve.



PMBFJ308, 309 & 310.

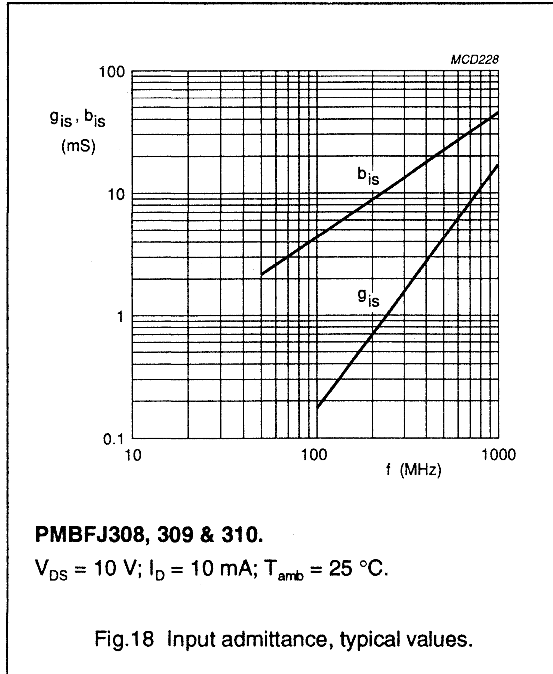
T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



PMBFJ308, 309 & 310.

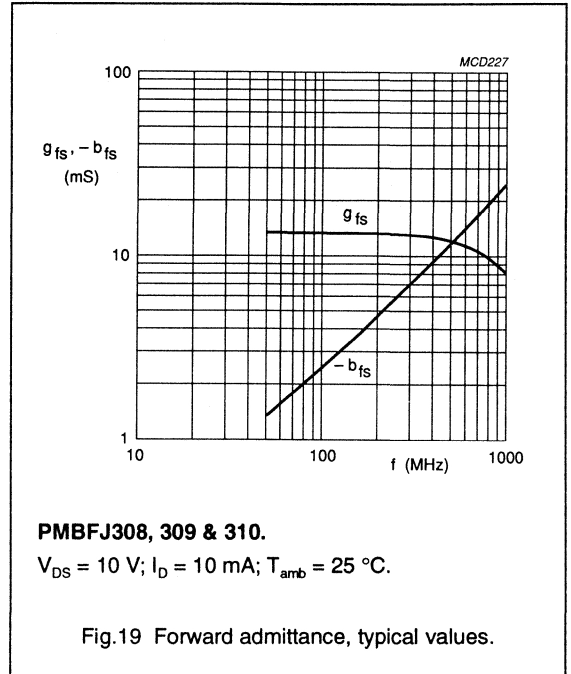
Fig.17 Gate current as a function of junction temperature, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

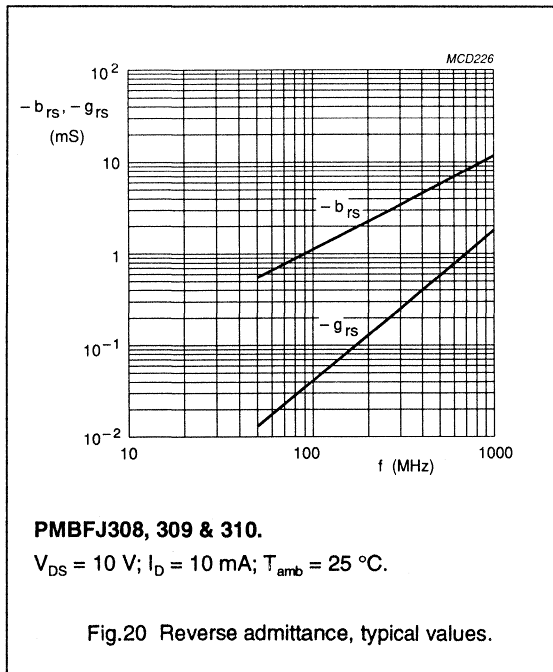
Fig.18 Input admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

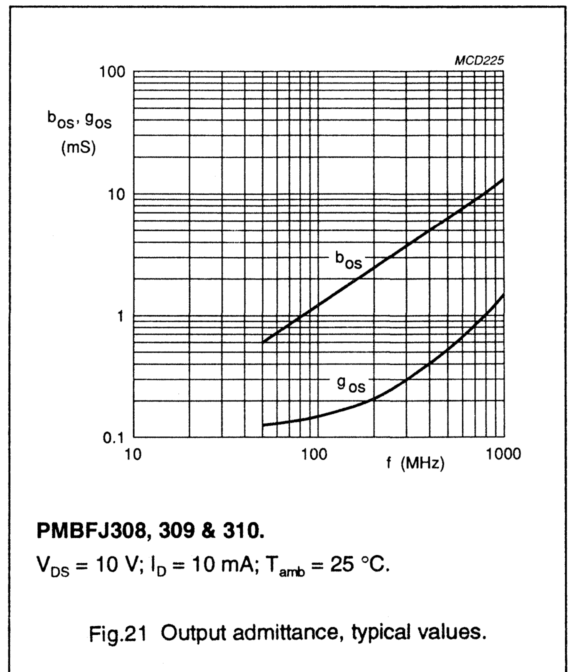
Fig.19 Forward admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		360		mW
			PN4391	PN4392	PN4393	
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
Gate-source cut-off voltage V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4	2	0.5	V
		max.	10	5	3	V
Drain-source on-resistance I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100	Ω

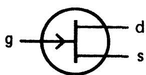
MECHANICAL DATA

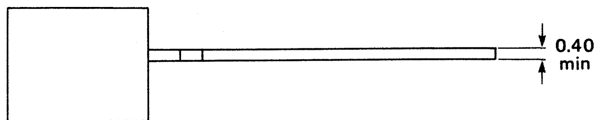
Dimensions in mm

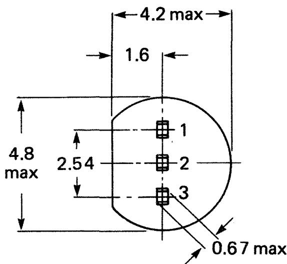
Fig.1 TO-92.

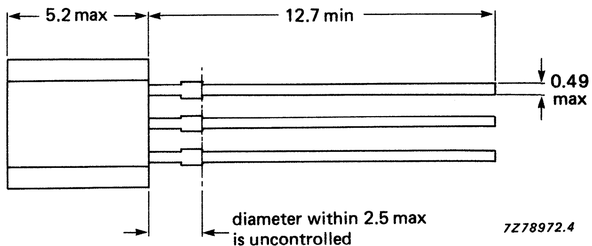
Pinning

1 = Gate
2 = Source
3 = Drain









Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Forward gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	360	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	350	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Reverse gate current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	1.0	1.0	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 100 °C	$-I_{GSS}$	max.	200	200	200	nA
Drain cut-off current						
$-V_{GS}$ = 12 V; V_{DS} = 20 V	I_{DSX}	max.	1.0			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V	I_{DSX}	max.		1.0		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V	I_{DSX}	max.			1.0	nA
$-V_{GS}$ = 12 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.	200			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.		200		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.			200	nA
Drain saturation current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
		max.	150	100	60	mA
Gate-source breakdown voltage						
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage						
V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4.0	2.0	0.5	V
		max.	10	5.0	3.0	V
Drain-source on-resistance						
I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100	Ω
Drain-source on-voltage						
V_{GS} = 0; I_D = 12 mA	$V_{DS\,on}$	max.	0.4			V
V_{GS} = 0; I_D = 6 mA	$V_{DS\,on}$	max.		0.4		V
V_{GS} = 0; I_D = 3 mA	$V_{DS\,on}$	max.			0.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Drain-source on-resistance						
V_{DS} = 0; V_{GS} = 0; f = 1 kHz; T_a = 25 °C	$R_{DS\,on}$	max.	30	60	100	Ω
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_a = 25 °C	C_{iss}	max.	16	16	16	pF
Feedback capacitance						
V_{DS} = 0; $-V_{GS}$ = 12 V; f = 1 MHz	C_{rss}	max.	5			pF
V_{DS} = 0; $-V_{GS}$ = 7 V; f = 1 MHz	C_{rss}	max.		5		pF
V_{DS} = 0; $-V_{GS}$ = 5 V; f = 1 MHz	C_{rss}	max.			5	pF
Switching times						
test conditions						
V_{DD} = 10 V; V_{GS} = 0 to $V_{GS\,off}$	I_D	=	12	6.0	3.0	mA
	$-V_{GS\,off}$	=	12	7.0	5.0	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	max.	5	5	5	ns
Turn-on time	t_{on}	max.	15	15	15	ns
Fall time	t_f	max.	15	20	30	ns
Turn-off time	t_{off}	max.	20	35	50	ns

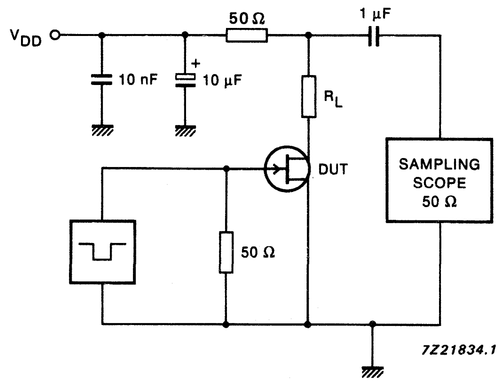


Fig.2 Switching times test circuit.

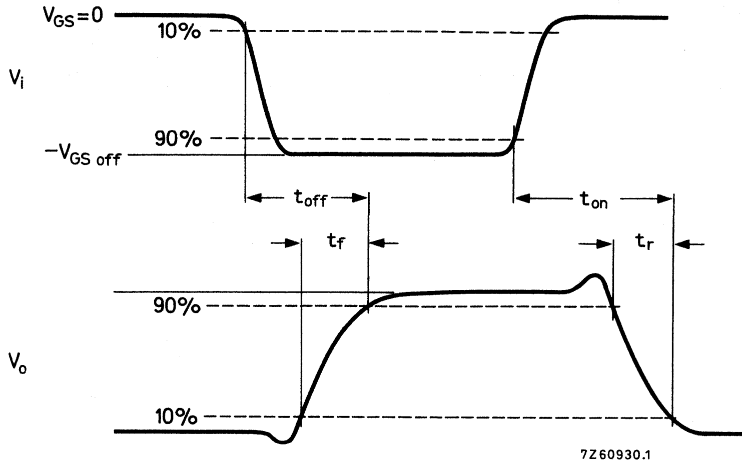


Fig.3 Input and output waveforms.

N-channel field-effect transistor PN4416; PN4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a SOT54 envelope. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT54 (TO-92).

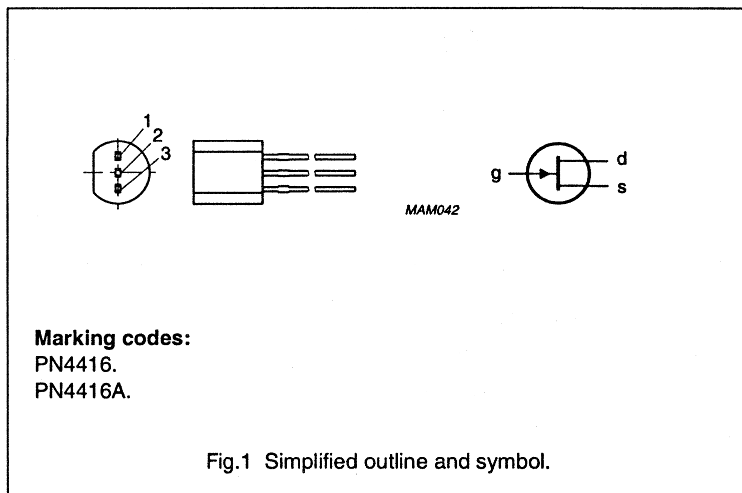
PIN	DESCRIPTION
1	gate
2	source
3	drain

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PN4416		–	30	V
	PN4416A		–	35	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	400	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PN4416		–	−6	V
	PN4416A		−2.5	−6	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS



Marking codes:
PN4416.
PN4416A.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PN4416		–	30	V
	PN4416A		–	35	V
V_{GSO}	gate-source voltage				
	PN4416		–	–30	V
	PN4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	PN4416		–	–30	V
	PN4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	350 K/W

Note

1. Mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for drain leads 10 mm^2.

STATIC CHARACTERISTICS

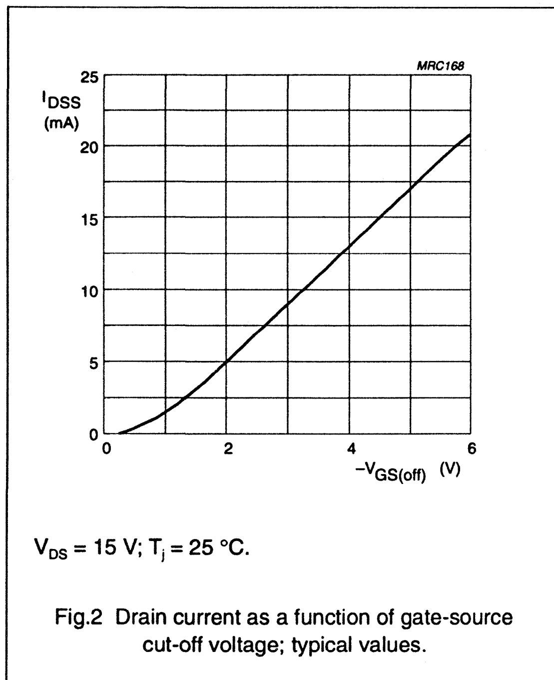
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 µA			
	PN4416		–30	–	V
	PN4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PN4416		–	–6	V
	PN4416A		–2.5	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\|Y_{os}\|$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PN4416		–	50	µS
	PN4416A		–	50	µS

DYNAMIC CHARACTERISTICS

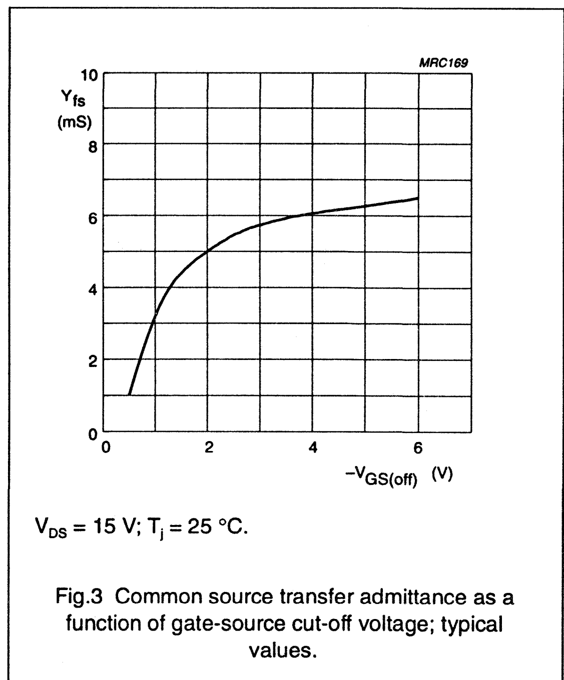
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	μS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	–8	–	μS
		f = 400 MHz	–	–100	–	μS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	μS
		f = 400 MHz	–	–	100	μS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√HZ



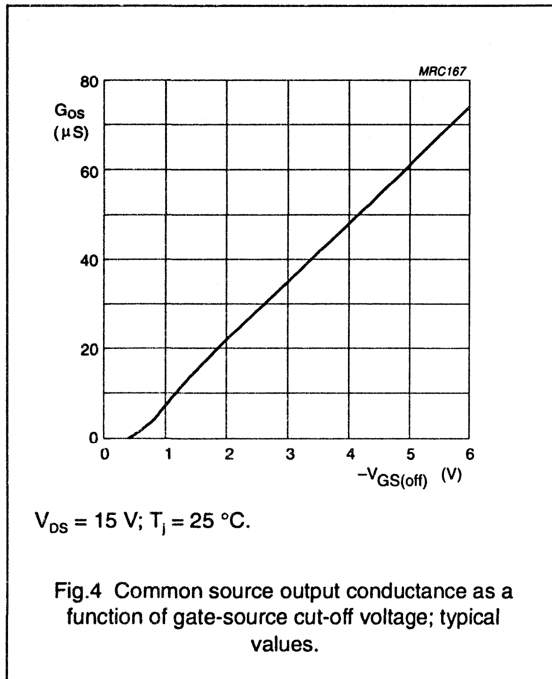
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



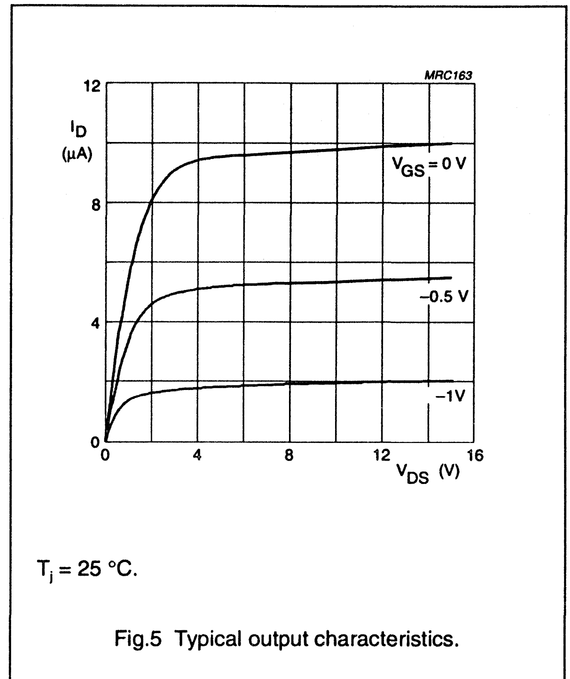
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



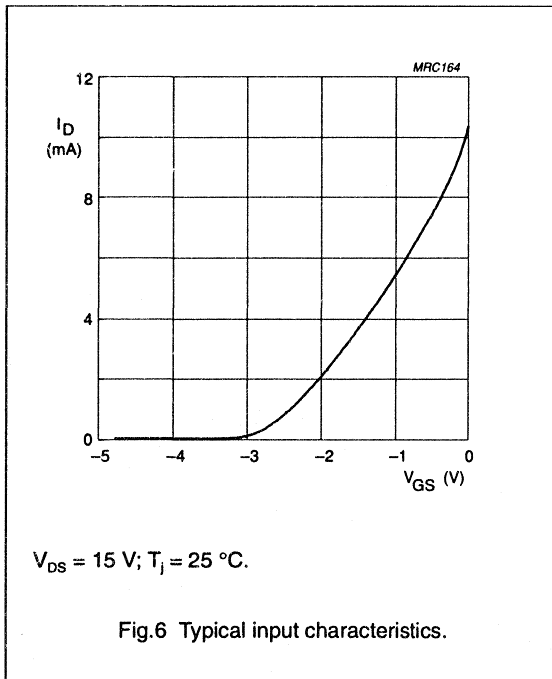
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



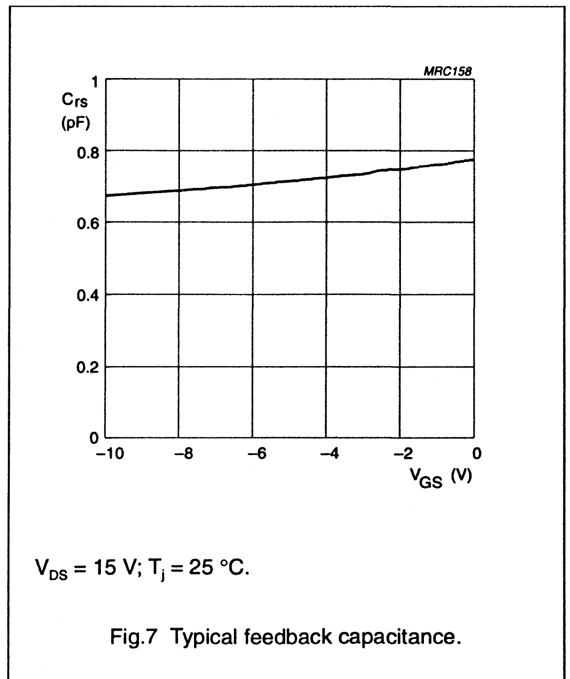
T_j = 25 °C.

Fig.5 Typical output characteristics.



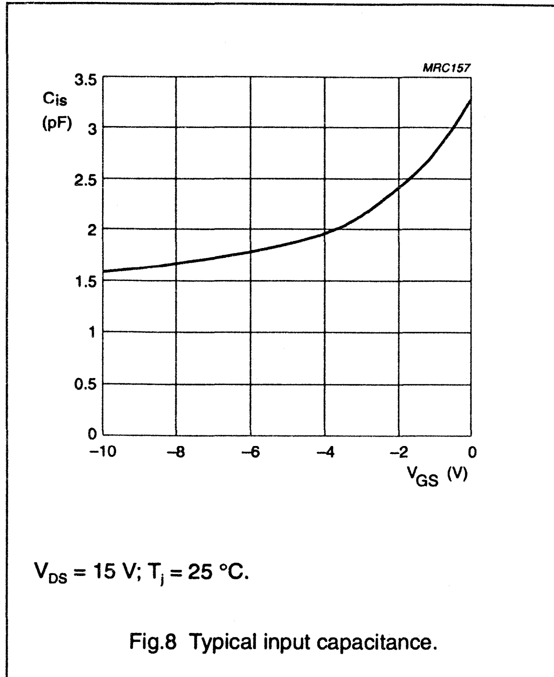
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

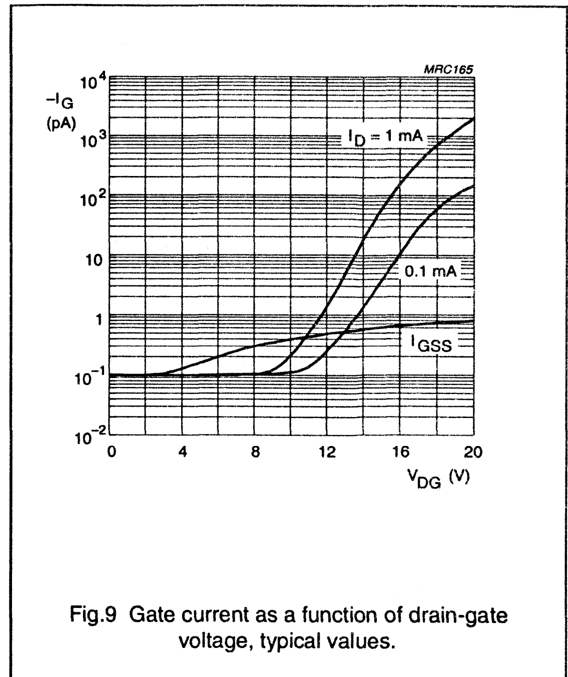


Fig.9 Gate current as a function of drain-gate voltage, typical values.

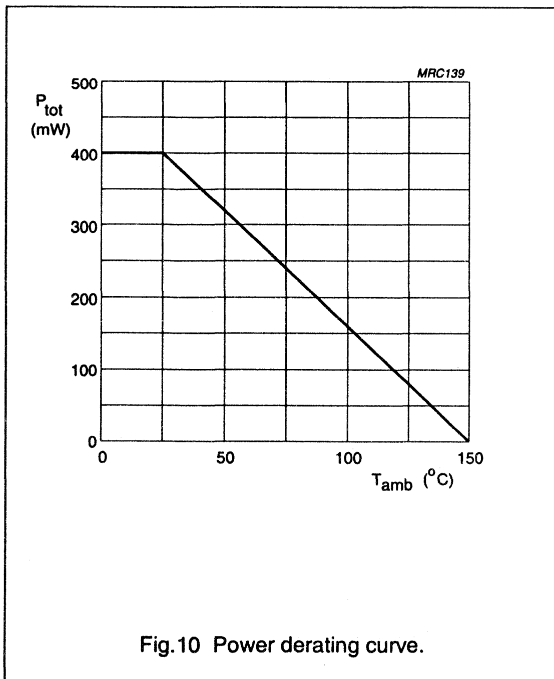
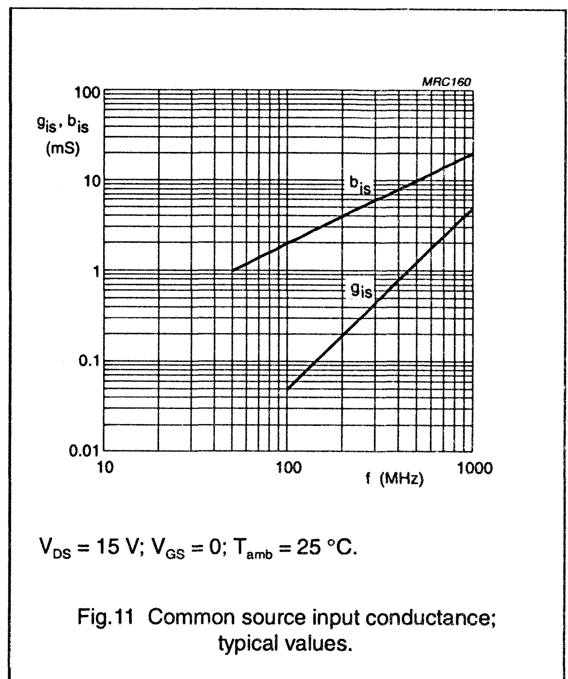
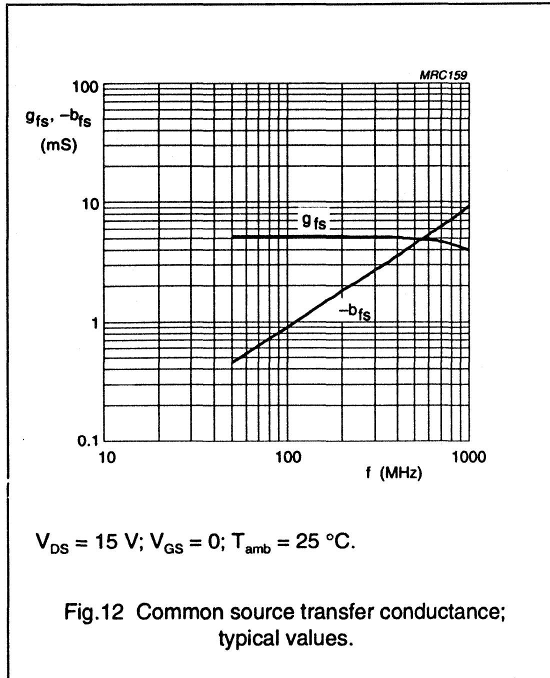


Fig.10 Power derating curve.



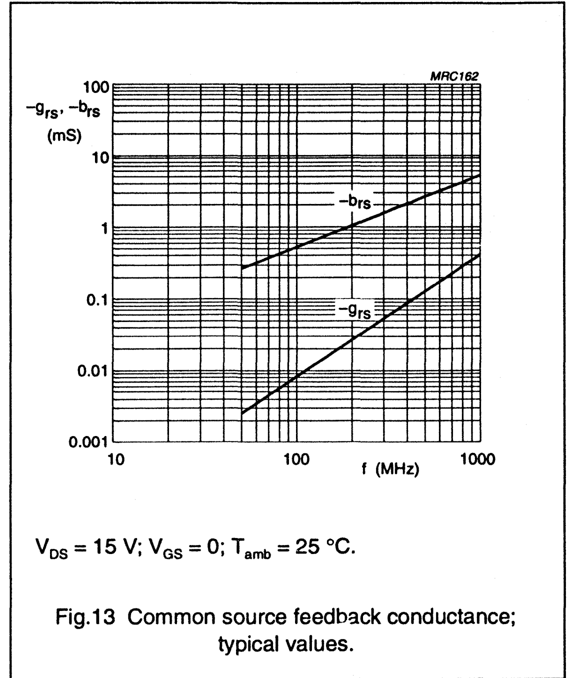
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



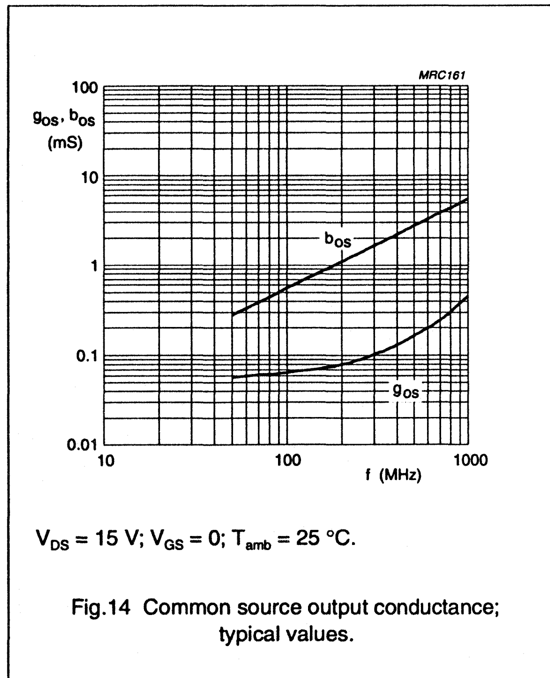
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for PN4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V²
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

Note

1. Parameter not extracted; default value.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	July 1993

PZFJ108/PZFJ109/PZFJ110
N-channel junction FETs

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for PZFJ108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT223 envelope. They are intended for use in applications such as analog switches, choppers and commutators, as well as in audio amplifiers.

PINNING - SOT223

PIN	DESCRIPTION
1	drain
2	gate
3	source
4	gate

Note

1. Drain and source are interchangeable.

PIN CONFIGURATION

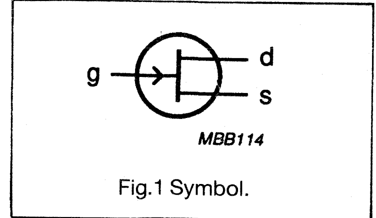


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C (note 1)	-	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Notes

1. Device mounted on an epoxy PCB, 40 mm x 40 mm x 1.5 mm. Mounting pad for the gate lead minimum 6 cm^2.

STATIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS} = 10$ V $V_{DS} = 5$ V		-	3	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V	PZFJ108 PZFJ109 PZFJ110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ μA $V_{DS} = 0$		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ μA $V_{DS} = 5$ V	PZFJ108 PZFJ109 PZFJ110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V	PZFJ108 PZFJ109 PZFJ110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Figs. 2 and 3)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (PZFJ108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (PZFJ109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (PZFJ110).

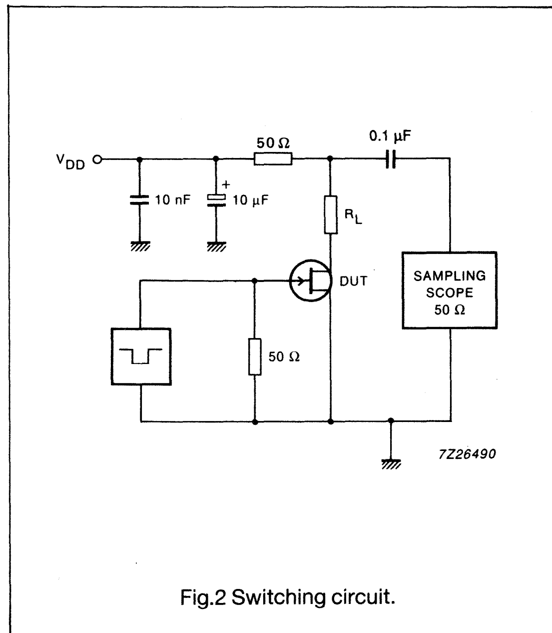


Fig.2 Switching circuit.

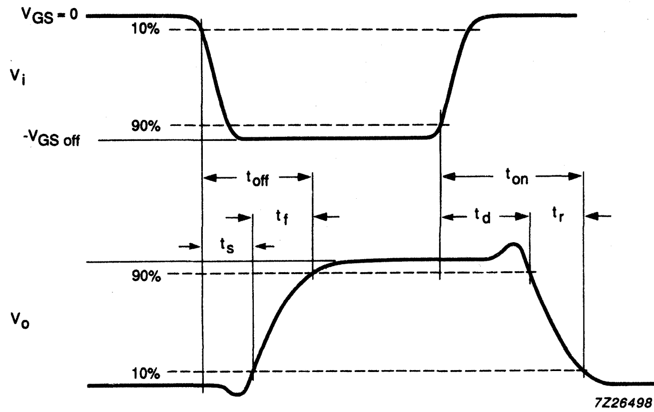


Fig.3 Input and output waveforms.

Data sheet	
status	Product specification
date of issue	July 1993

VN2406L

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and designed for use as a line current interrupter in telephone sets and for applications in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

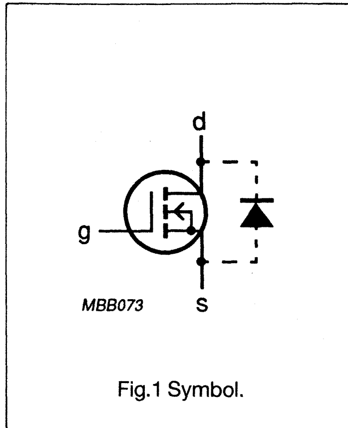


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	210	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

N-channel enhancement mode vertical D-MOS transistor

VN2406L

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	40	V
I_D	drain current	DC value	-	210	mA
I_{DM}	drain current	peak value	-	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

CHARACTERISTICS

$T_j = 25\ °C$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100\ \mu A$ $V_{GS} = 0$	240	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 120\ V$ $V_{GS} = 0$	-	-	10	μA
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 20\ V$	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	$I_D = 1\ mA$ $V_{DS} = V_{GS}$	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500\ mA$ $V_{GS} = 10\ V$	-	-	6	Ω
$R_{DS(on)}$	drain-source on-resistance	$I_D = 100\ mA$ $V_{GS} = 2.5\ V$	-	-	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$I_D = 300\ mA$ $V_{DS} = 25\ V$	200	400	-	mS
C_{iss}	input capacitance	$V_{DS} = 25\ V$ $V_{GS} = 0$ $f = 1\ MHz$	-	65	90	pF
C_{oss}	output capacitance	$V_{DS} = 25\ V$ $V_{GS} = 0$ $f = 1\ MHz$	-	20	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25\ V$ $V_{GS} = 0$ $f = 1\ MHz$	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250\ mA$ $V_{DD} = 50\ V$ $V_{GS} = 0\text{-}10\ V$	-	5	10	ns
t_{off}	turn-off time	$I_D = 250\ mA$ $V_{DD} = 50\ V$ $V_{GS} = 0\text{-}10\ V$	-	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

VN2406L

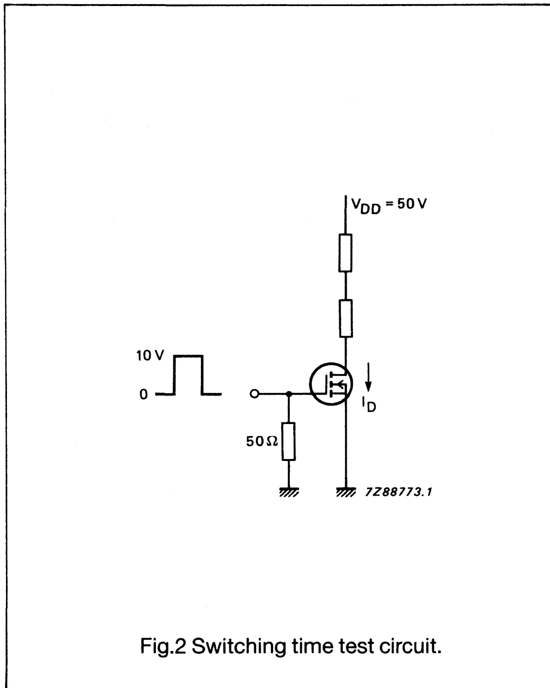


Fig.2 Switching time test circuit.

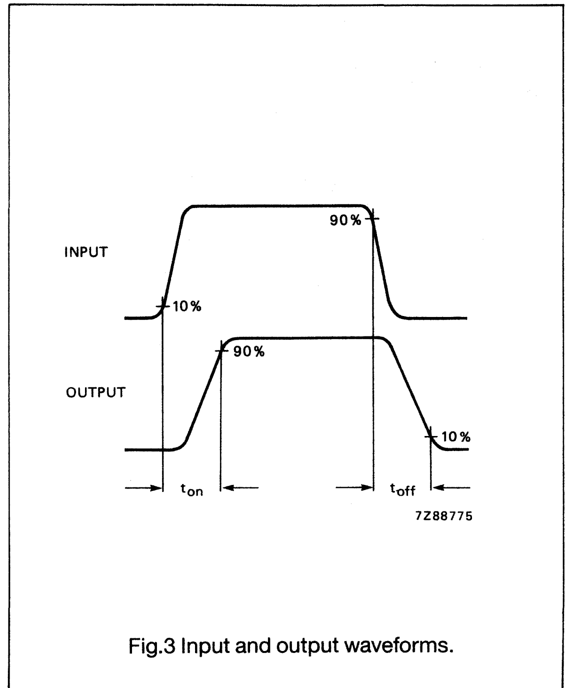


Fig.3 Input and output waveforms.

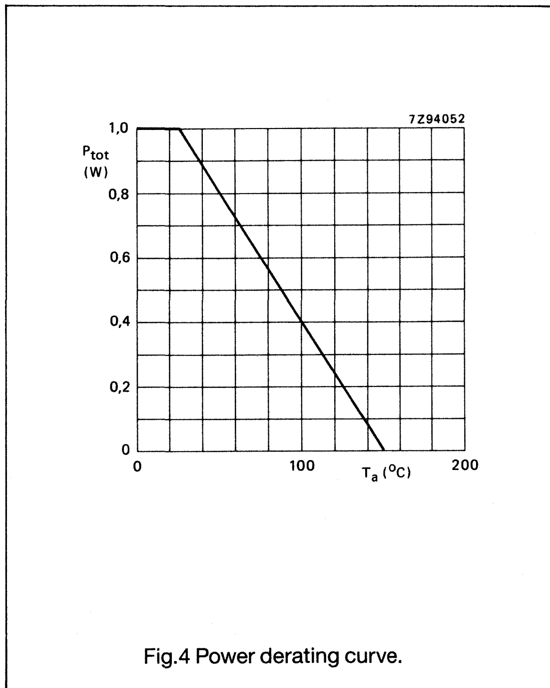


Fig.4 Power derating curve.

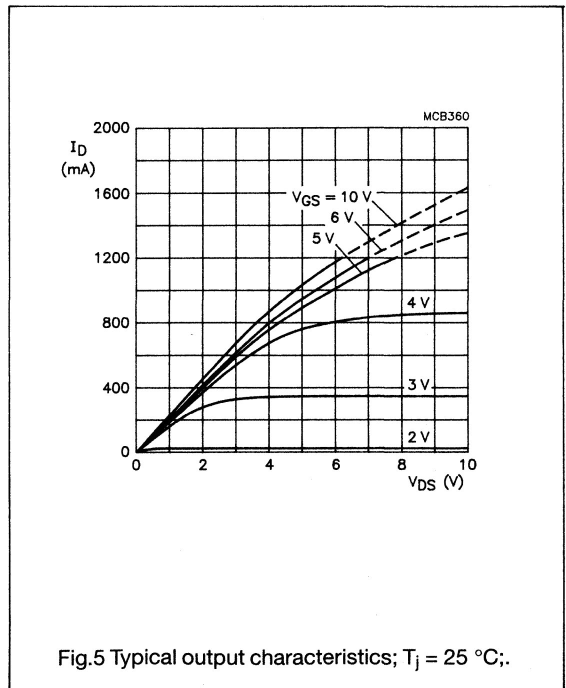


Fig.5 Typical output characteristics; T_j = 25 °C;.

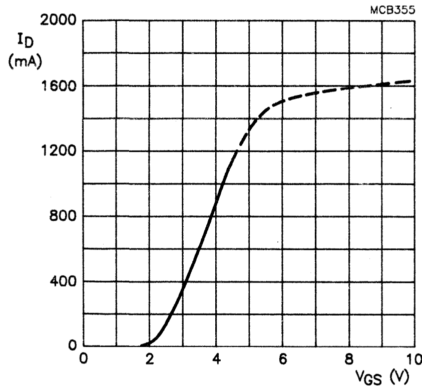


Fig.6 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25 °C;.

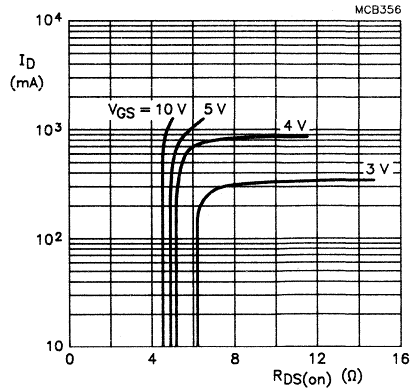


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C;.

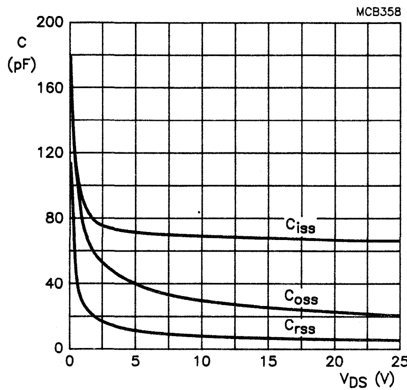


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C;.

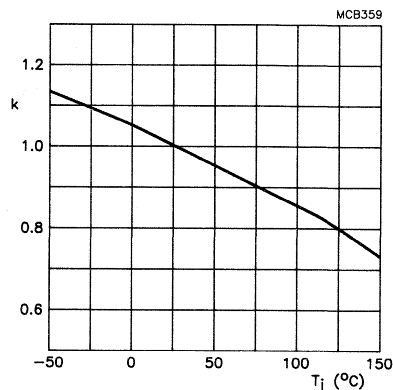


Fig.9 Temperature coefficient of gate-source threshold voltage;

$k = \frac{+V_{GS(th)} \text{ at } T_j}{+V_{GS(th)} \text{ at } 25\ °C}$; $V_{GS(th)}$ at 1 mA; typical values.

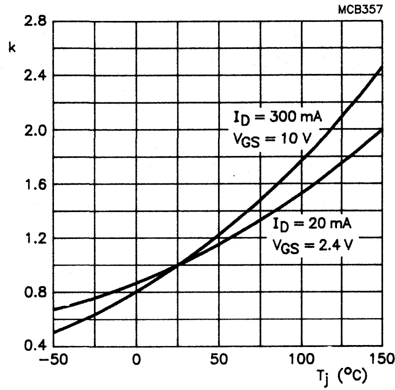


Fig.10 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical values.

Data sheet	
status	Product specification
date of issue	July 1993

VN2410L

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and designed for use as a line current interrupter in telephone sets and for applications in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

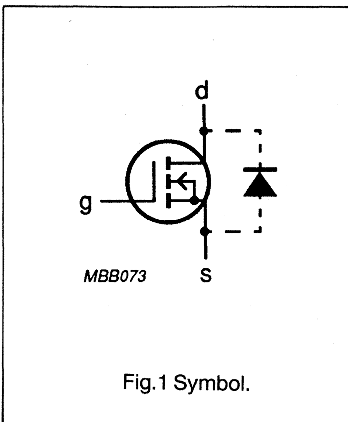


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	150	mA
$R_{DS(on)}$	drain-source on-resistance	10	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

N-channel enhancement mode vertical D-MOS transistor

VN2410L

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	40	V
I_D	drain current	DC value	-	150	mA
I_{DM}	drain current	peak value	-	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 100 μA V_{GS} = 0	240	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 120 V V_{GS} = 0	-	-	10	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 20 V	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA $V_{DS} = V_{GS}$	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	-	-	10	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA V_{GS} = 2.5 V	-	-	10	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA V_{DS} = 25 V	200	400	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	65	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0-10 V	-	5	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0-10 V	-	20	30	ns

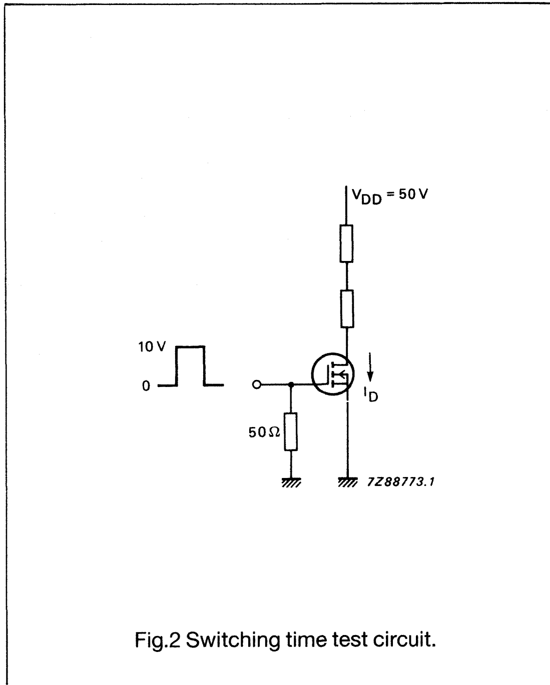


Fig.2 Switching time test circuit.

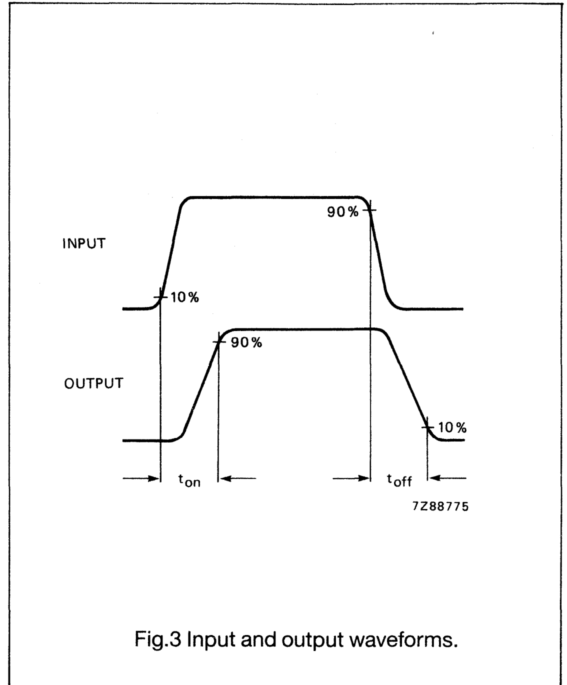


Fig.3 Input and output waveforms.

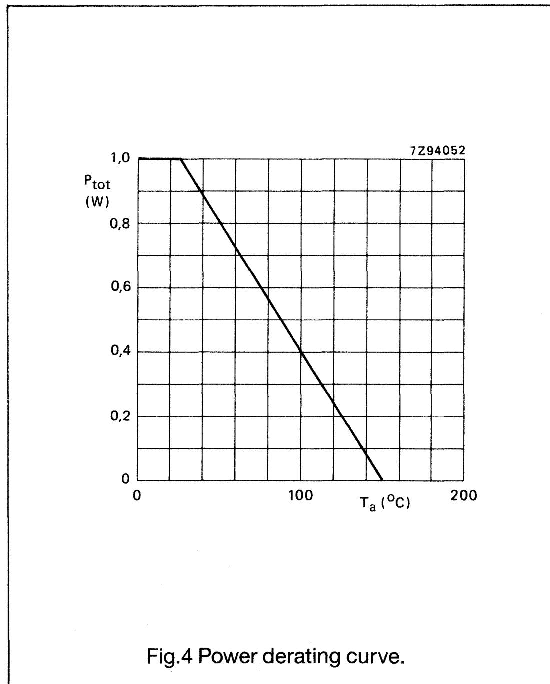


Fig.4 Power derating curve.

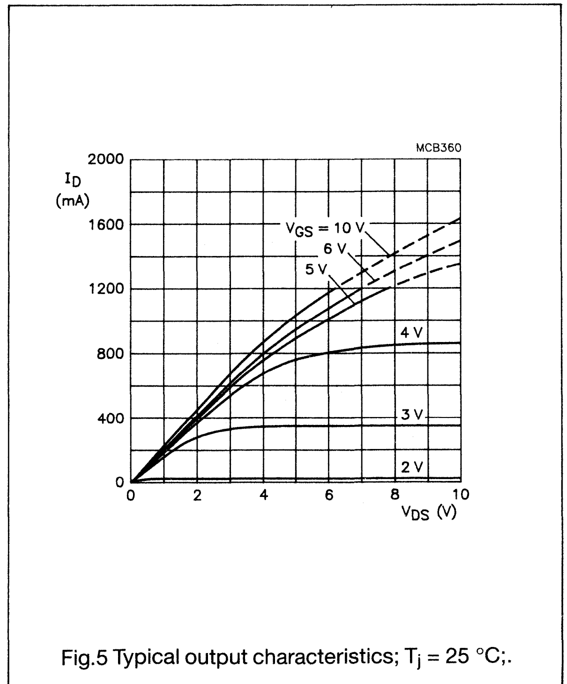


Fig.5 Typical output characteristics; T_j = 25 °C;.

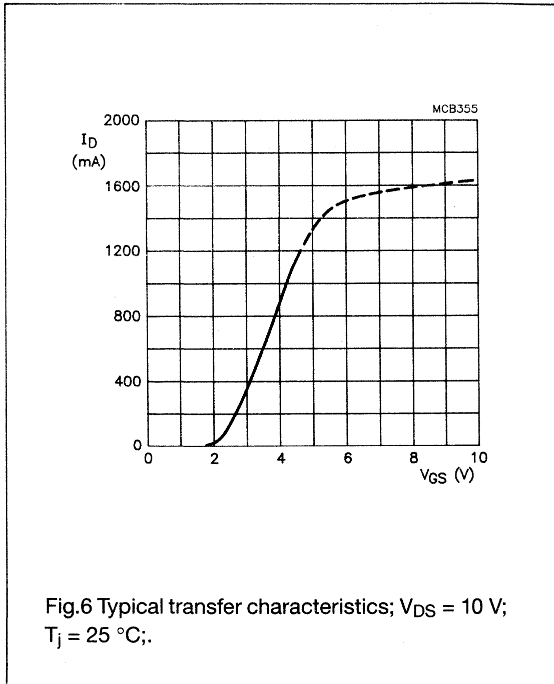


Fig.6 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25 °C;.

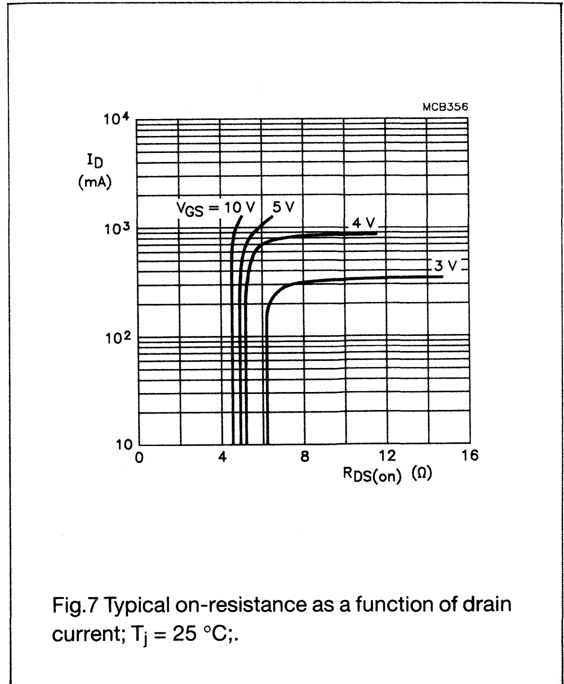


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C;.

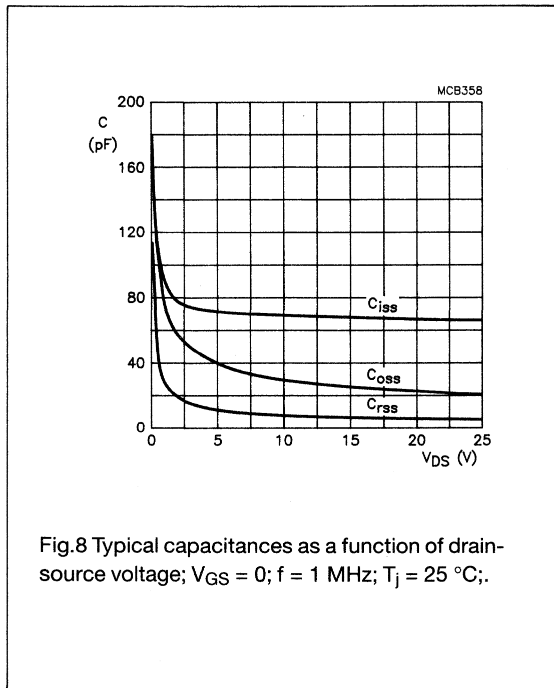


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C;.

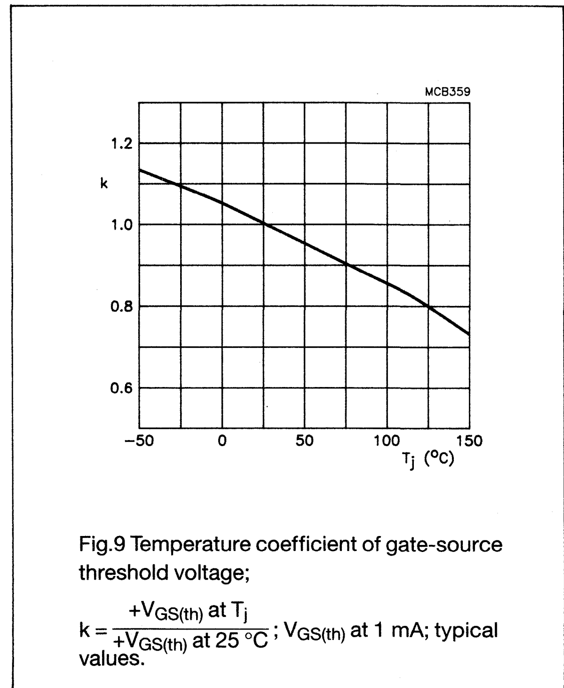


Fig.9 Temperature coefficient of gate-source threshold voltage;

$k = \frac{+V_{GS(th)} \text{ at } T_j}{+V_{GS(th)} \text{ at } 25\ °C}$; $V_{GS(th)}$ at 1 mA; typical values.

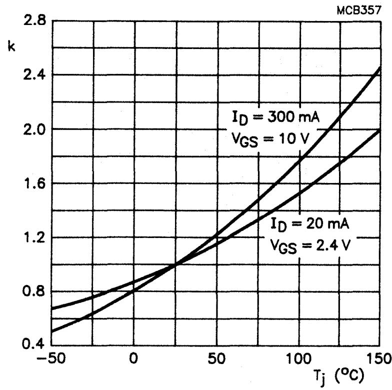


Fig.10 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical values.

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

			2N4091	2N4092	2N4093	
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max		1.5		W
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	5,0	2,0	1,0	V
		<	10	7,0	5,0	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	30	50	80	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 20 V	C_{rs}	<		5,0		pF
Turn-off time V_{DD} = 3,0 V; V_{GS} = 0						
I_D = 6,6 mA; $-V_{GSM}$ = 12 V **2N4091**	t_{off}	<		40		ns
I_D = 4,0 mA; $-V_{GSM}$ = 8 V **2N4092**	t_{off}	<		60		ns
I_D = 2,5 mA; $-V_{GSM}$ = 6 V **2N4093**	t_{off}	<		80		ns

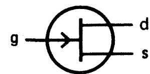
MECHANICAL DATA

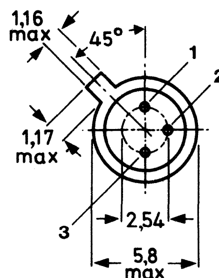
Dimensions in mm

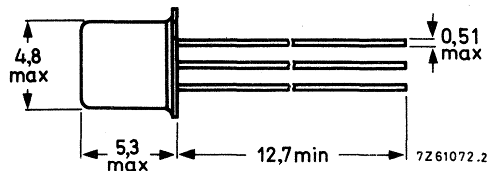
Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V

Current

Forward gate current (DC)	I_G	max.	10	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−55 to	+175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to case in free air	$R_{th\ j-c}$	=	100	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4091	2N4092	2N4093	
Drain currents						
V_{DG} = 20 V; I_S = 0	I_{DGO}	<		0.2		nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<		0.4		μA
Source current						
V_{SG} = 20 V; I_D = 0	I_{SGO}	<		0.2		nA
Drain cut-off current						
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX}	<	0.2	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 8 V	I_{DSX}	<	–	0.2	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 6 V	I_{DSX}	<	–	–	0.2	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX}	<	0.4	–	–	μA
V_{DS} = 20 V; $-V_{GS}$ = 8 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.4	–	μA
V_{DS} = 20 V; $-V_{GS}$ = 6 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.4	μA
Gate-source breakdown voltage						
$-I_G$ = 1.0 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Drain current [1]						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	5.0	2.0	1.0	V
		<	10	7.0	5.0	V
Drain-source voltages (on)						
I_D = 6.6 mA; V_{GS} = 0	V_{DSon}	<	0.2	–	–	V
I_D = 4.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.2	–	V
I_D = 2.5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.2	V
Drain-source resistance (on)						
I_D = 1.0 mA; V_{GS} = 0	R_{DSon}	<	30	50	80	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	30	50	80	Ω

[1]) Measured under pulsed conditions: $t_p \leq 300\ \mu s$; $\delta \leq 0.03$

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

y-parameters at f = 1 MHz (common source)

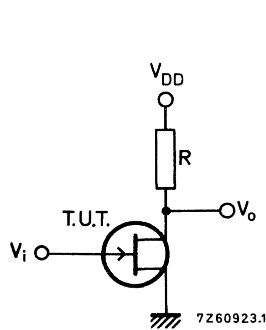
Input capacitance				
V_{DS} = 20 V ; V_{GS} = 0	C_{is}	<	16	pF
Feedback capacitance				
V_{DS} = 0 ; $-V_{GS}$ = 20 V	C_{rs}	<	5	pF

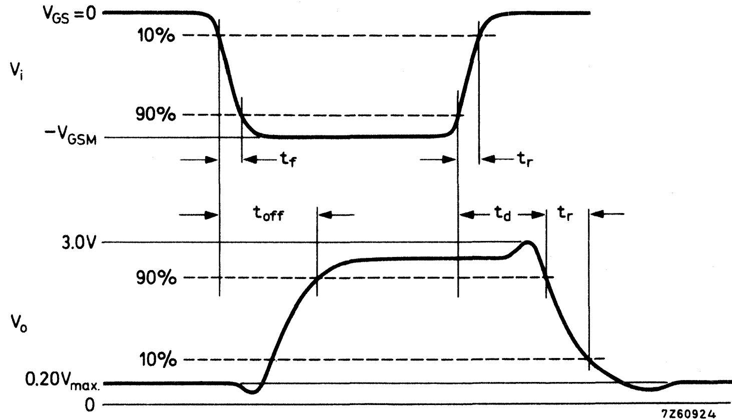
Switching times

V_{DD} = 3,0 V; V_{GS} = 0

			2N4091	2N4092	2N4093	
	I_D	=	6,6	4,0	2,5	mA
	$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	<	15	15	20	ns
Rise time	t_r	<	10	20	40	ns
Turn-off time	t_{off}	<	40	60	80	ns

Test circuit:





$R = \frac{2,8}{I_D}$

Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1,0	µs
δ	=	0,1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0,4	ns
R_i	>	9,8	MΩ
C_i	<	1,7	pF

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N4220/4220A/4221/4221A/ 4222/4222A

N-channel J-FETs

FEATURES

- High gain in VHF range
- Low receiver noise figure.

DESCRIPTION

Symmetrical n-channel silicon junction field-effect transistor in a TO-72 envelope. It is intended for use as a VHF amplifier and in oscillators and mixers.

PINNING - TO-72

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	substrate

PIN CONFIGURATION

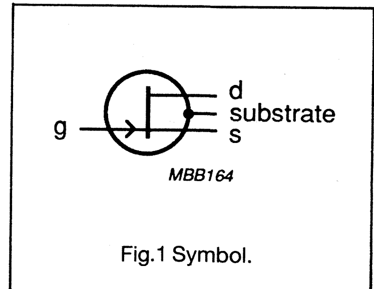


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	30	V
$-V_{GS}$	gate-source voltage		-	30	V
V_{DG}	drain-gate voltage		-	30	V
I_D	drain current		-	15	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	300	mW
T_{stg}	storage temperature range		−65	175	°C
T_j	junction temperature		-	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

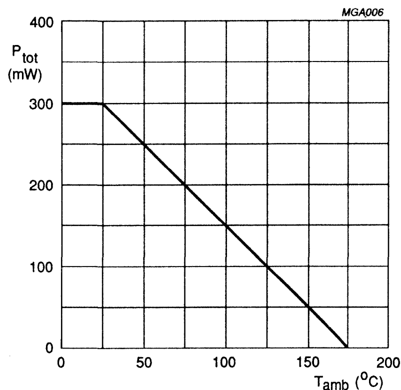


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 10 μA V_{DS} = 0		30	-	-	V
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 15 V V_{DS} = 0		-	-	0.1	nA
		$-V_{GS}$ = 15 V V_{DS} = 0 T_{amb} = 150 °C		-	-	100	nA
I_{DSS}	drain-source current	V_{DS} = 15 V V_{GS} = 0	2N4220/A 2N4221/A 2N4222/A	0.5 2 5	- - -	3 6 15	mA mA mA
$-V_{GS}$	gate-source voltage	V_{DS} = 15 V I_D = 50 μA	2N4220/A	0.5	-	2.5	V
		V_{DS} = 15 V I_D = 200 μA	2N4221/A	1	-	5	V
		V_{DS} = 15 V I_D = 500 μA	2N4222/A	2	-	6	V
$-V_{P(GS)}$	gate-source cut-off voltage	V_{DS} = 15 V I_D = 0.1 nA	2N4220/A 2N4221/A 2N4222/A	- - -	- - -	4 6 8	V V V
$\|g_{fs}\|$	transfer conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N4220/A 2N4221/A 2N4222/A	1 2 2.5	- - -	4 5 6	mS mS mS
$\|y_{fs}\|$	transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 100 MHz		750	-	-	μS
$\|y_{os}\|$	output admittance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N4220/A 2N4221/A 2N4222/A	- - -	- - -	10 20 40	μS μS μS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	4.5	6	pF
$-C_{rss}$	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	1.2	2	pF
C_{oss}	output capacitance	V_{DS} = 15 V V_{GS} = 0 f = 30 MHz		-	1.5	-	pF
$R_{DS(on)}$	drain-source on resistance	V_{DS} = 0 V_{GS} = 0	2N4220/A 2N4221/A 2N4222/A	- - -	500 400 300	- - -	Ω Ω Ω
F	noise figure	V_{DS} = 15 V V_{GS} = 0 R_S = 1 MΩ f = 100 Hz	2N4220A 2N4221A 2N4222A	-	-	2.5	dB

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N4340
N-channel J-FET

FEATURES

- Low noise, noise figure < 1 dB
- High off isolation.

DESCRIPTION

Symmetrical n-channel silicon junction field-effect transistor in a TO-18 metal envelope. It is intended for use in small-signal audio amplifiers, as a switch in choppers, and as a voltage-controlled resistor.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	drain
3	gate, substrate

PIN CONFIGURATION

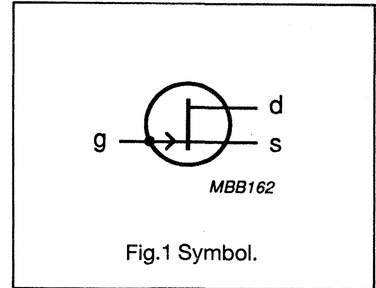


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{GD}$	gate-drain voltage		-	50	V
$-V_{GS}$	gate-source voltage		-	50	V
I_G	gate current		-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	300	mW
T_{stg}	storage temperature range		−65	200	°C
T_j	junction temperature		-	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

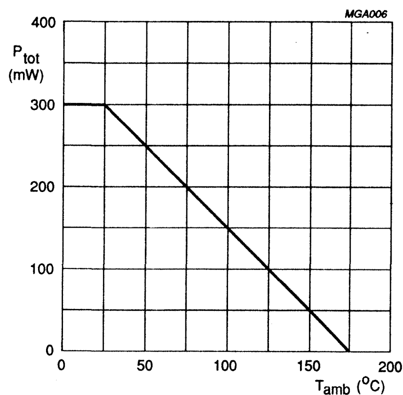


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 $-I_G$ = 1 μA	50	-	-	V
I_{DSS}	drain-source current	V_{GS} = 0 V_{DS} = 15 V	1.2	-	3.6	mA
I_{DSX}	drain-source cut-off current	$-V_{GS}$ = 5 V V_{DS} = 15 V	-	-	0.05	nA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 30 V	-	-	0.1	nA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 30 V T_{amb} = 150 °C	-	-	0.1	μA
$-V_{P(GS)}$	gate-source cut-off voltage	I_D = 0.1 μA V_{DS} = 15 V	1	-	3	V
$r_{ds(on)}$	drain-source on resistance	V_{DS} = 0 V_{GS} = 0 f = 1 kHz	-	-	1.5	kΩ
g_{fs}	transfer conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	1.3	-	3	mS
g_{os}	output conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	-	-	30	μS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	-	7	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	-	3	pF
F	noise figure	V_{GS} = 0 V_{DS} = 15 V R_G = 1 MΩ f = 1 kHz B = 200 Hz	-	-	1	dB

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to $T_{case} = 25\ ^oC$	P_{tot}	max.		1.5		W
			2N4391	**2N4392**	**2N4393**	
Drain current $V_{DS} = 20\ V;\ V_{GS} = 0$	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage $I_D = 1\ nA;\ V_{DS} = 20\ V$	$-V_{(P)GS}$	>	4,0	2,0	0,5	V
		<	10	5,0	3,0	V
Drain-source resistance (on) at f = 1 kHz $I_D = 1\ mA;\ V_{GS} = 0$	R_{DSon}	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz $V_{DS} = 0;\ -V_{GS} = 12\ V$ **2N4391**; $V_{DS} = 0;\ -V_{GS} = 7\ V$ **2N4392**; $V_{DS} = 0;\ -V_{GS} = 5\ V$ **2N4393**	C_{rs}	<	3,5	3,5	3,5	pF
Turn-off time $V_{DD} = 10\ V;\ V_{GS} = 0$						
$I_D = 12\ mA;\ -V_{GSoff} = 12\ V$	t_{off}	<	20	–	–	ns
$I_D = 6,0\ mA;\ -V_{GSoff} = 7\ V$	t_{off}	<	–	35	–	ns
$I_D = 3,0\ mA;\ -V_{GSoff} = 5\ V$	t_{off}	<	–	–	50	ns

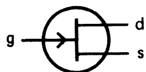
MECHANICAL DATA

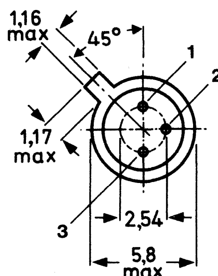
Dimensions in mm

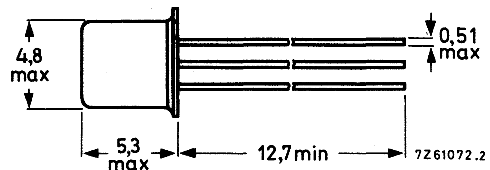
Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65	to +175	°C
Junction temperature	T_j	max.	175	°C
From junction to case in free air	$R_{th\ j\text{-}c}$	=	100	K/W

CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Gate cut-off current

$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$ <	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$ <	0.2	μA

Drain cut-off current

		2N4391	2N4392	2N4393	
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX} <	0.1	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 7 V	I_{DSX} <	–	0.1	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 5 V	I_{DSX} <	–	–	0.1	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX} <	0.2	–	–	μA
V_{DS} = 20 V; $-V_{GS}$ = 7 V; T_{amb} = 150 °C	I_{DSX} <	–	0.2	–	μA
V_{DS} = 20 V; $-V_{GS}$ = 5 V; T_{amb} = 150 °C	I_{DSX} <	–	–	0.2	μA

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

			2N4391	2N4392	2N4393	
Drain currents (note 1)						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	–	–	mA
		<	150	–	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	25	–	mA
		<	–	75	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	–	5	mA
		<	–	–	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source voltage						
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1.0	1.0	1.0	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4.0	2.0	0.5	V
		<	10	5.0	3.0	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.4	–	V
I_D = 3.0 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 1 mA; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
y parameters at f = 1 MHz (common source)						
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	–	–	pF
$-V_{GS}$ = 7 V; V_{DS} = 0	C_{rs}	<	–	3.5	–	pF
$-V_{GS}$ = 5 V; V_{DS} = 0	C_{rs}	<	–	–	3.5	pF

Note

1. measured under pulsed conditions: t_p = 100 μs; δ = 0.01

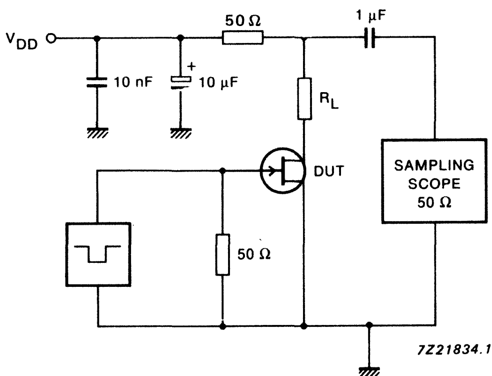
CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

Switching times

V_{DD} = 10 V; V_{GS} = 0

			2N4391	2N4392	2N4393	
	I_D	=	12	6.0	3.0	mA
	$-V_{GSoff}$	=	12	7	5	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

Test circuit:

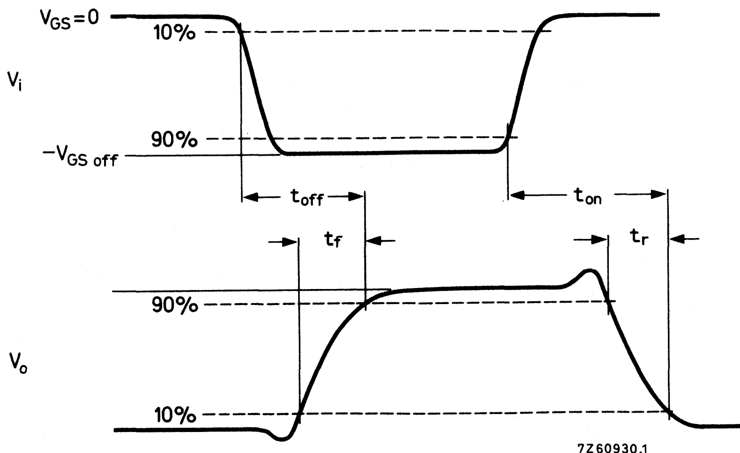


Pulse generator:

t_r	<	0.5	ns
t_f	<	0.5	ns
t_p	=	100	μs
δ	=	0.01	

Oscilloscope:

R_i = 50 Ω



N-channel field-effect transistor 2N4416; 2N4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a TO-72 envelope, with shield connected to the case. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - TO-72.

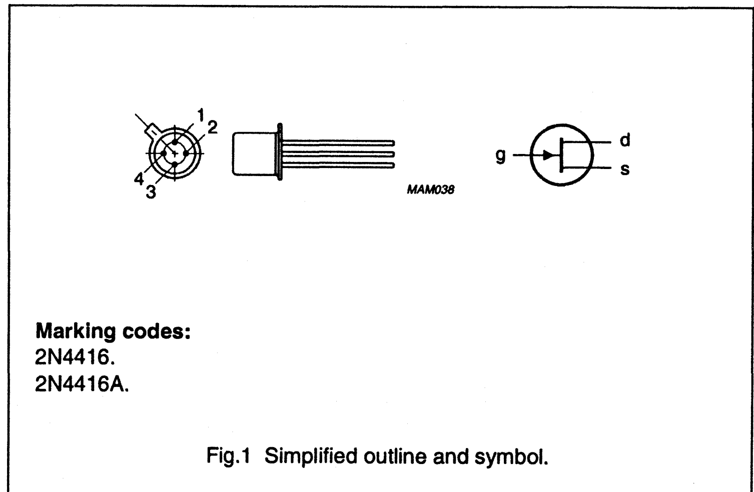
PIN	DESCRIPTION
1	source
2	drain
3	gate
4	shield

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	2N4416		–	30	V
	2N4416A		–	35	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N4416		–	−6	V
	2N4416A		−2.5	−6	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS



Marking codes:
2N4416.
2N4416A.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	2N4416		–	30	V
	2N4416A		–	35	V
V_{GSO}	gate-source voltage				
	2N4416		–	–30	V
	2N4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	2N4416		–	–30	V
	2N4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+175	°C
T_j	junction temperature		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	590 K/W

Note

1. Mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead 10 mm^2.

STATIC CHARACTERISTICS

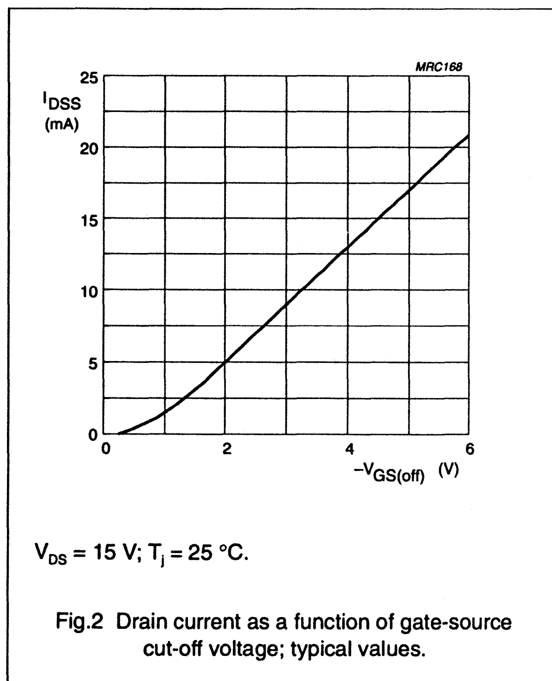
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA			
	2N4416		–30	–	V
	2N4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–0.1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N4416		–	–6	V
	2N4416A		–2.5	–6	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\lvert Y_{os} \rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N4416		–	50	μS
	2N4416A		–	50	μS

DYNAMIC CHARACTERISTICS

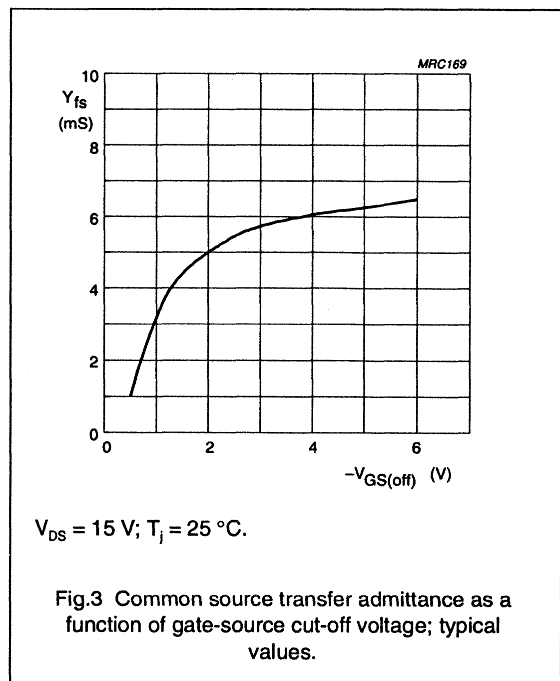
$T_j = 25$ °C; $V_{DS} = 15$ V; $V_{GS} = 0$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	µS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	–8	–	µS
		f = 400 MHz	–	–100	–	µS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	µS
		f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√HZ



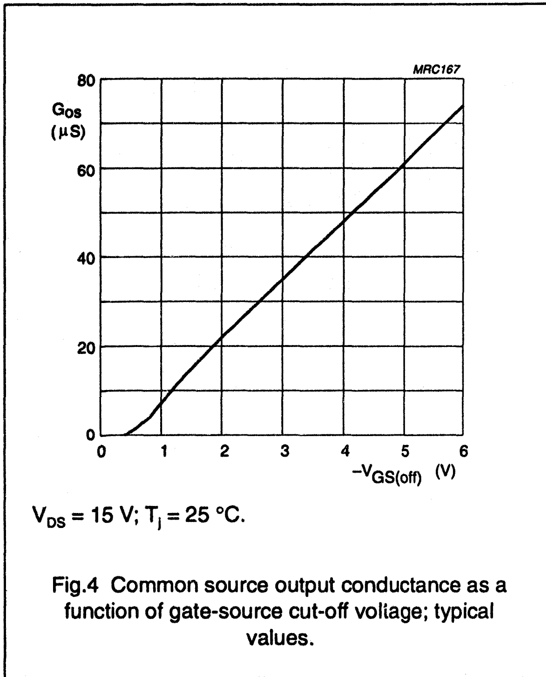
$V_{DS} = 15$ V; $T_j = 25$ °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



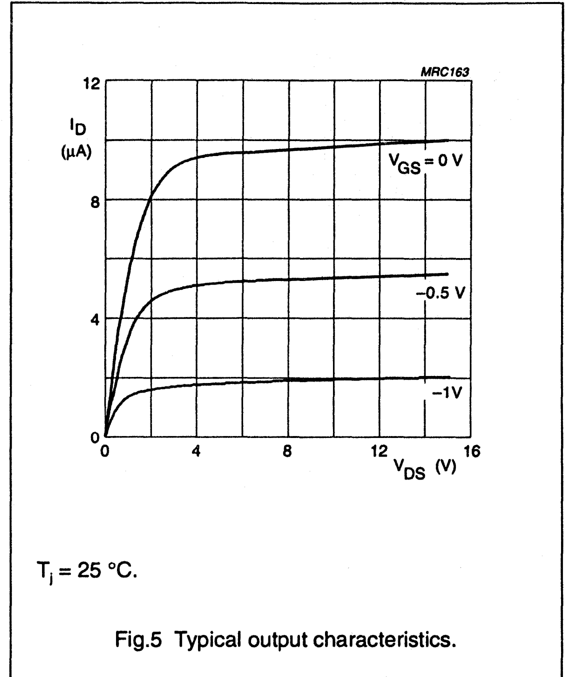
$V_{DS} = 15$ V; $T_j = 25$ °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



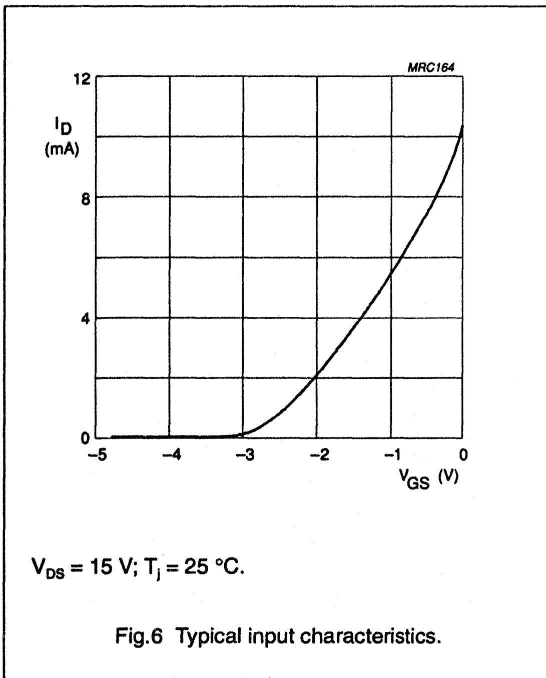
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



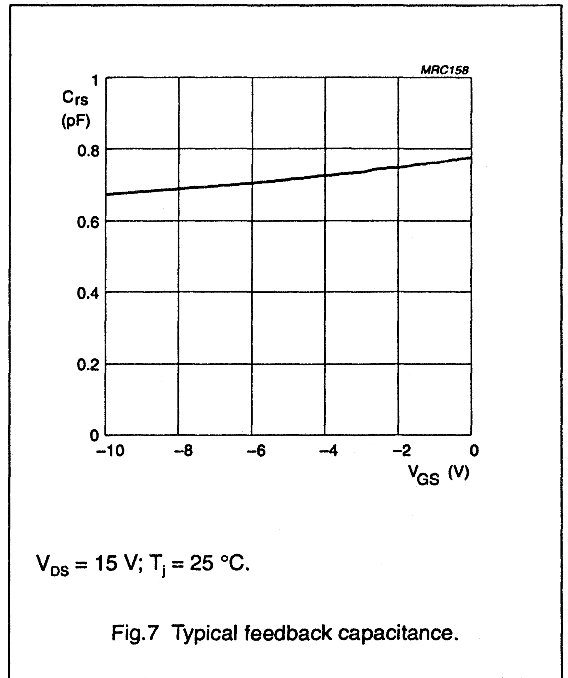
T_j = 25 °C.

Fig.5 Typical output characteristics.



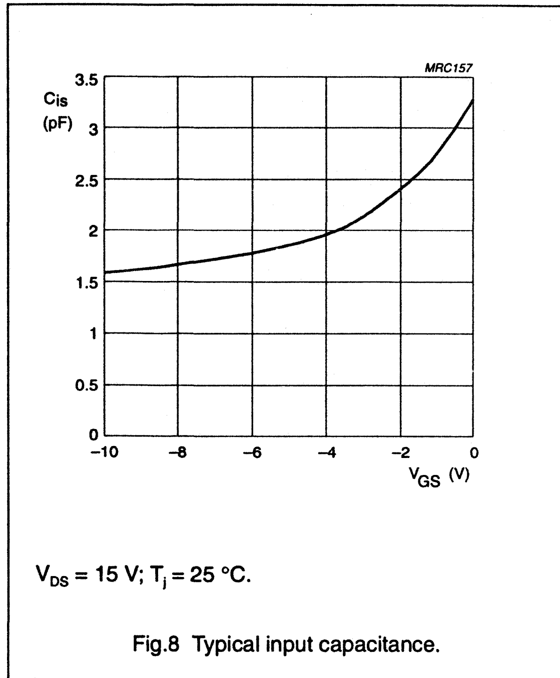
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

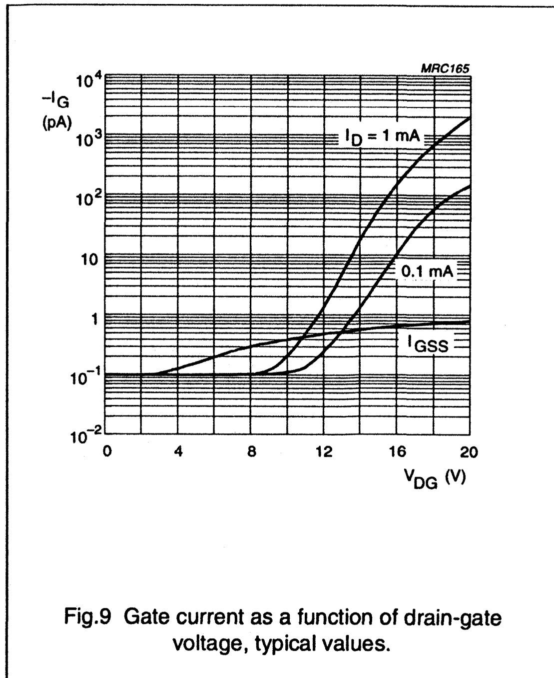


Fig.9 Gate current as a function of drain-gate voltage, typical values.

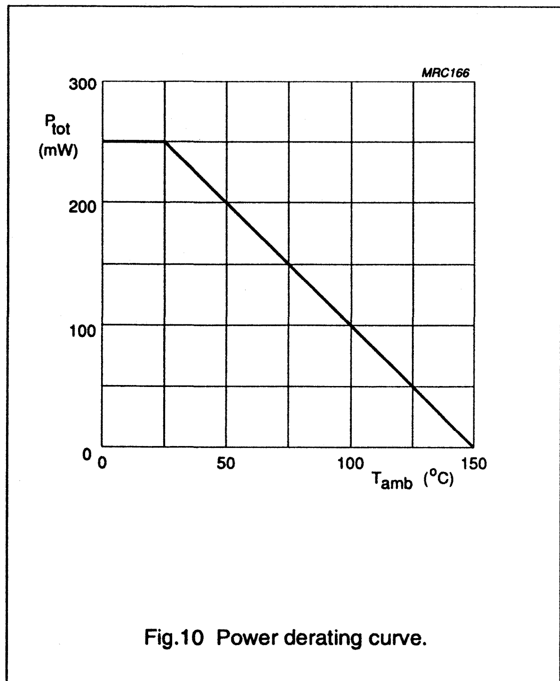
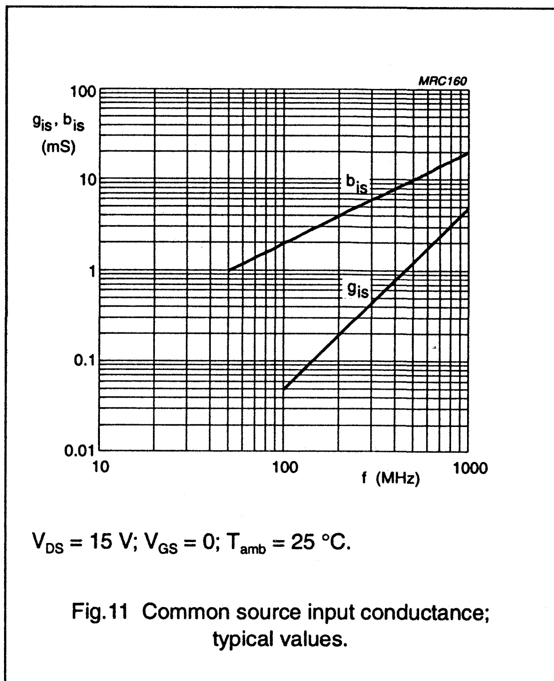
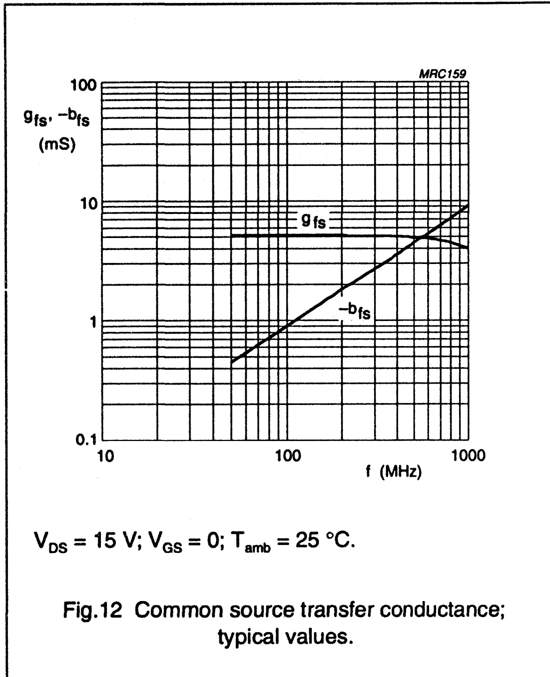


Fig.10 Power derating curve.



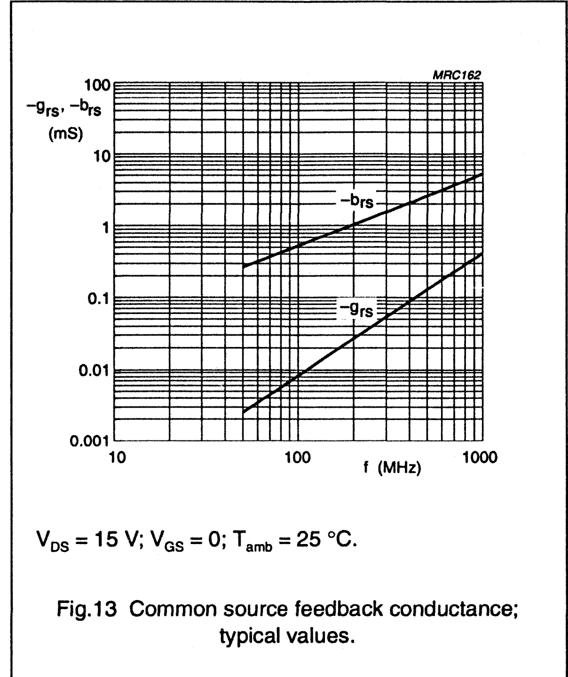
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



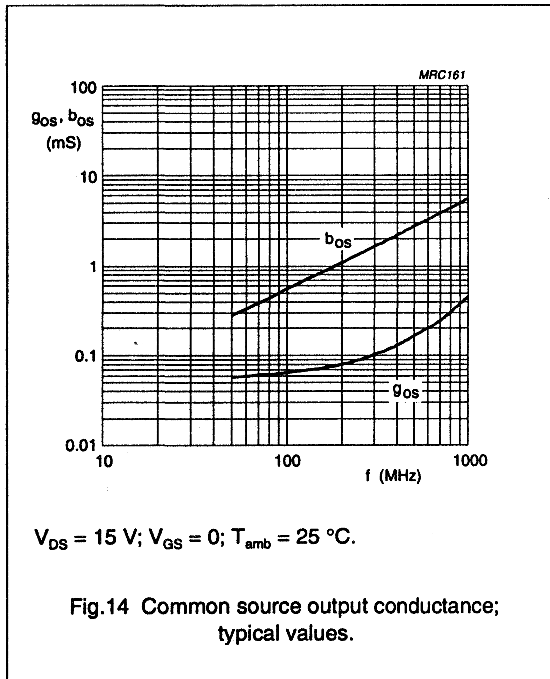
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for 2N4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V²
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

Note

1. Parameter not extracted; default value.

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

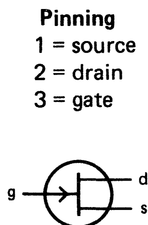
Drain-source voltage	2N4856 to 2N4858	$\pm V_{DS}$	max.		40		V
	2N4859 to 2N4861	$\pm V_{DS}$	max.		30		V
Total power dissipation up to T_{amb} = 25 °C		P_{tot}	max.		360		mW
				2N4856 **2N4859**	**2N4857** **2N4860**	**2N4858** **2N4861**	
Drain current V_{DS} = 15 V; V_{GS} = 0		I_{DSS}	>	50	20	8	mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V		$-V_{(P)GS}$	>	4	2	0,8	V
			<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0		$R_{DS\,on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V		C_{rs}	<		8		pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0							
I_D = 20 mA; $-V_{GSM}$ = 10 V	**2N4856; 2N4859**	t_{off}	<		25		ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	**2N4857; 2N4860**	t_{off}	<		50		ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	**2N4858; 2N4861**	t_{off}	<		100		ns

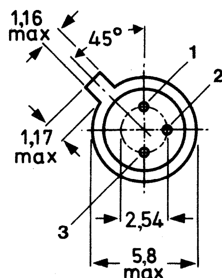
MECHANICAL DATA

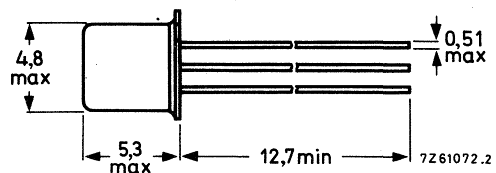
Dimensions in mm

Fig. 1 TO-18

Gate connected to case







Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Drain-source voltage	$\pm V_{DS}$	max.	40	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	30	V
Gate current (d.c.)	I_G	max.	50		mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300		mW
Storage temperature range	T_{stg}		−65 to +175		^oC
Junction temperature	T_j	max.	175		^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	490	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.25	–	nA
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	–	0.25	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0.5	–	µA
$-V_{GS}$ = 15 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	–	0.5	µA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	<	0.25	0.25	nA
V_{DS} = 15 V; $-V_{GS}$ = 10 V; T_{amb} = 150 °C	I_{DSX}	<	0.5	0.5	µA

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current [1]						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate-source breakdown voltage					
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$		40	30	V

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Gate-source cut-off voltage						
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	0.75	–	–	V
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	0.50	–	V
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.50	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	25	40	60	Ω

[1]) measured under pulsed conditions: t_p = 100 ms; $\delta \leq 0.1$

y-parameters (common source)

$V_{DS} = 0$; $-V_{GS} = 10$ V; f = 1 MHz

Input capacitance	C_{is}	<	18	pF
Feedback capacitance	C_{rs}	<	8	pF

Switching times (see Figs 2 and 3)

$V_{DD} = 10$ V; $V_{GS} = 0$

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current	I_D	=	20	10	5	mA
Gate-source voltage (peak value)	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

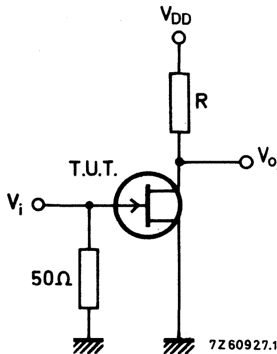


Fig. 2 Switching times test circuit.

	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861
R =	464	953	1910 Ω

Pulse generator:

$t_r \leqslant$ 1 ns

$t_f \leqslant$ 1 ns

δ = 0,02

Z_o = 50 Ω

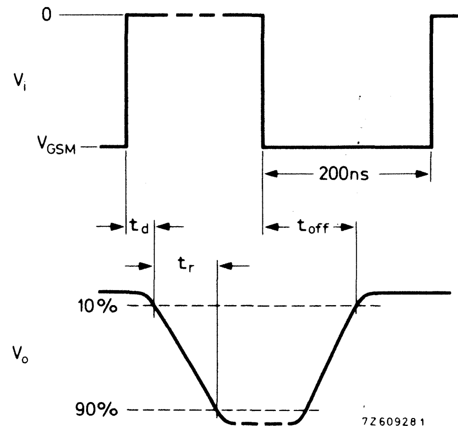


Fig. 3 Input and output waveforms.

Oscilloscope:

$t_r \leqslant$ 0,75 ns

$R_i \geqslant$ 1 MΩ

$C_i \leqslant$ 2,5 pF

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	July 1993

2N5116
P-channel J-FET

FEATURES

- P-channel complement of 2N4393
- Short sample and hold aperture time.

DESCRIPTION

P-channel silicon junction field-effect transistor in a TO-18 metal envelope. It is intended for applications as an analog switch, on commutators and choppers, and as an integrator reset switch.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	gate
3	drain

PIN CONFIGURATION

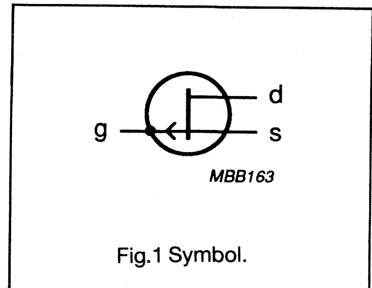


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{GD}	gate-drain voltage		-	30	V
V_{GS}	gate-source voltage		-	30	V
$-I_G$	gate current		-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	500	mW
T_{stg}	storage temperature range		−65	200	°C
T_j	junction temperature		-	200	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

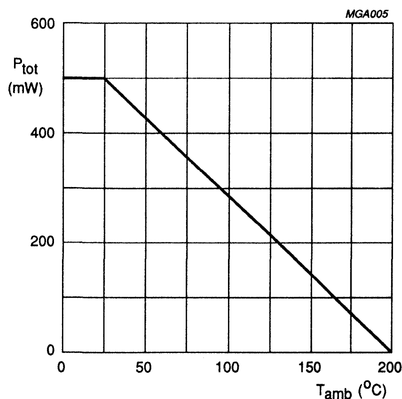


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 I_G = 1 μA	30	-	V
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0	-	0.5	nA
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0 T_{amb} = 150 °C	-	1	μA
$-I_{DSX}$	drain cut-off current	V_{GS} = 5 V $-V_{DS}$ = 15 V	-	0.5	nA
$-I_{DSX}$	drain cut-off current	V_{GS} = 5 V $-V_{DS}$ = 15 V T_{amb} = 150 °C	-	1	μA
$-I_{DSS}$	drain current	V_{GS} = 0 $-V_{DS}$ = 15 V	5	25	mA
$-V_{GS}$	gate-source voltage	$-I_G$ = 1 mA V_{DS} = 0	-	1	V
$V_{P(GS)}$	gate-source cut-off voltage	$-V_{DS}$ = 15 V $-I_D$ = 1 nA	1	4	V
$-V_{(DS)on}$	drain-source on voltage	V_{GS} = 0 $-I_D$ = 3 mA	-	0.6	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 0 $-I_D$ = 1 mA	-	150	Ω
$r_{ds(on)}$	drain-source on resistance	V_{GS} = 0 I_D = 0 f = 1 kHz	-	150	Ω
C_{iss}	input capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz	-	27	pF
C_{rss}	feedback capacitance	V_{DS} = 0 V_{GS} = 5 V f = 1 MHz	-	7	pF
Switching times					
t_d	delay time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	25	ns
t_r	rise time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	35	ns
$t_{d(off)}$	delay time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	20	ns
t_f	fall time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	60	ns

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N5460/5461/5462
P-channel J-FETs

DESCRIPTION

P-channel silicon junction field-effect transistor in a TO-92 plastic envelope. It is intended for use as an analog switch and an amplifier.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	drain
3	source

PIN CONFIGURATION

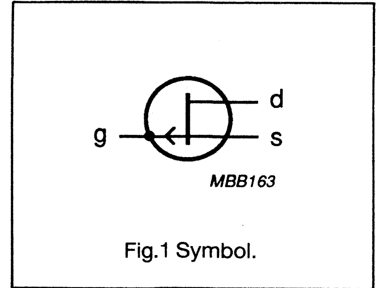


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	40	V
V_{GS}	gate-source voltage		-	40	V
$-I_G$	gate current		-	10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 40$ °C	-	310	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	355	K/W

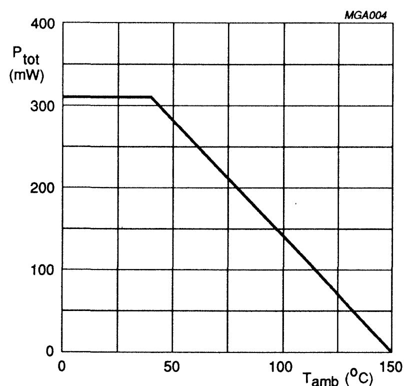


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0		-	5	nA
		V_{GS} = 20 V V_{DS} = 0 T_{amb} = 100 °C		-	1	μA
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 15 V V_{GS} = 0	2N5460 2N5461 2N5462	1 2 4	5 9 16	mA mA mA
V_{GS}	gate-source voltage	$-I_D$ = 0.1 mA $-V_{DS}$ = 15 V	2N5460	0.5	4	V
V_{GS}	gate-source voltage	$-I_D$ = 0.2 mA $-V_{DS}$ = 15 V	2N5461	0.8	4.5	V
V_{GS}	gate-source voltage	$-I_D$ = 0.4 mA $-V_{DS}$ = 15 V	2N5462	1.5	6	V
$V_{P(GS)}$	gate-source cut-off voltage	$-I_D$ = 1 μA $-V_{DS}$ = 15 V	2N5460 2N5461 2N5462	0.75 1 1.8	6 7.5 9	V V V
$\|y_{fs}\|$	transfer admittance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 kHz	2N5460 2N5461 2N5462	1 1.5 2	4 5 6	mS mS mS
$\|y_{os}\|$	output admittance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 kHz		-	75	μS
C_{iss}	input capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz		-	7	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz		-	2	pF
NF	noise figure	$-V_{DS}$ = 15 V V_{GS} = 0 f = 100 Hz B = 1 Hz		-	2.5	dB

N-channel field-effect transistors — 2N5484; 2N5485; 2N5486

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel, symmetrical, silicon junction FETs in a SOT54 (TO-92) envelope, intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT54 (TO-92)

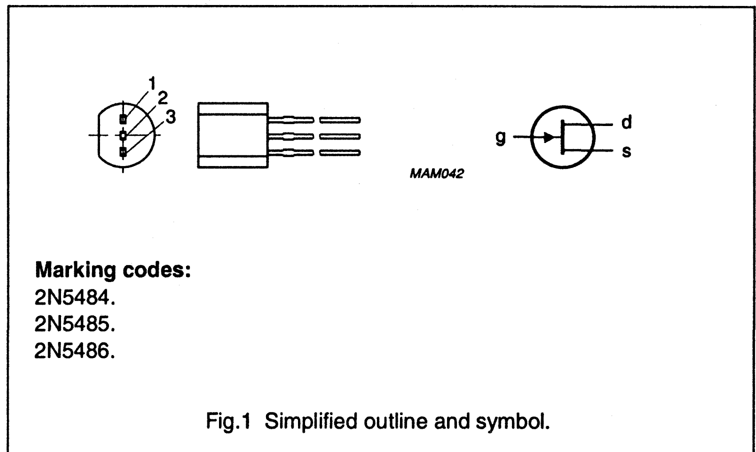
PIN	DESCRIPTION
1	gate
2	source
3	drain

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		1	5	mA
	2N5485		4	10	mA
	2N5486		8	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	400	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N5484		–0.3	–3	V
	2N5485		–0.5	–4	V
	2N5486		–2	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz			
	2N5484		3	6	mS
	2N5485		3.5	7	mS
	2N5486		4	8	mS



Marking codes:
2N5484.
2N5485.
2N5486.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	gate-drain voltage		–	–25	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	350 K/W

Note

1. Device mounted on a printed circuit board; maximum lead length 3 mm; mounting pad for drain lead minimum 10 mm x 10 mm.

STATIC CHARACTERISTICS

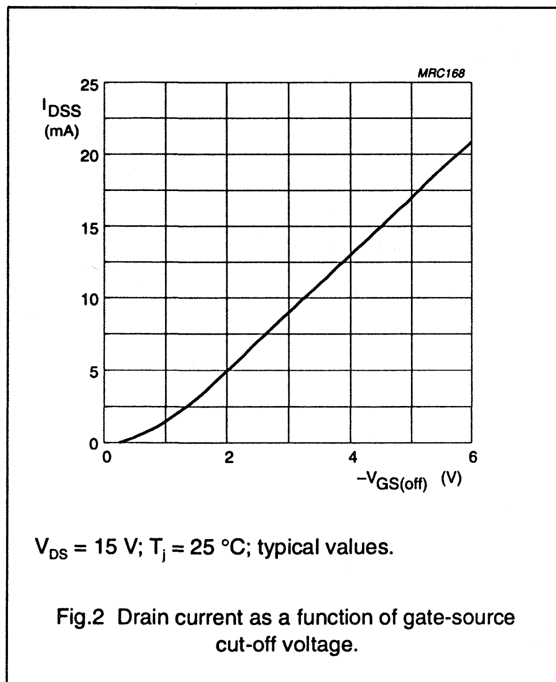
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 µA	–25	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		1	5	mA
	2N5485		4	10	mA
	2N5486		8	20	mA
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N5484		–0.3	–3	V
	2N5485		–0.5	–4	V
	2N5486		–2	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		3	6	mS
	2N5485		3.5	7	mS
	2N5486		4	8	mS
$\|Y_{os}\|$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		–	50	µS
	2N5485		–	60	µS
	2N5486		–	75	µS

DYNAMIC CHARACTERISTICS

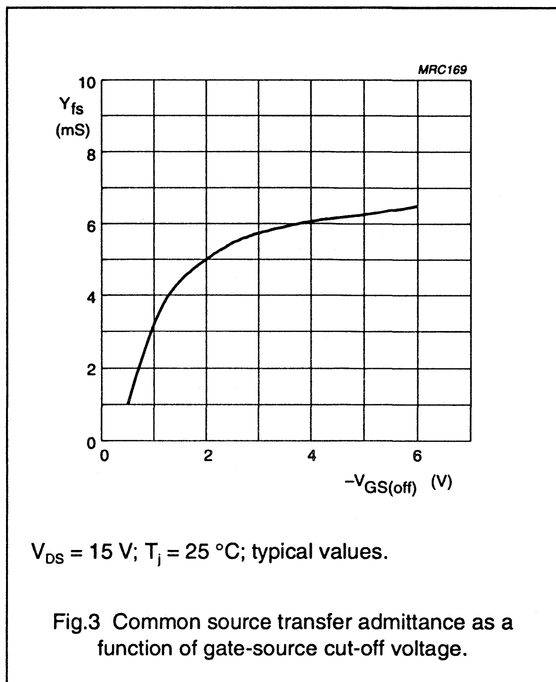
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	5	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	1	pF
g_{is}	common source input conductance					
	2N5484	f = 100 MHz	100	–	–	µS
	2N5485; 2N5486	f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance					
	2N5484	f = 100 MHz	2.5	–	–	mS
	2N5485	f = 400 MHz	3	–	1	mS
	2N5486	f = 400 MHz	3.5	–	1	mS
g_{os}	common source output conductance					
	2N5484	f = 100 MHz	–	–	75	µS
	2N5485; 2N5486	f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



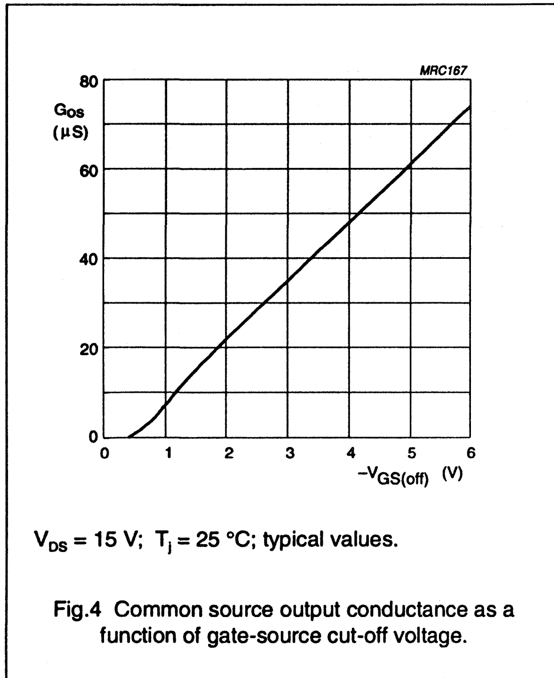
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.2 Drain current as a function of gate-source cut-off voltage.



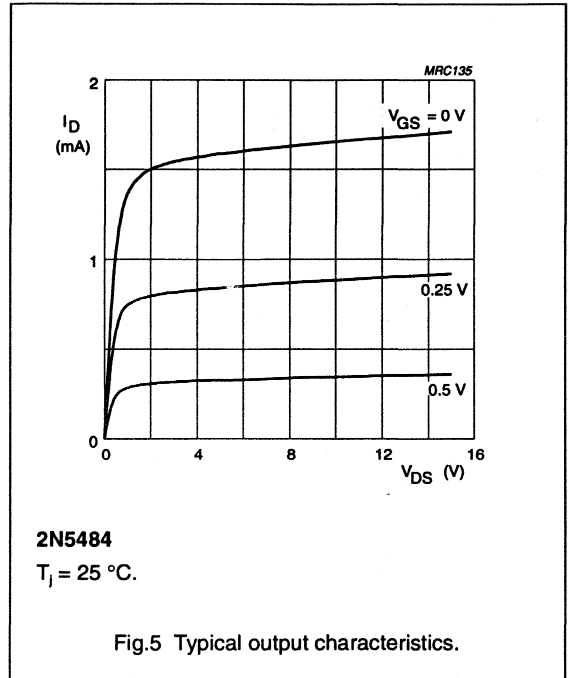
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



V_{DS} = 15 V; T_j = 25 °C; typical values.

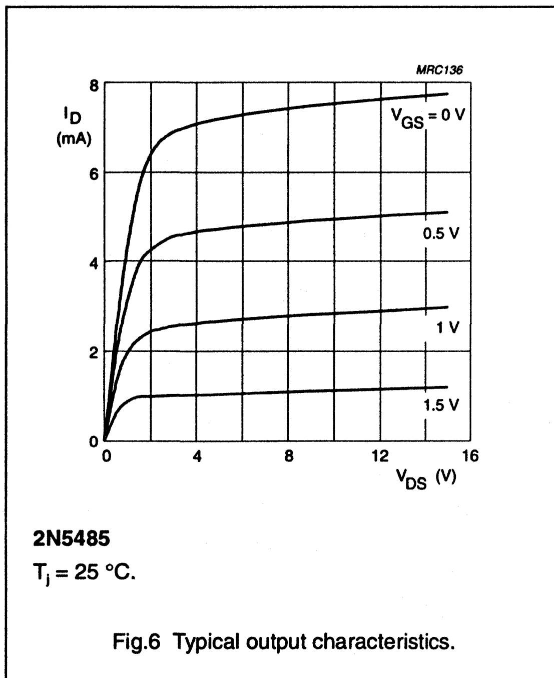
Fig.4 Common source output conductance as a function of gate-source cut-off voltage.



2N5484

T_j = 25 °C.

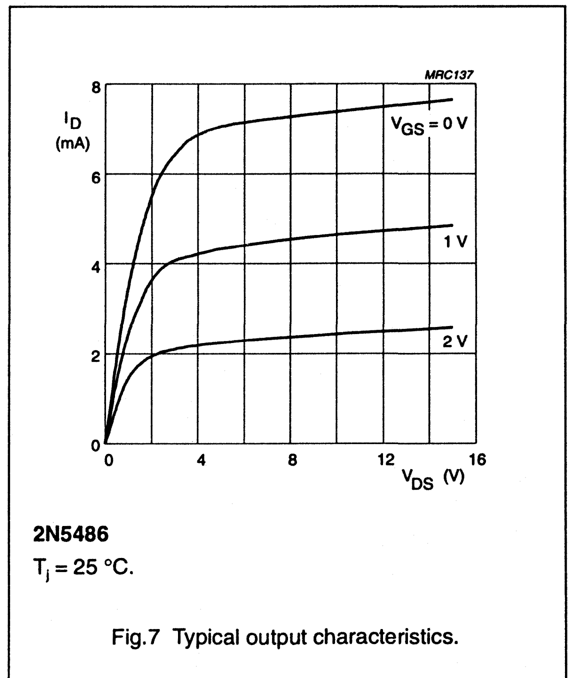
Fig.5 Typical output characteristics.



2N5485

T_j = 25 °C.

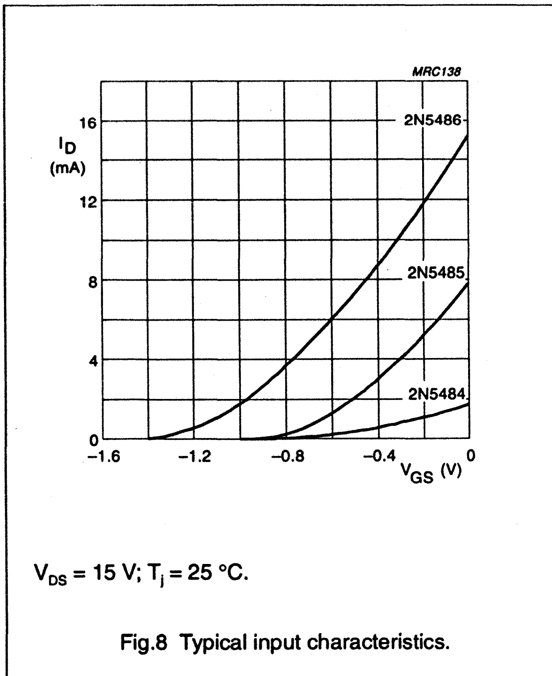
Fig.6 Typical output characteristics.



2N5486

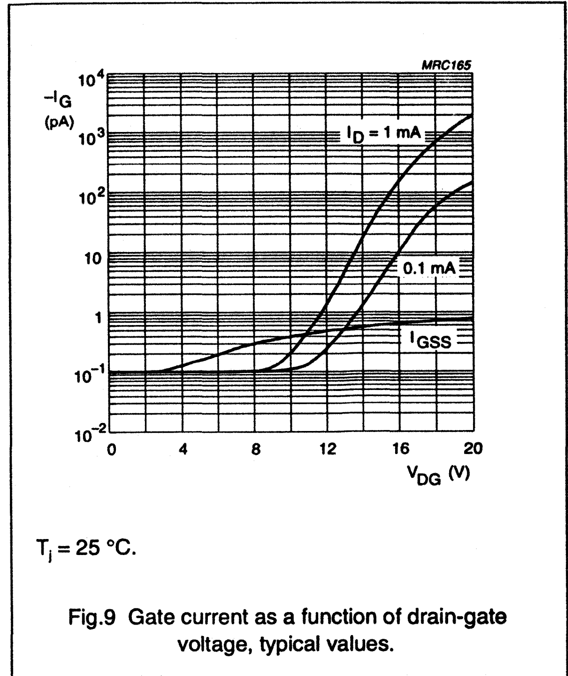
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input characteristics.



T_j = 25 °C.

Fig.9 Gate current as a function of drain-gate voltage, typical values.

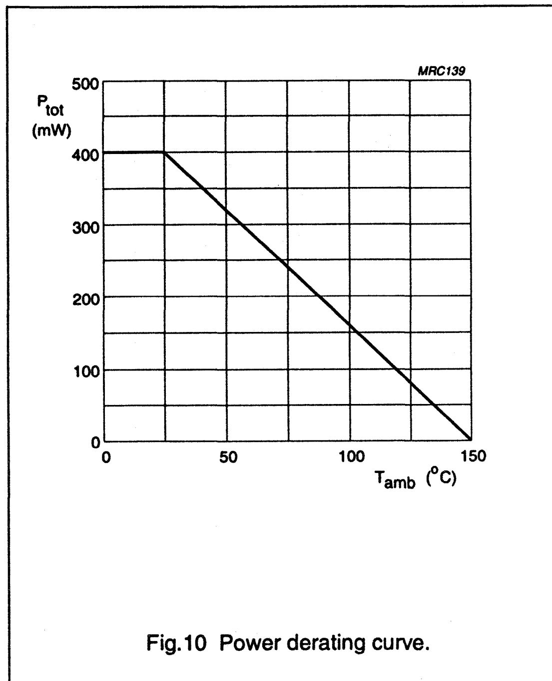
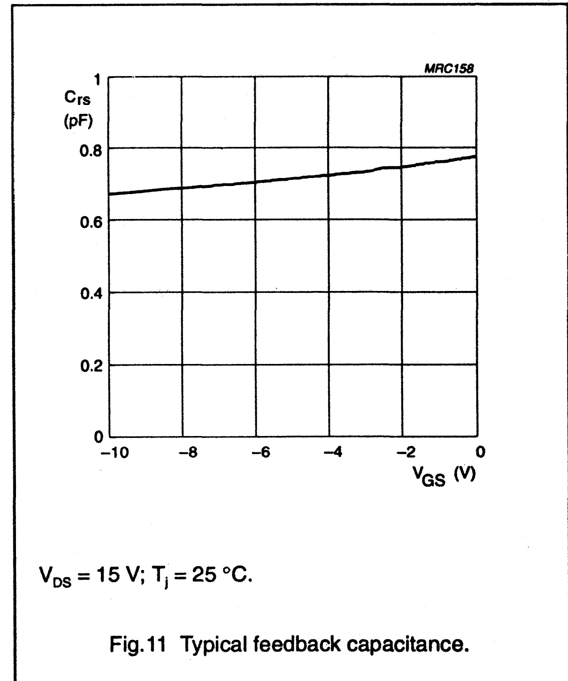
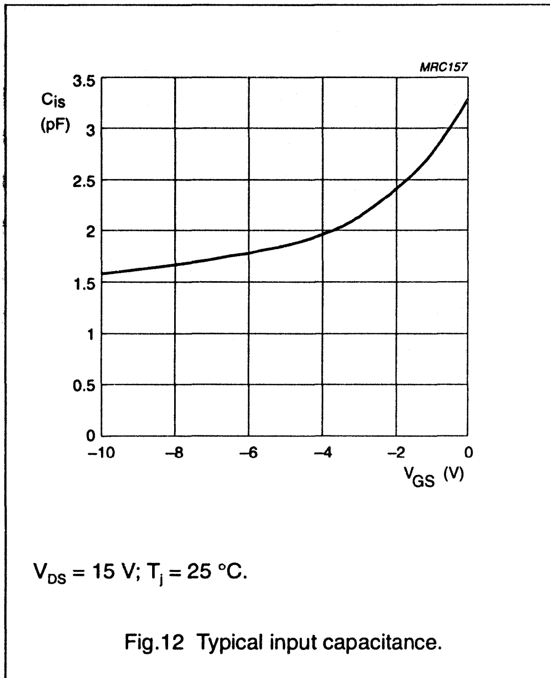


Fig.10 Power derating curve.



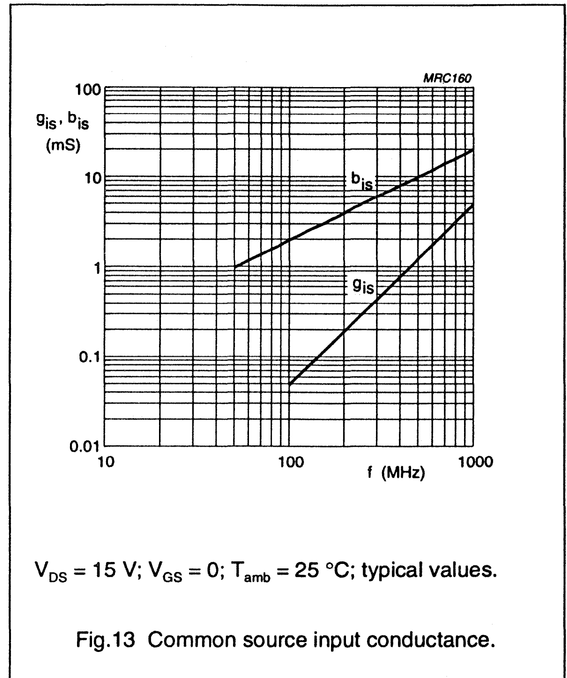
V_{DS} = 15 V; T_j = 25 °C.

Fig.11 Typical feedback capacitance.



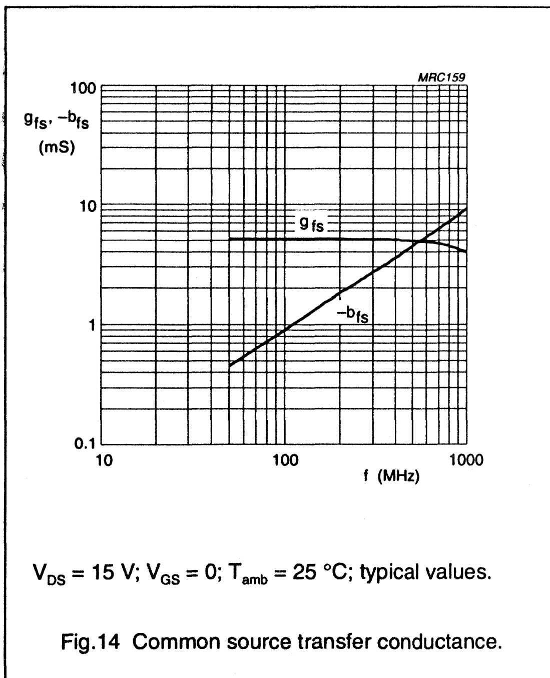
V_{DS} = 15 V; T_j = 25 °C.

Fig.12 Typical input capacitance.



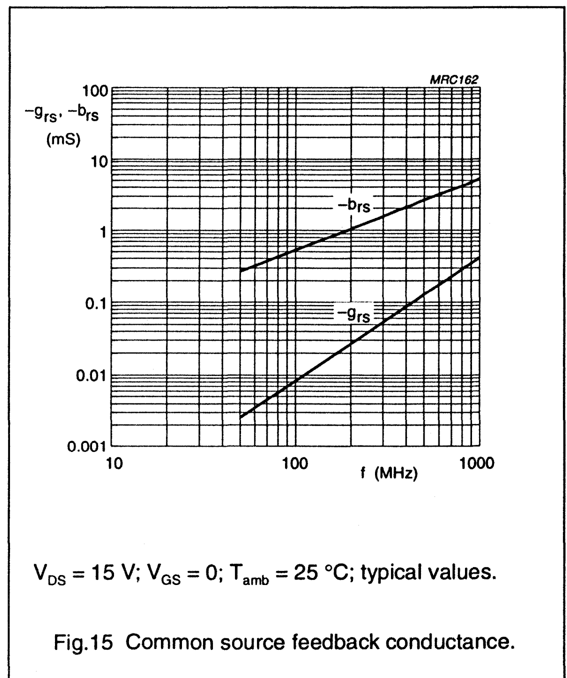
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.13 Common source input conductance.



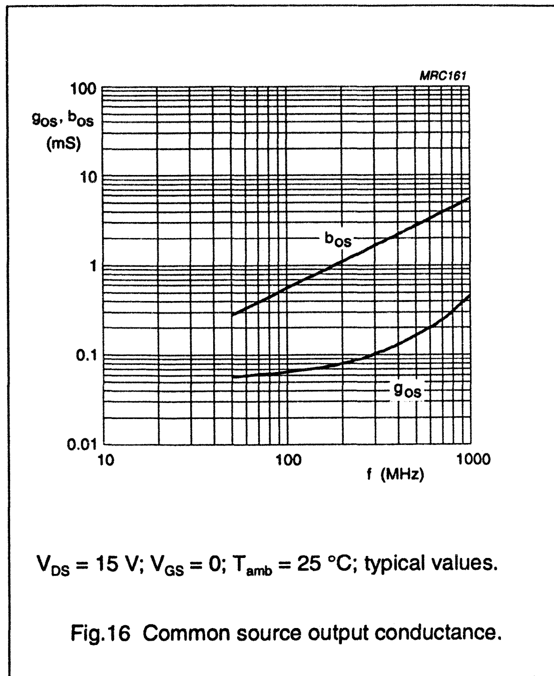
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.14 Common source transfer conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.15 Common source feedback conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.16 Common source output conductance.

Data sheet	
status	Product specification
date of issue	October 1990

2N7000
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	280	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

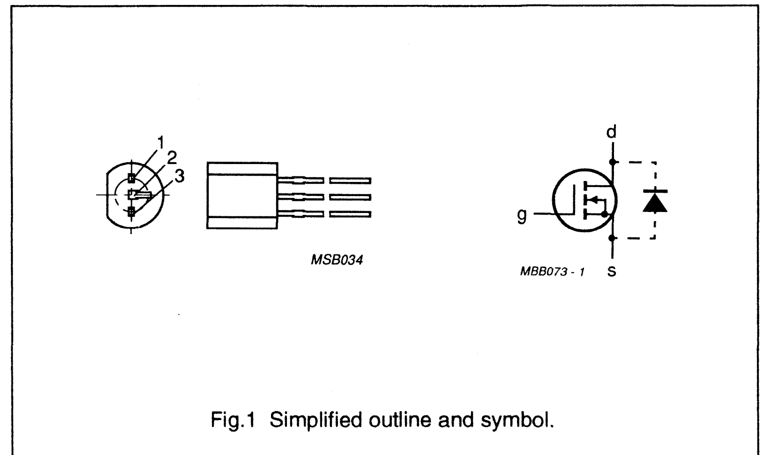


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	280	mA
I_{DM}	drain current	peak value	–	1.3	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	2.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\lvert Y_{fs}\rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns

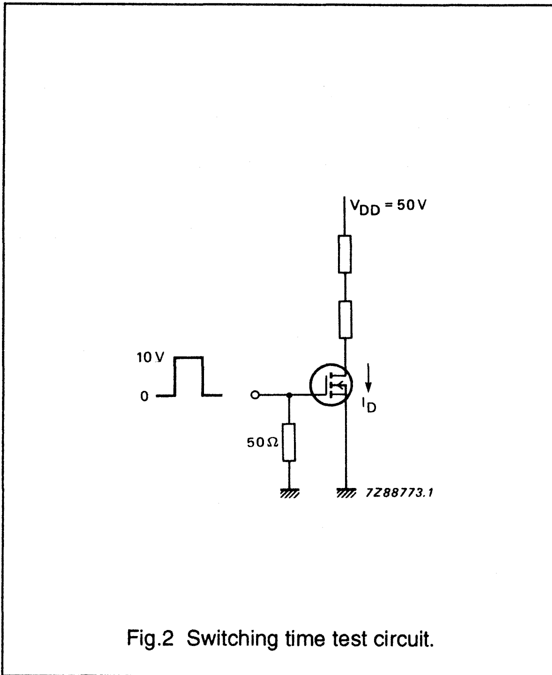


Fig.2 Switching time test circuit.

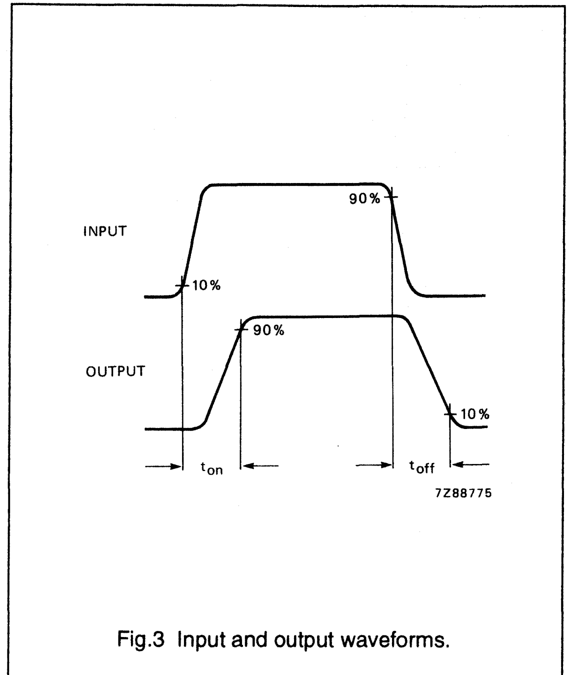


Fig.3 Input and output waveforms.

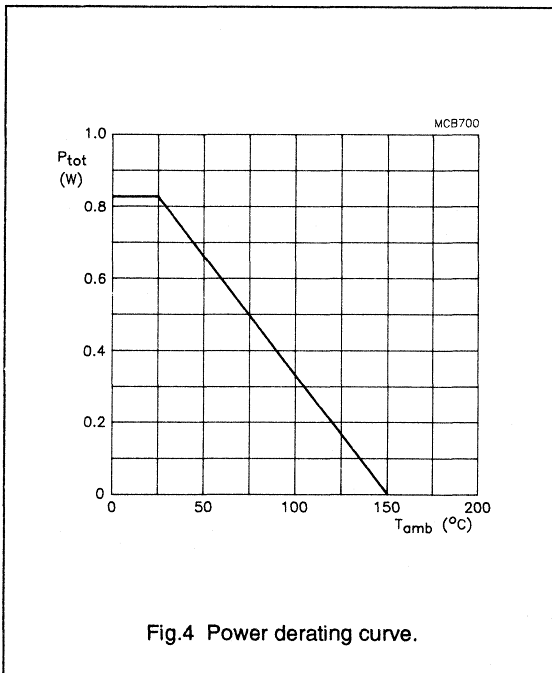


Fig.4 Power derating curve.

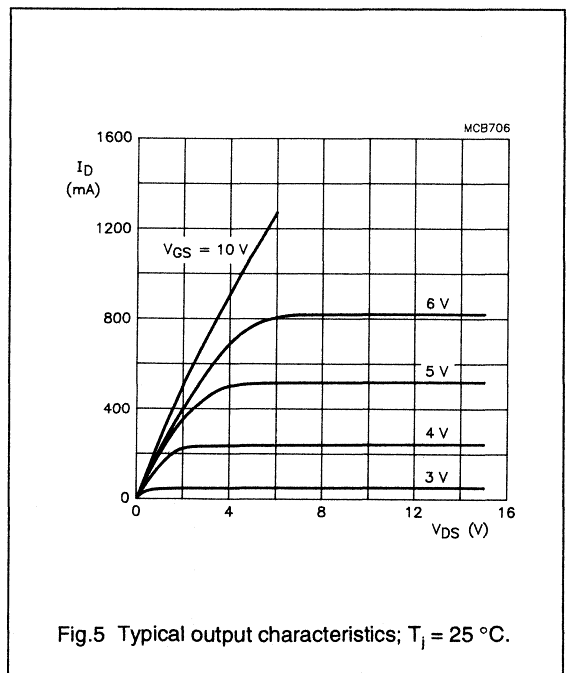


Fig.5 Typical output characteristics; $T_j = 25$ °C.

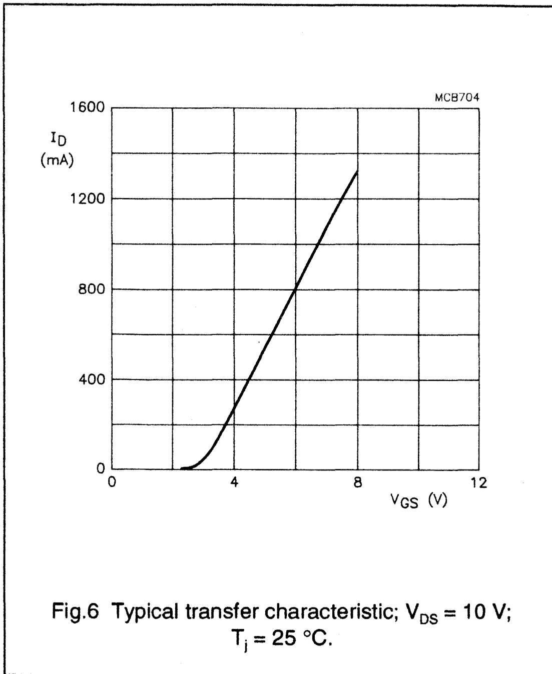


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

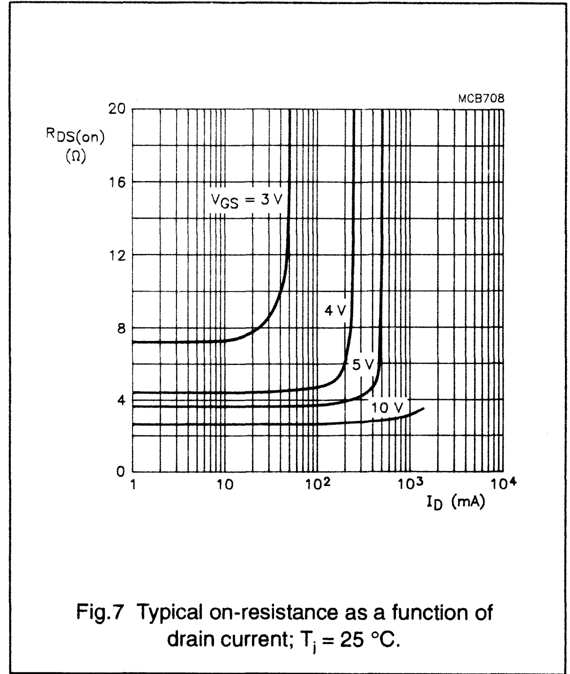


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

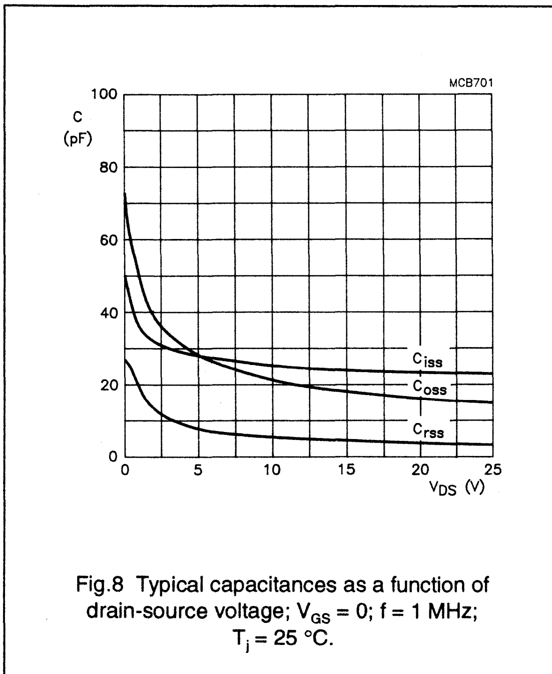
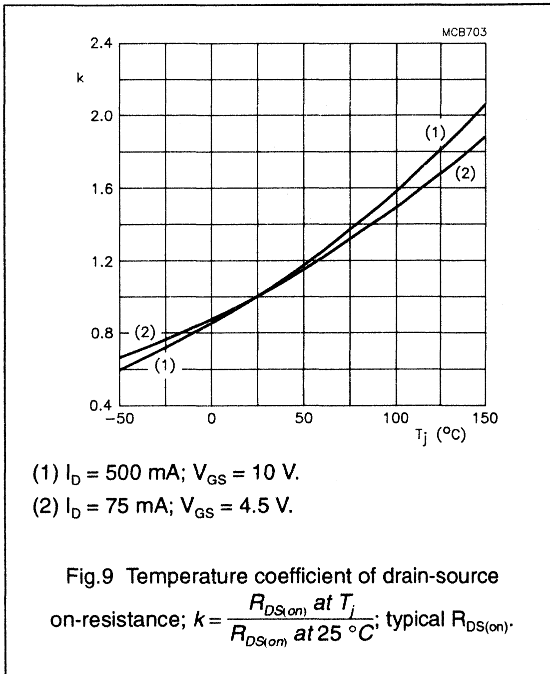


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor 2N7000



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\,°C}$; typical $R_{DS(on)}$.

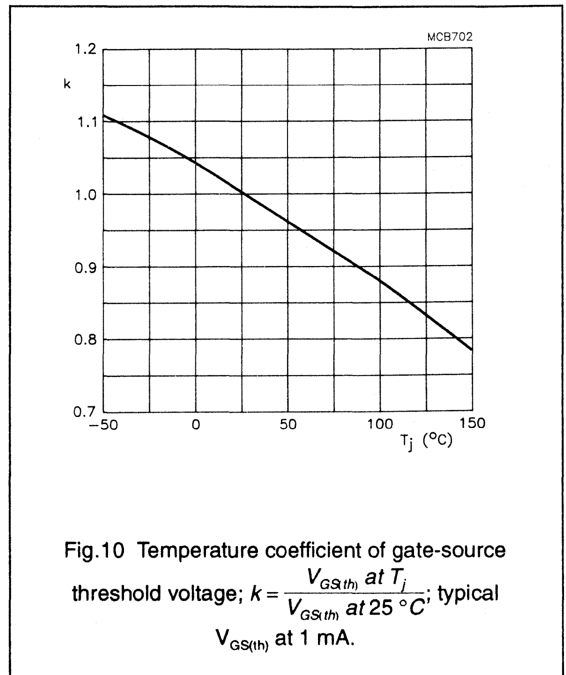


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\,°C}$; typical $V_{GS(th)}$ at 1 mA.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1991

2N7002
N-channel vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

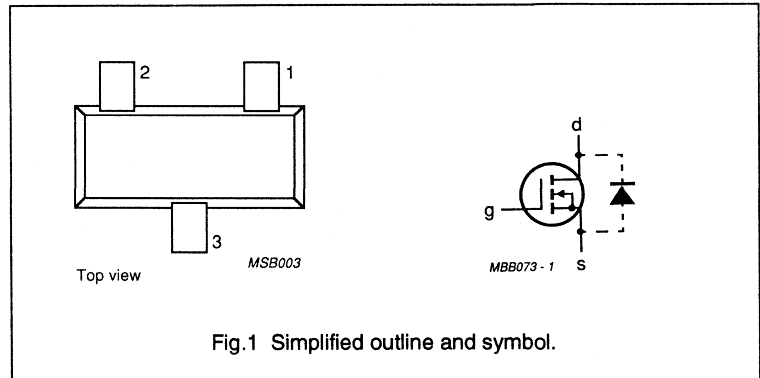


Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor

2N7002

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	180	mA
I_{DM}	drain current	peak value	–	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1) (note 2)	 – –	 300 250	 mW mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted on a ceramic substrate measuring 10 x 8 x 0.7 mm.
2. Mounted on a printed circuit board.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	note 1 note 2	430 500	K/W K/W

Notes

1. Mounted on a ceramic substrate measuring 10 x 8 x 0.7 mm.
2. Mounted on a printed circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	2.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	15	ns

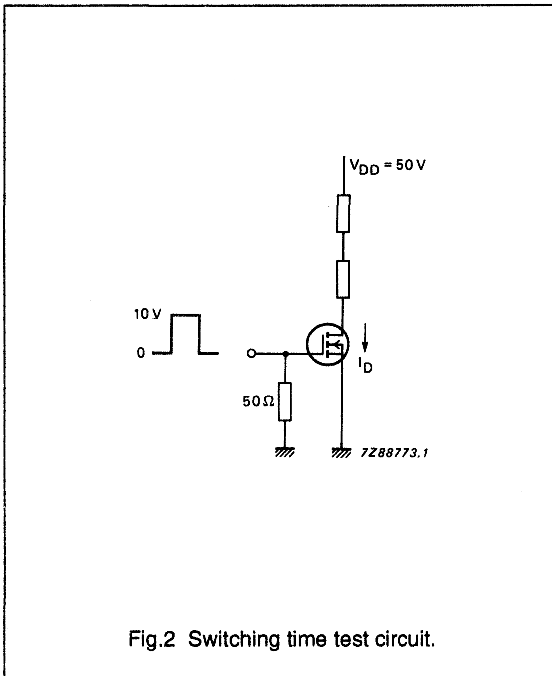


Fig.2 Switching time test circuit.

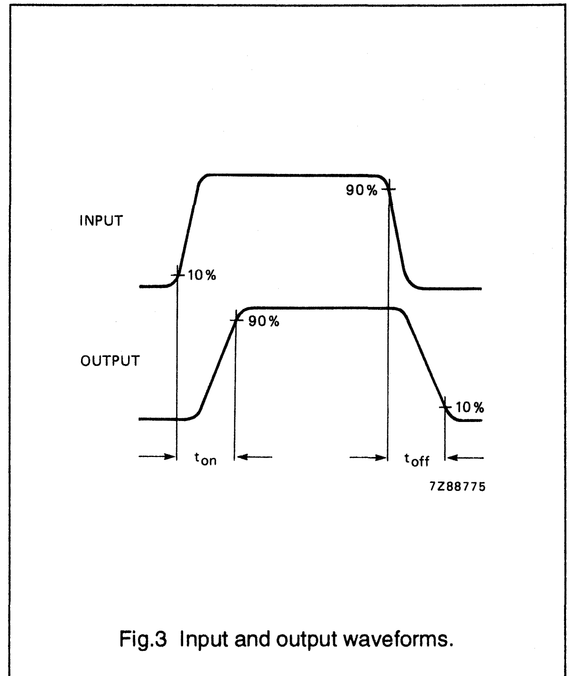
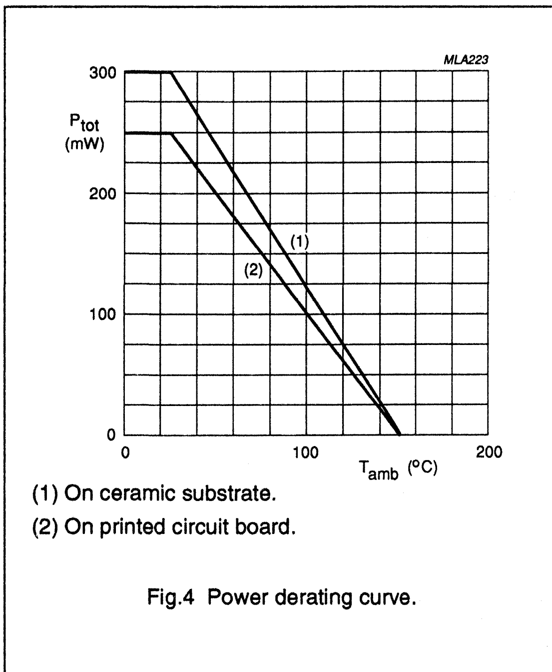


Fig.3 Input and output waveforms.



(1) On ceramic substrate.

(2) On printed circuit board.

Fig.4 Power derating curve.

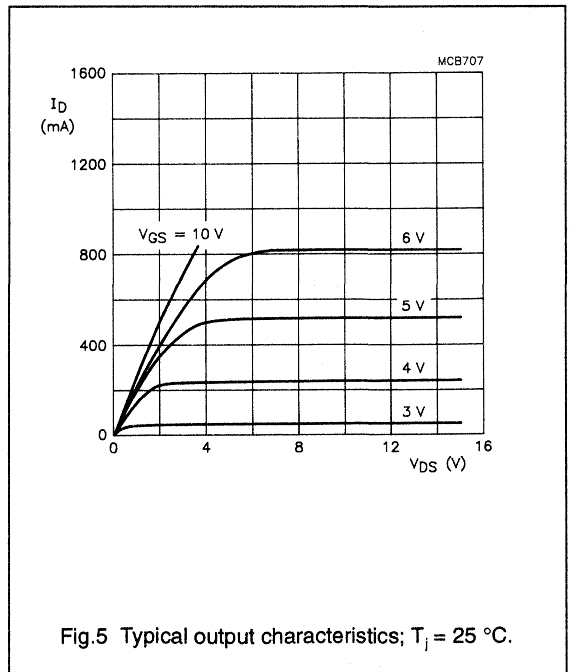


Fig.5 Typical output characteristics; T_j = 25 °C.

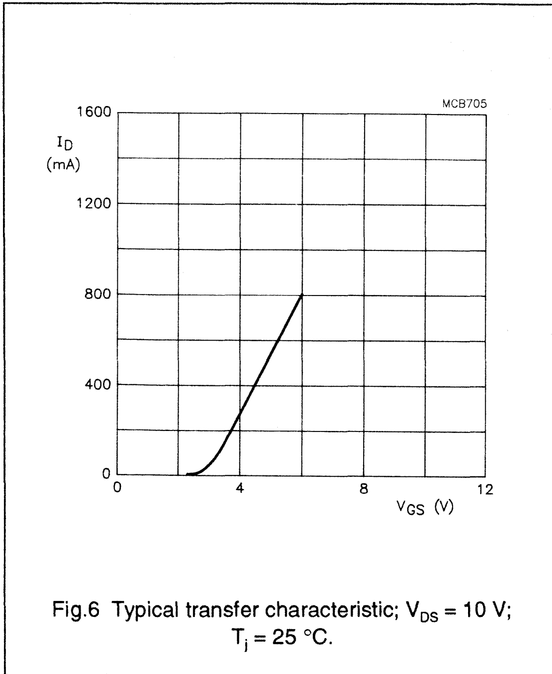


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

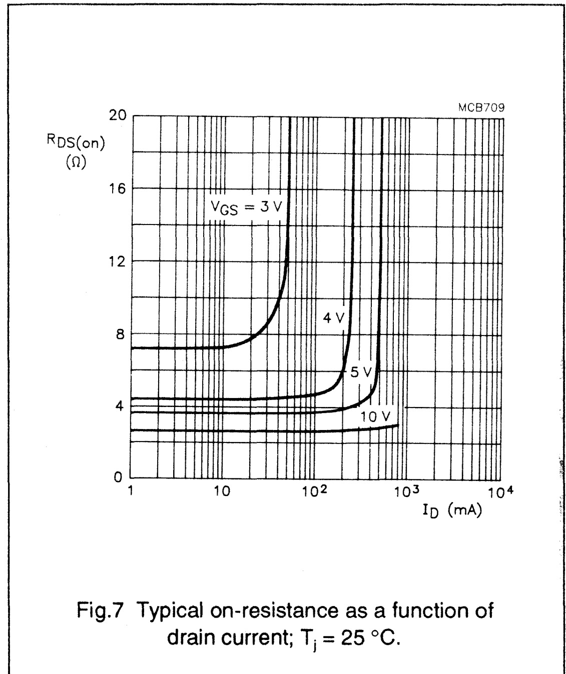


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

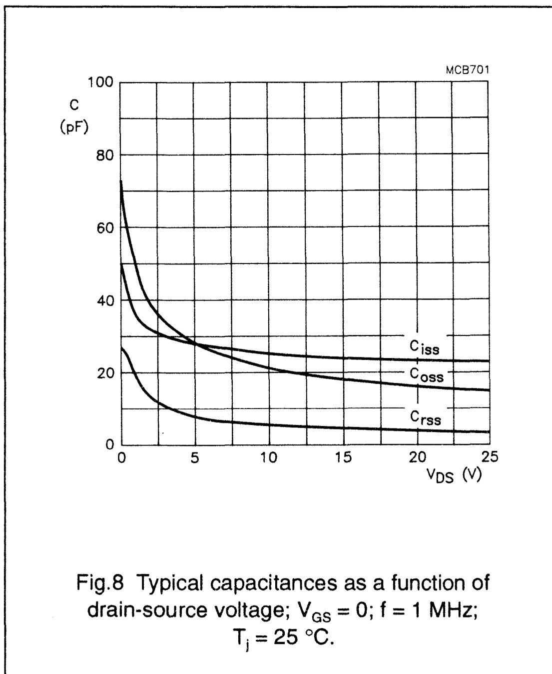
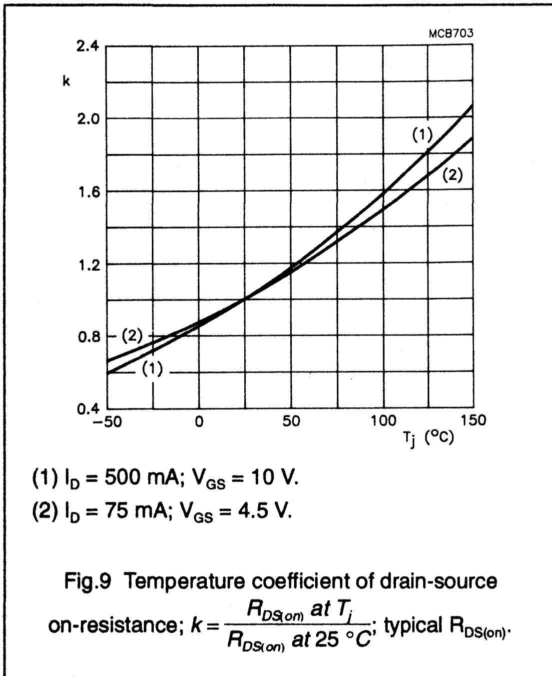


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel vertical D-MOS transistor

2N7002



(1) I_D = 500 mA; V_{GS} = 10 V.

(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$.

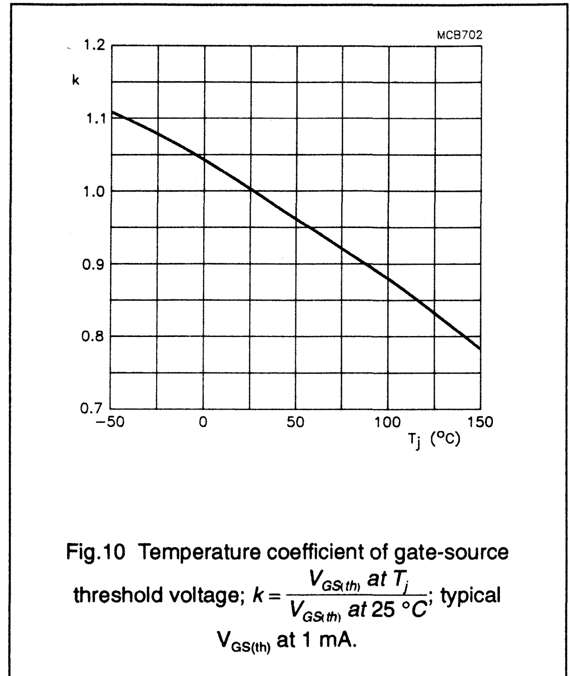
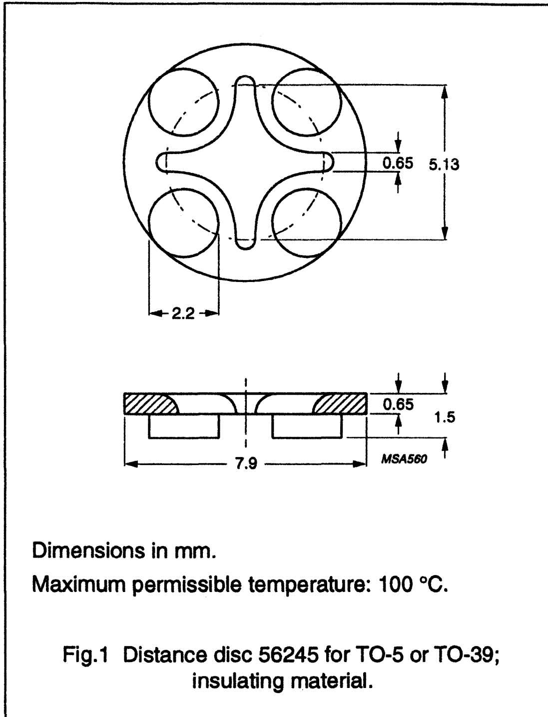


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

ACCESSORIES

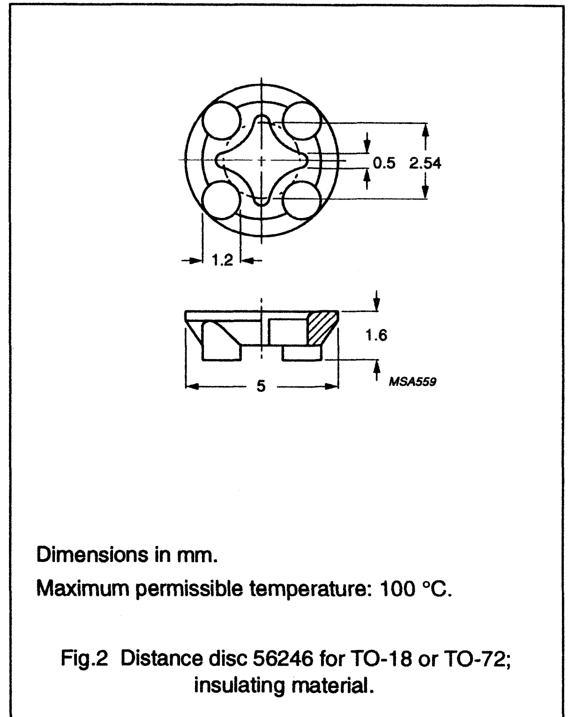
MECHANICAL DATA



Dimensions in mm.

Maximum permissible temperature: 100 °C.

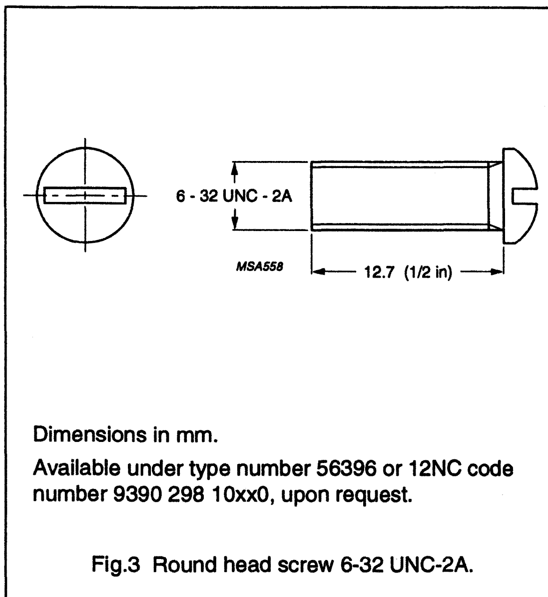
Fig.1 Distance disc 56245 for TO-5 or TO-39; insulating material.



Dimensions in mm.

Maximum permissible temperature: 100 °C.

Fig.2 Distance disc 56246 for TO-18 or TO-72; insulating material.

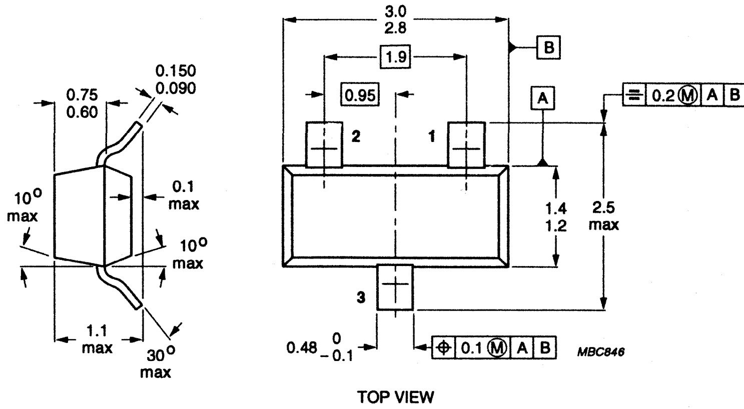


Dimensions in mm.

Available under type number 56396 or 12NC code number 9390 298 10xx0, upon request.

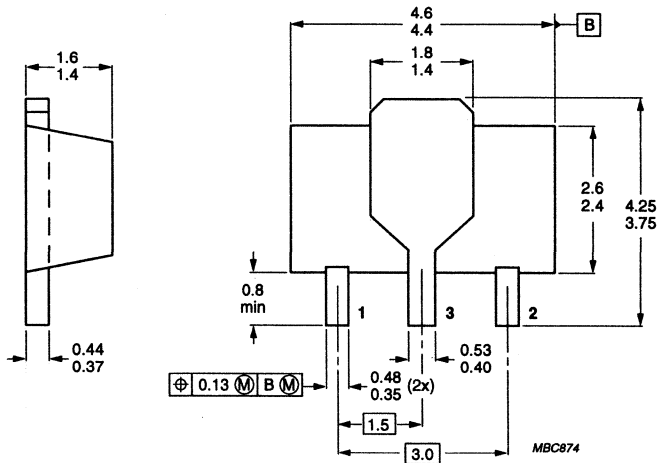
Fig.3 Round head screw 6-32 UNC-2A.

ENVELOPES



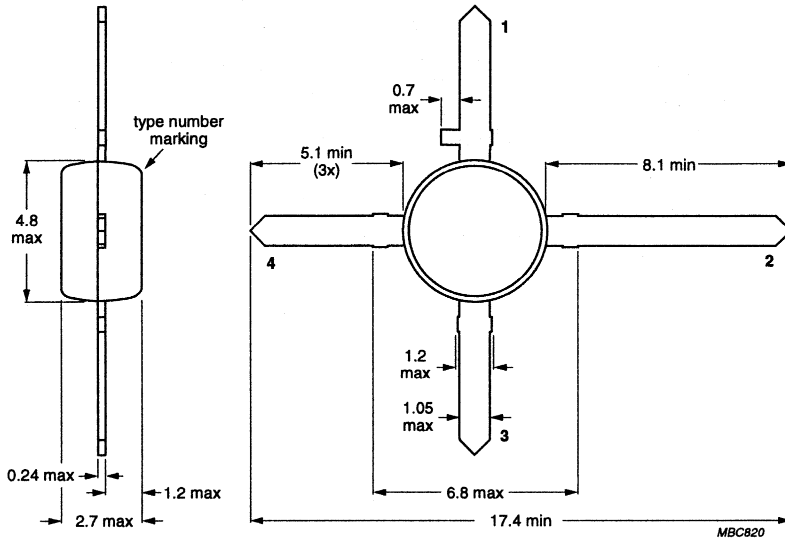
Dimensions in mm.

Fig.1 SOT23.



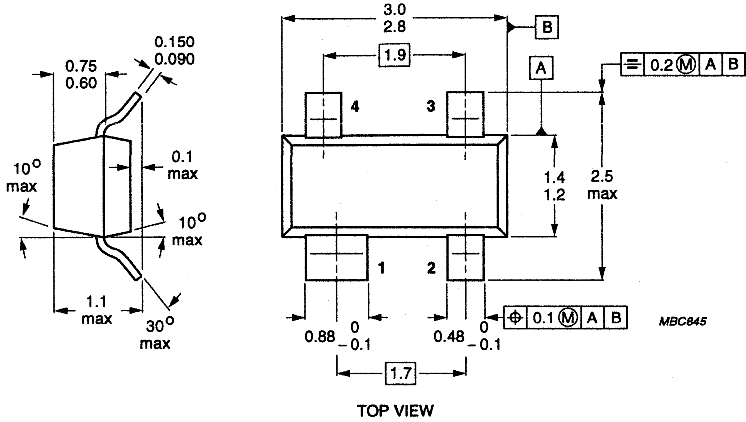
Dimensions in mm.

Fig.2 SOT89.



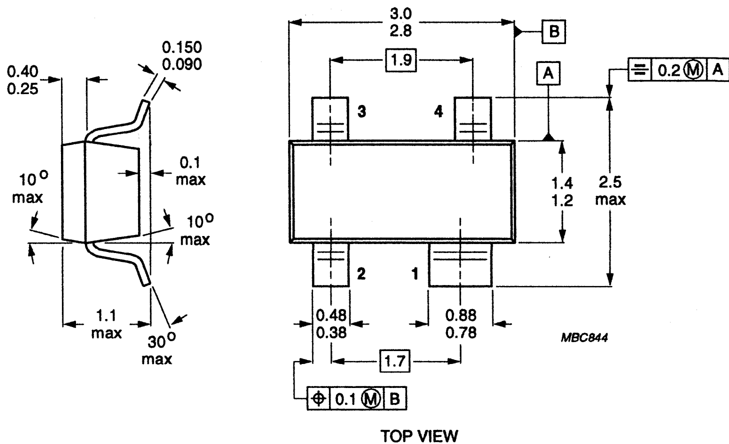
Dimensions in mm.

Fig.3 SOT103.



Dimensions in mm.

Fig.4 SOT143.



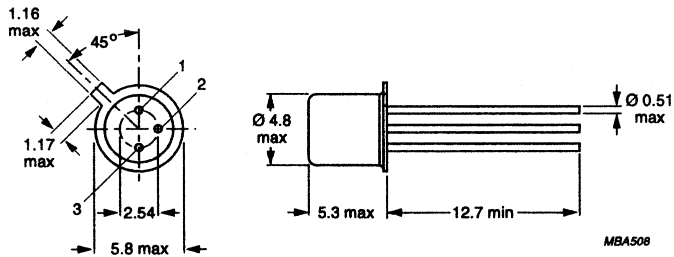
Dimensions in mm.

Fig.5 SOT143R.

0.32
0.24
0.10
0.02
16°
max
13°
1.80
max
10°
max
1.70
1.45
0.73
0.67
6.7
6.3
B
3.1
2.9
0.2 M A
4
A
3.7
3.3
7.3
6.7
1
2
3
1.05
0.85
2.3
0.80
0.60
0.1 M B
(4x)
4.6
MSA035

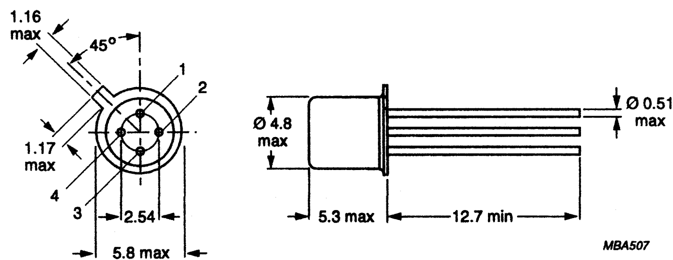
Dimensions in mm.

Fig.6 SOT223.



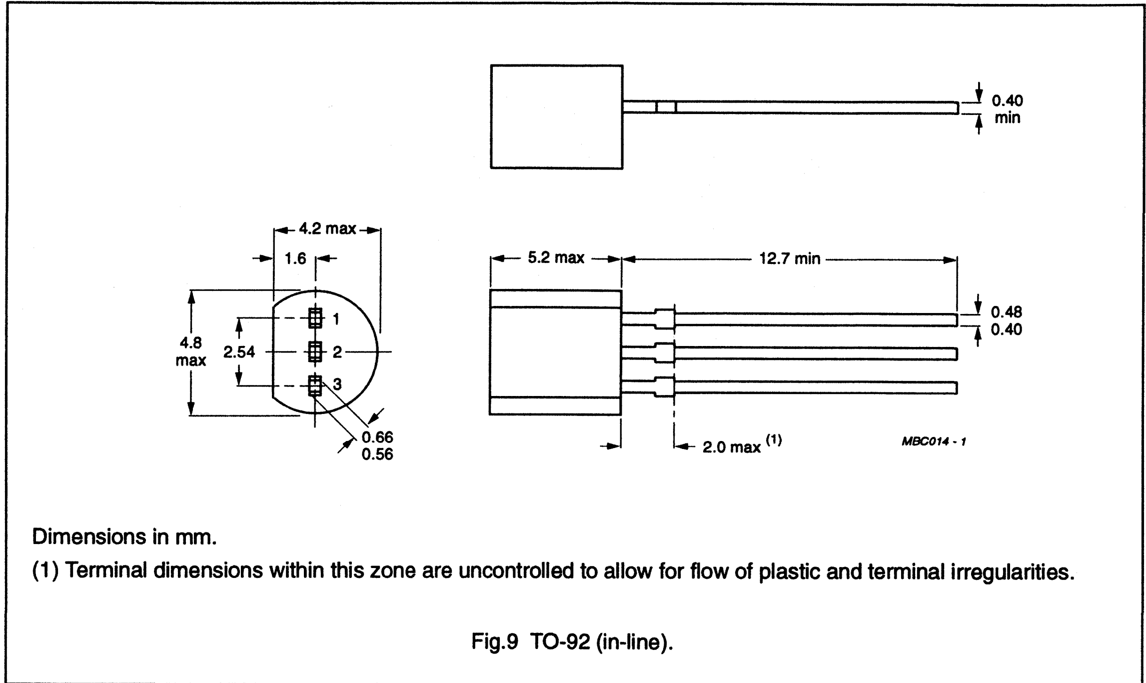
Dimensions in mm.

Fig.7 TO-18.



Dimensions in mm.

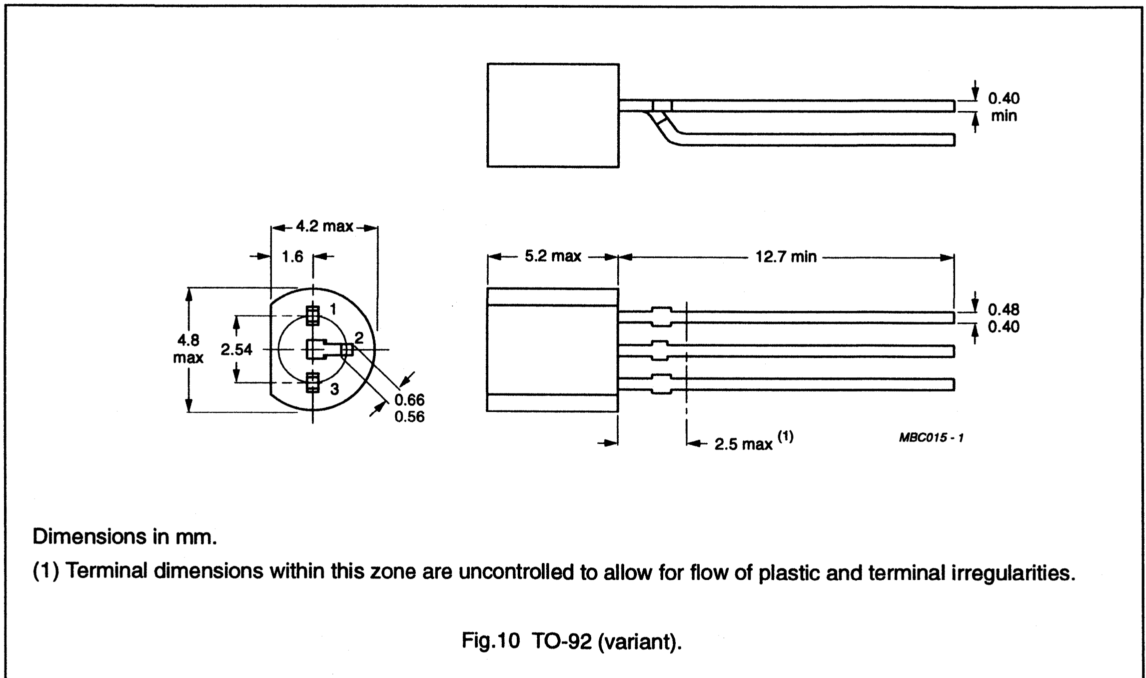
Fig.8 TO-72.



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

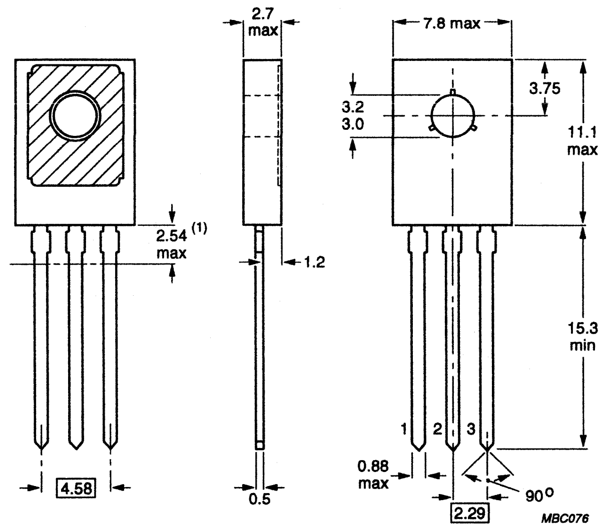
Fig.9 TO-92 (in-line).



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.10 TO-92 (variant).



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled.

Fig.11 TO-126.

DATA HANDBOOK SYSTEM

Data handbook system

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogues are available for selected product ranges (some catalogues are also on floppy discs).

Our data handbook titles are listed here.

Integrated circuits

Book	*Title*
IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	100K ECL Logic Family
IC10	Memories
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals (planned)
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications (planned)
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fibre Optics
IC20	8051-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers (planned)
IC22	ICs for Multi-media Systems (planned)
IC23	QUBIC Advanced BiCMOS Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS Logic

Discrete semiconductors

Book	*Title*
SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC13	PowerMOS Transistors including TOPFETs and IGBTs
SC14	RF Wideband Transistors, Video Transistors and Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Professional components

PC01	High-power Klystrons and Accessories
PC06	Circulators and Isolators

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Data handbook system

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display components

Book	*Title*
DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

Magnetic products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Applications
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

Professional components

PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC12	Electron Multipliers

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Belgium: BRUXELLES, Tel. (02)741 8211, Fax. (02)735 8667.
Brazil: SÃO PAULO, Tel. (011)829 1166, Fax. (011)829 1849.
Canada: SCARBOROUGH, Tel. (416)292 5161, Fax. (416)754 6248.
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